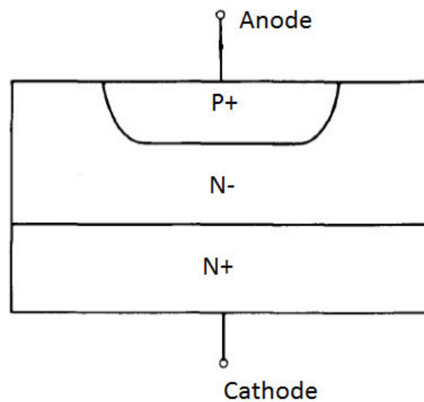
SHIVAJI UNIVERSITY, KOLHAPUR
B.Sc. (Part III) Semester -V
*Electronics (Paper-XII)*
*Power Electronic Devices and Applications*

**Unit 1:-Power Diodes and Transistors (12 Marks)**

# *Power Diode*

Power Diode is the two terminals (namely anode and cathode), two layer (P-N) device which is used in most of the power electronics circuits. The power semiconductor diode is similar to low power PN junction diode (signal diode). In fact, power diode is more complex in structure and in operation than their low power counterparts. This complex happens because low power device must be modified to make them suitable for high power applications.

**Construction of the diode (drift layer):-**

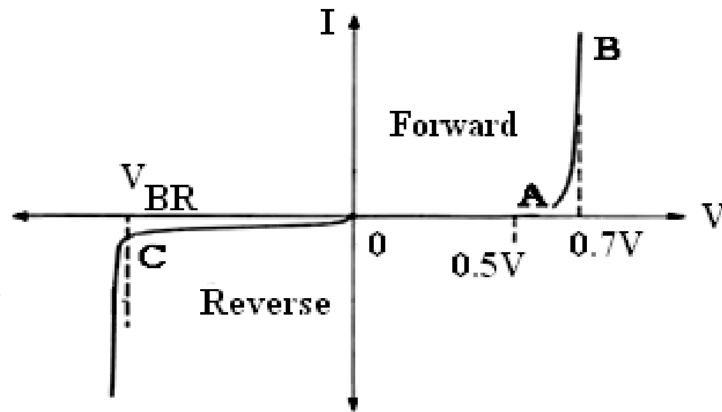



- As shown in the figure, there is heavily doped N+ substrate with doping level of $10^{19}/cm^3$. This substrate forms a cathode of the power diode.
- On N+ substrate, lightly doped N- epitaxial layer is grown. This layer is also known as drift region. The doping level N- layer is about $10^{14}/cm^3$.
- The PN junction is formed by diffusing a heavily doped P+ region. This P+ region forms anode of the diode. The doping level of P+ region is about $10^{19}/cm^3$.
- The thickness of P+ region is 10 um. The thickness of N+ substrate is 250 um.
- The thickness of N- drift region depends upon the breakdown voltage of the diode.
- The drift region determines the reverse breakdown voltage of the diode.
- Its function is to absorb the depletion layer of the reverse biased P+N- junction.
- As it is lightly doped, it will add significant ohmic resistance to the diode when it is forward biased.
- For higher breakdown voltages, the drift region is wide.
- The N- drift region is absent in low power signal diodes.

**Conductivity Modulation of drift layer:-**

- When the power diode is forward biased, the holes will be injected from P+ region into the drift region.
- Some of the holes combine with the electrons in the drift region. Since injected holes are large, they attract electrons from the N- layer.
- Thus holes and electrons are injected in the drift region simultaneously.
- Hence resistance of the drift region reduces significantly.
- Thus diode current goes on increasing, but drift region resistance remains constant.
- So on-state losses in the diode are reduced. This phenomenon is called as Conductivity Modulation of drift region.

**I-V characteristics:-**



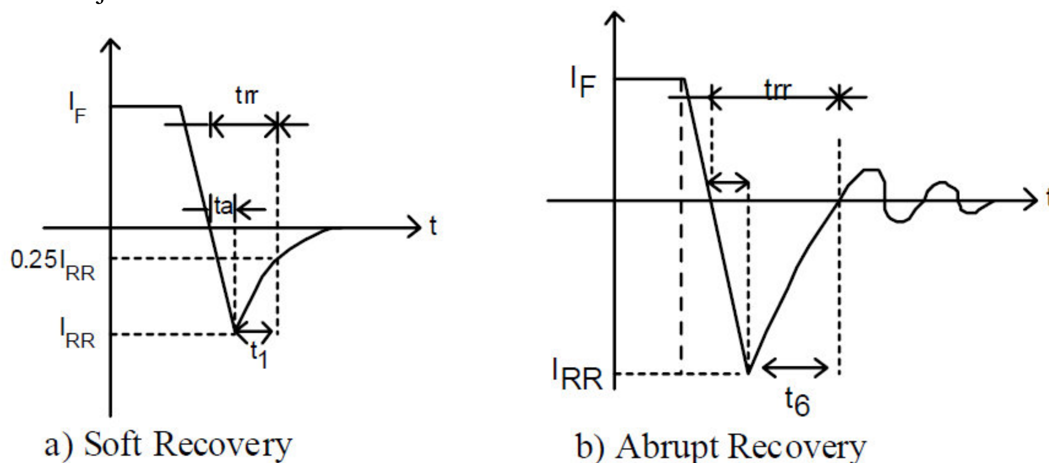

**Forward biased mode: -** With a small forward biased the current increases very slowly and the curve is non-linear as shown by the region OA. This is because the external applied voltage is used in overcoming the potential barrier. However once the external voltage exceeds the potential barrier voltage, the diode behaves like a conductor. Therefore current rises very sharply with the increases in external voltage as shown by the region AB. The forward voltage at which the current through the diode increases very rapidly is called as **cut-in voltage** or **knee voltage**. It is 0.3 for Ge and 0.7 for Si.

**Reverse biased mode: -** With the reverse bias to the diode the potential barrier at the junction goes on increasing. Therefore the diode resistance also increases and thus no current flows through the junction because of majority carriers. But a very small current of the order of few microamperes flows through the diode because of minority carriers as shown by the region OC.

If reverse voltage is increased continuously, then at a particular reverse voltage, the number of carrier crossing the junction increases giving rise to sudden increase in current. The corresponding reverse voltage at which break down of junction occurs is called break down voltage.

**Reverse Recovery effect:-**

The current in a forward leased junction diode is due to the net effect of majority and minority carriers. Once a diode is in forward conductor mode and then it's forward current is reduced to zero, the diode continuity to conduct due to minority carrier which remain store in P-N Junction and bulk semi-conductor material. The minority carrier requires a certain time to recombine with opposite charges and to be neutralized. This time is called reverse recovery time of the diode. Figure shows two reverse recovery characteristics of a junction diode.




a) Soft Recovery b) Abrupt Recovery

From the graph it can be seen that, $t_{rr} = t_a + t_b$

$t_{rr}$ = reverse recovery time

$I_{RR}$ = maximum reverse current

$t_a$ = time between zero crossing and the maximum reverse current and it is due to the charge stored in the depletion region of the junction

$t_b$ = time between maximum reverse current $I_{RR}$ and 25% of the of the maximum reverse current $I_{RR}$ and is due to charge stored in the bulk semiconductor material

The ratio $t_a / t_b$ is known as Softness Factor, denoted by SF.

Reverse recovery time ($T_{RR}$) may be defined as the time interval between the instant the current passes through zero during the change over from forward conduction to reverse blocking conduction and the movement, the reverse current has decayed to 25% of its peak reverse value $I_{RR}$. Its magnitude depends on:

1. Junction temperature
2. Rate of fall of forward current
3. Forward current prior to commutation

**Types of Diodes:-**

1. Standard Diodes or General Purpose Diodes: -

Standard or general purpose diodes have a comparatively high reverse recovery time, when compared to other diodes. Due to this reason they are used in applications which are not time sensitive and generally run on low speeds. Usually the reverse recovery time for general purpose diodes varies between 20 micro seconds to 30 micro seconds which is quite a lot. Typical low speed applications for general purpose diodes include the power diode being used as a rectifier or in a converter, where the frequency input is quite low.

2. Fast Recovery Diodes:-

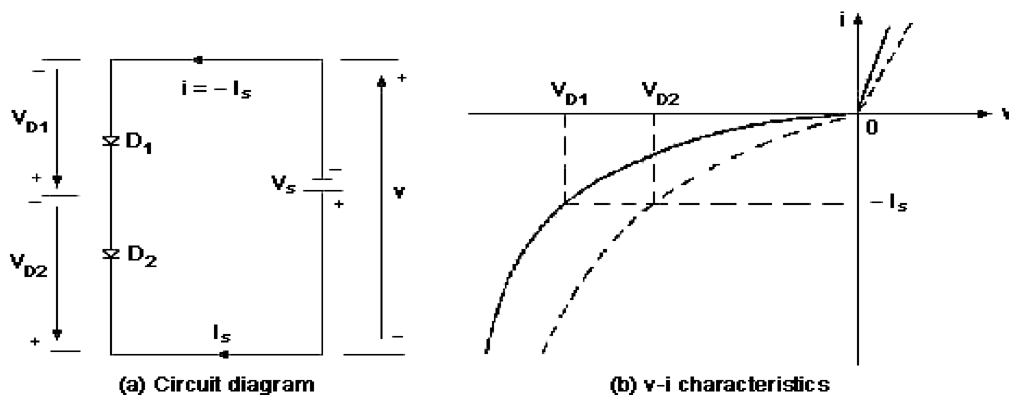
As their name suggests, these are the type of power diodes which have a relatively faster reverse recovery time, which usually varies from 2 micro seconds to 5 micro seconds. With such a fast recovery time, they can be easily used in high speed switching applications where the time is of great importance. Due to their property of fast reverse recovery, they are also comparatively expensive as compared to the general purpose diodes.

3. Schottky Diodes:-

Sometimes we face problem in charge storage in a PN-junction. This thing can be minimized to a great extent in a Schottky diode. A Schottky diode sets a barrier potential, i.e. a metal layer is deposited on n-type silicon. As the rectification depends upon the majority charge carriers, so this layer prevents the recombination of these majority charge carriers, and a fast recovery can also be achieved in this way.

**Series Connected Diodes:-**

A single diode cannot meet higher voltage requirements and therefore diodes are connected in series to increase the reverse blocking capabilities.

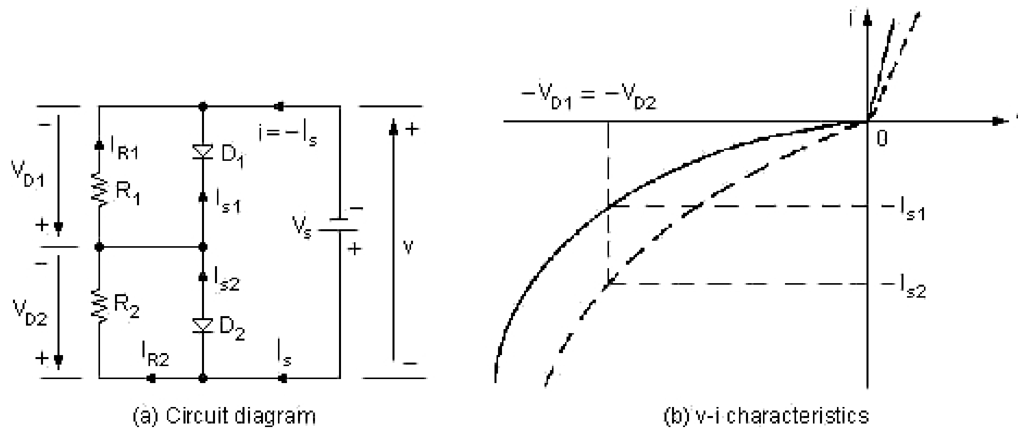


(a) Circuit diagram (b) v-i characteristics

Consider two identical diodes $D_1$ and $D_2$ are connected in series. As $D_1$ and $D_2$ both are same, there I-V characteristics also same. But, in practical, the I-V characteristics of same type of diodes differ due to the tolerances in their production.

In forward biased state, the voltage drop and the forward current would be same on the diodes. While in the reverse biased the blocking voltages $V_{D1}$ and $V_{D2}$ are different as the diodes have to carry the same leakage current.

This problem can be solved by connected resistances across every diode. Voltage would be shared equally; hence the leakage current would differ.



(a) Circuit diagram (b) v-i characteristics

Total leakage current would now be:

$$I_S = I_{S1} + I_{R1} = I_{S2} + I_{R2}$$

Our requirement is:

$$V_{D1} = V_{D2}$$

We know,

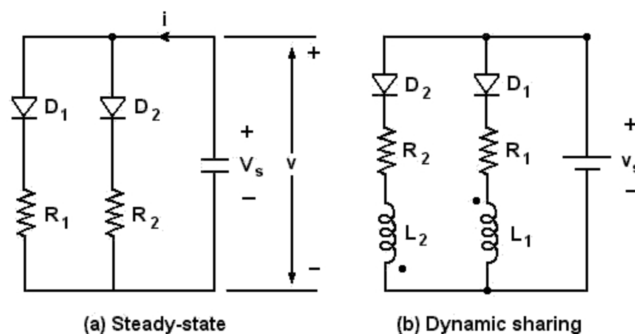
$$I_{R1} = \frac{V_{D1}}{R_1} \qquad I_{R2} = \frac{V_{D1}}{R_2}$$

So we get,

$$I_{S1} + \frac{V_{D1}}{R_1} = I_{S2} + \frac{V_{D1}}{R_2}$$

**Parallel Connected Diodes:-**

A single diode cannot meet higher current requirements and therefore diodes are connected in parallel.

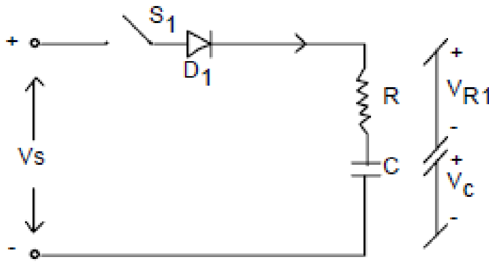


(a) Steady-state (b) Dynamic sharing

Consider two diodes connected in parallel configuration. Current would be shared among the two diodes. To make this sharing equal, inductors (with same inductances) are connected.

Inductors are used for dynamic conditions. When current at D1 increases, the voltage drop across L1 increases, generating an opposite polarity value at L2. Therefore current through D2 increases and uniform current sharing is achieved.

**Diodes with RC load:-**




When switch $s_1$ is closed at t=0

$$V_s = V_R + V_c$$

$$= R_i + \frac{1}{c}\int idt + V_c(t=0)$$

With initial condition, $V_c(t=0)=0$

$$\frac{V_s}{s} \neq RI(s) + \frac{I(s)}{s}$$

$$or,\ \left(R + \frac{1}{cs}\right)I(s) = \frac{V_s}{s}$$

$$or,\ \left(\frac{Rcs+1}{cs}\right)I(s) = \frac{V_s}{s}$$

$$or,\ I(s) = \frac{Vsc}{Rc(s+1/Rc)}$$

$$or, I(s) = \frac{Vs}{R(s+1/Rc)}$$

Taking Inverse Laplace,

$$i(t) = \frac{V_s}{R}e^{-t/Rc}$$

Capacitor Voltage

$$V_c(t) = \frac{1}{c}\int_0^t idt$$

$$= \frac{1}{c}\int_0^t \frac{V_R}{R}e^{-t/Rc}dt$$

$$= \frac{V_s}{Rc}\left[\frac{e^{-t/Rc}}{-1/Rc}\right]^t$$

$$= V_s\left[1 - e^{-t/Rc}\right]$$

$$= V_s\left[1 - e^{-t/T}\right]$$

T = Rc = Time constant of Rc load.

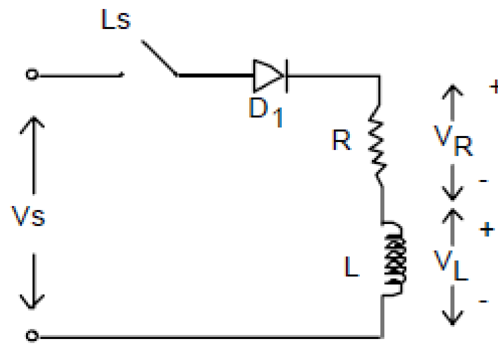
The rate of change of capacitor voltage is

$$\frac{dV_c(t)}{dt} = -V_s\left(-\frac{1}{Rc}\right)e^{-1/Rc^t} = \frac{V_s}{Rc}e^{-t/Rc}$$

& the initial rate of change of capacitor voltage (at t=0) is

$$\left.\frac{dV_c(t)}{dt}\right|_{t=0} = \frac{V_s}{Rc}$$

**Diodes with RL load:-**




When switch S is closed at t=0

$$V_s = V_R + V_L$$

$$= Ri + L\frac{di}{dt} \text{ z}$$

$$\frac{V_s}{s} = RI(s) + L[sI(s)) - i(0)]$$

With initial condition i(0) = 0

$$\frac{V_s}{s} = RI(s) + LsI(s)$$

$$(R + Ls)I_s = \frac{V_s}{s}$$

$$I(s) = \frac{V_s}{s(R + Ls)}$$

$$= \frac{V_s}{Ls(s + R/L)}$$

$$I(s) = \frac{V_s}{L}\left[\frac{1}{s} - \frac{1}{s + R/L}\right]\frac{L}{R}$$

$$I(s) = \frac{V_s}{R}\left[\frac{1}{s} - \frac{1}{s + R/L}\right]$$

By inversion,

$$i(t) = \frac{V_s}{R}\left(1 - e^{\frac{-R}{L}t}\right) = \frac{V_s}{L}e^{-\frac{R}{L}t}$$

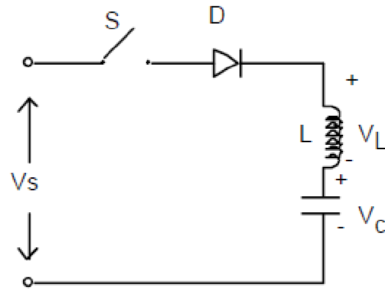
$$\left.\frac{di}{dt}\right|_{t=0} = \frac{V_s}{L}$$

Voltage across inductor,

$$V_L = L\frac{di}{dt} = V_s e^{-\frac{R}{L}t} = V_s e^{-\frac{t}{T}}$$

where, $T = \frac{L}{R} =$ time constant RL load

**Diodes with LC load:-**




At t=0, switch s is closed.

$$V_s = L\frac{di}{dt} + \frac{1}{c}\int_0^t i\,dt + V_c(t=0)$$

$$V_c(t=0) = 0$$

Using Laplace Transform:

$$\frac{V_s}{s} = L[sI(s) - i(0)] + \frac{I(s)}{Cs}$$

$$i(0) = 0$$

$$\left(Ls + \frac{1}{cs}\right)I(s) = \frac{V_s}{s}$$

$$\left(\frac{Lcs^2 + 1}{cs}\right)I(s) = \frac{V_s}{s}$$

$$I(s)) = \frac{CV_s}{LC\left(s^2 + \frac{1}{LC}\right)}$$

$$I(s) = \frac{V_s}{L(s^2 + \omega^2)}, \qquad where\ \omega = \frac{1}{\sqrt{LC}}$$

By inversion,

$$i(t) = \frac{V_s}{L}.\frac{1}{\omega}.\sin\omega t$$

$$= V_s\sqrt{\frac{C}{L}}.\sin\omega t$$

$$i(t) = I_p \sin\omega t \ \ where\ I_p = V_s\sqrt{\frac{C}{L}}$$

$$i(t) = \frac{V_s}{L}.\frac{1}{\omega}.\sin\omega t$$

$$= V_s\sqrt{\frac{C}{L}}.\sin\omega t$$

$$i(t) = I_p \sin\omega t \ \ where\ I_p = V_s\sqrt{\frac{C}{L}}$$

The rate of current is

$$\frac{di}{dt} = I_p.\omega\cos\omega t = V_s\sqrt{\frac{C}{L}}.\frac{1}{\sqrt{LC}}.\cos\omega t$$

$$\frac{di}{dt} = \frac{V_s}{L}.\cos\omega t \qquad -(2)$$

Initial rate of rise of current,

$$\left.\frac{di}{dt}\right|_{t=0} = \frac{V_s}{L} \qquad -(3)$$

Voltage across capacitor

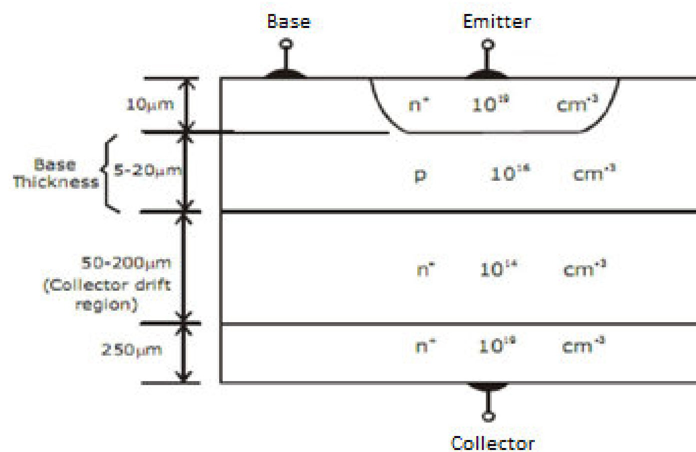
$$V_c(t) = \frac{1}{c}\int_0^t i dt = \frac{1}{c}\int_0^t I_p \sin\omega t dt = \frac{1}{c}.V_s\sqrt{\frac{C}{L}}\left[-\frac{\cos\omega t}{\omega}\right]_0^t$$

$$= \frac{V_s}{\sqrt{LC}}.\frac{1}{\omega}(1-\cos\omega t)$$

$$= V_s(1-\cos\omega t) \qquad -(4)$$

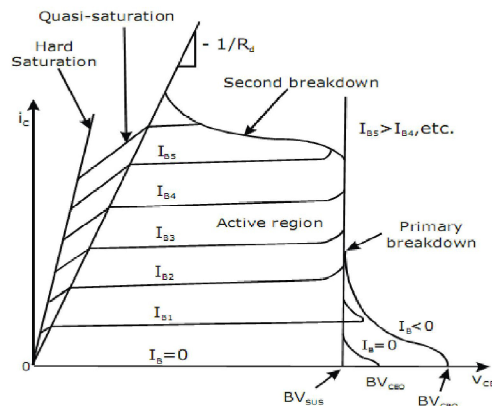
## ***Power Transistors***

**Structure:-**




- A power transistor is a vertically oriented four layer structure of alternating p-type and n-type. This is maximizing the cross-section area results in current rating of BJT, minimize the on-state resistance, and thus reduce the power losses.
- The doping of emitter layer and collector layer is quite large typically 1019 cm-3
- A special layer called the collector drift region (n-) has a light doping level of 1014.
- The thickness of the drift region determines the breakdown voltage of the transistor.
- The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

**Operation:-**




Three regions of operation for a BJT can be recognized:

**Cutoff Region:** When the base current ($I_B$) is zero, the collector current ($I_C$) is insignificant and the transistor is driven into the cutoff region. The transistor is now in the OFF state. The collector–base and base–emitter junctions are reverse biased in the cutoff region or OFF state, and the transistor behaves as an open switch.
In this region: $I_C= 0$ and the collector–emitter voltage $V_{CE}$ is equal to the supply voltage $V_{CC}$

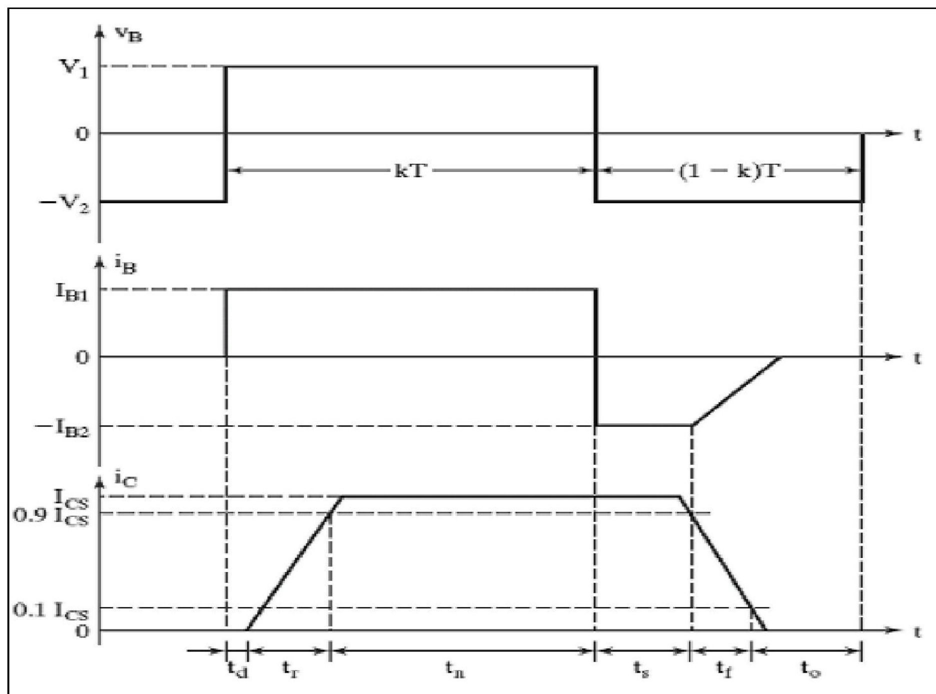
**Saturation Region:** When the base current is sufficient to drive the transistor into saturation. During saturation, both junctions are forward-biased and the transistor acts like a closed switch. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on.
In this region: $I_C = V_{CC} /R_C$ and $V_{CE}$ = zero

**Active Region:** In the active region, the collector–base junction is reversed-biased and the base–emitter junction is forward-biased. The active region of the transistor is mainly used for amplifier applications and should be avoided for switching operation. The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cut-off and saturation.

**Effect of drift layer:-**

In order to block voltage during "**OFF**" state a lightly doped drift region is introduced between the base and collector.

**Switching characteristics:-**




A forward biased PN-junction exhibits two parallel capacitances: a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased PN junction has only depletion capacitance. These capacitances change the turn on and turn off behavior of the transistor.

Due to internal capacitances, the transistor does not turn on instantly.

1. **Delay time**: The time required for the current to rise to 10 present of its maximum value is called as delay time ($t_d$).
2. **Rise time**: The time required for the current to rise from 10 to 90 percent of its maximum value is called as rise time ($t_r$).
3. **Turn ON time**: It is the sum of delay time and rise time, $t_{on}= t_d + t_r$
4. **Storage time**: The interval which elapses between the transition of the input waveform and the time when current has dropped to 90 percent of its maximum current value ($t_s$).
5. **Fall Time**: The time required for current to fall 90 percent 10 percent of its maximum value ($t_f$).
6. **Off time**: It is sum of storage time and fall time, $t_{off} = t_s + t_f$

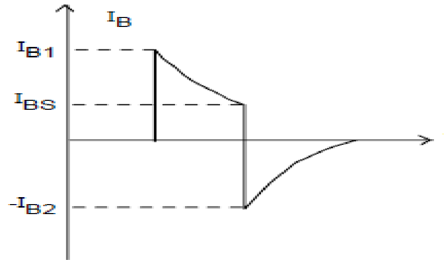
**Base drive circuit:-**

**Requirement of base drive circuit:**

1. The driver circuit should be capable of providing the required amount of base current of a power transistor.
2. The driver circuit must provide a negative base current to turn off a transistor. The negative base current is necessary to reduce the turn off time of the transistor.

**Base current waveform:**

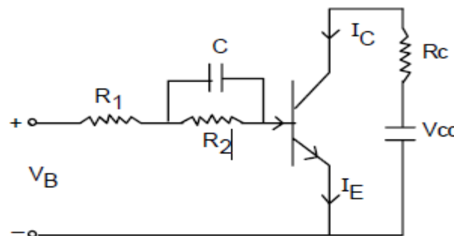
The switching speeds of a power BJT can be increased by reducing the turn on time $t_{on}$ and turn off time $t_{off}$. To achieve this we use a special type of base current waveform as shown in figure below:




1. The switching speed can be increased by reducing the turn on time $t_{on}$. This can be achieved by allowing the base current peaking during the turn on.
2. When the power BJT is conducting its base-emitter junction capacitance store charge. In order to turn off the conducting power BJT this charge should be removed as quickly as possible. This is achieved by drawing a negative base current as shown in figure above.

**Types of Base drive circuit:**

**1. Turn ON control:-**



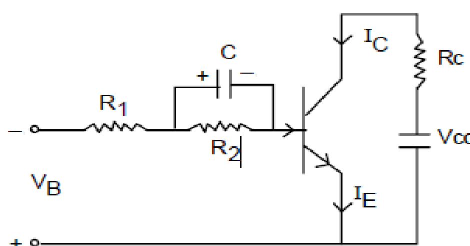

The base current peaking during turn on can be practically obtained by using the circuit shown in figure above. As soon as input is applied, the base voltage is equal to V1 and the initial base current is given by,

$$I_{B0} = \frac{V_1 - V_{BE}}{R_1}$$

But as time passes, C starts charging through $R_1$ and $I_B$ goes on decreasing. This is shown in equivalent circuit. After some time when C is fully charged the base current is given by,

$$I_{B1} = \frac{V_1 - V_{BE}}{R_1 + R_2}$$

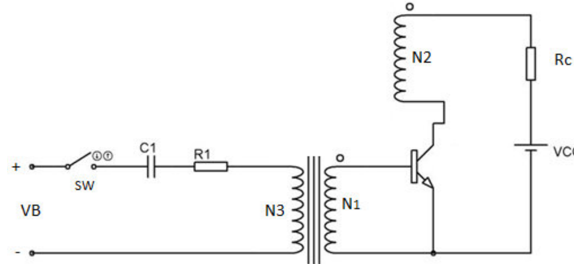
**2. Turn OFF control:-**



If the input voltage $V_B$ in figure is changed to $-V_2$, then the capacitor voltage $V_{C1}$ will get added to $V_B$ as shown in figure above. Hence $V_{BE}$ becomes negative and a reverse base current peaking is observed. The turn-off can be faster if more negative base current is forced to flow as this will remove the stored charges more quickly.

**3. Proportion Base control:-**

In this type of control the base current not kept constant. But if the collector current changes due to fluctuations in load, then the base current is changed in proportion with the collector current.




As we turn on switch, current flows through $C_1$, $R_1$ and $N_3$. Being a capacitor charging current it will be a pulse current of short duration. Due to this current pulse, a pulse current of short duration flows though the base of $Q_1$ and it goes into the saturation state.

As soon as collector current starts flowing a proportional base current is induced due to the transformer action. This will strengthen the collector current further and the transistor will be latching on itself. It will continue to conduct even when switch is open circuited.

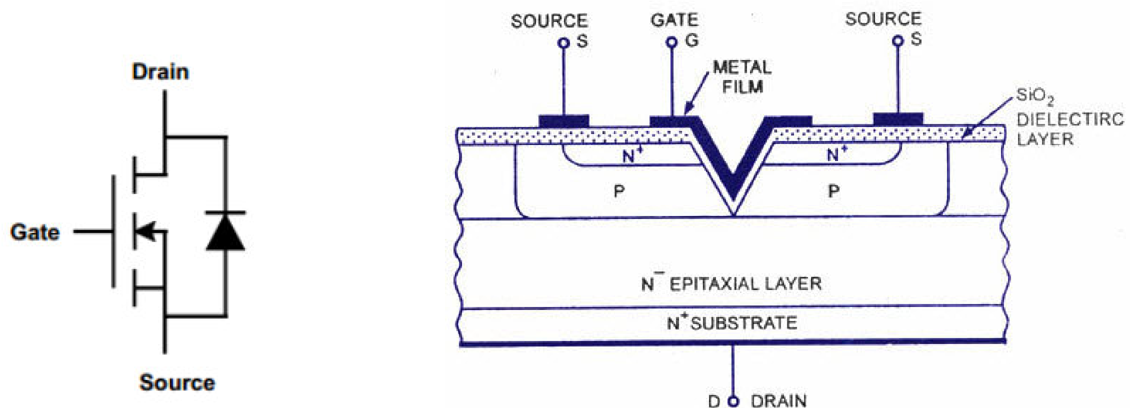
$$\frac{I_C}{I_B} = \frac{N_2}{N_1} = \beta \qquad\qquad I_B = \frac{N_1}{N_2} = I_C$$

Hence, as $I_C$ changes, $I_B$ will also change proportionally.

## ***Power MOSFET***

The Power MOSFET is the three terminal (Gate, Drain and Source), four layer (n+pn-n+), Unipolar only majority carriers in conduction) semiconductor device.

- The MOSFET is a majority carrier device, and as the majority carriers have no recombination delays, the MOSFET achieves extremely high bandwidths and switching times.
- The gate is electrically isolated from the source, and while this provides the MOSFET with its high input impedance, it also forms a good capacitor.
- MOSFETs do not have secondary breakdown area; their drain to source resistance has a positive temperature coefficient, so they tend to be self protective.
- It has very low ON resistance and no junction voltage drop when forward biased. These features make MOSFET an extremely attractive power supply switching device.

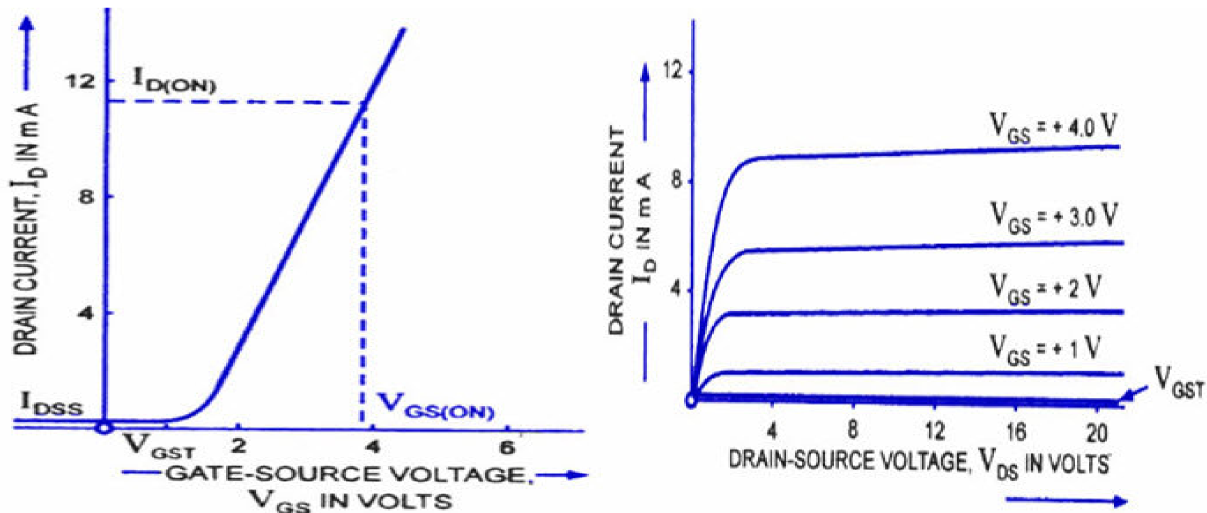



**Symbol** **Structure**

**Structure:**

- The construction of the power MOSFET is in V-configurations, as we can see in the following figure.
- Thus the device is also called as the V-MOSFET or V-FET.
- The V- the shape of power MOSFET is cut to penetrate from the device surface is almost to the N+ substrate to the N+, P, and N – layers.
- The N+ layer is the heavily doped layer with a low resistive material and the N- layer is a lightly doped layer with the high resistance region.
- Both the horizontal and the V cut surface are covered by the silicon dioxide dielectric layer and the insulated gate metal film is deposited on the SiO2 in the V shape.
- The source terminal contacts with the both N+ and P- layers through the SiO2 layer.
- The drain terminal of this device is N+.

**Characteristics:**




**Transfer & Drain characteristics**

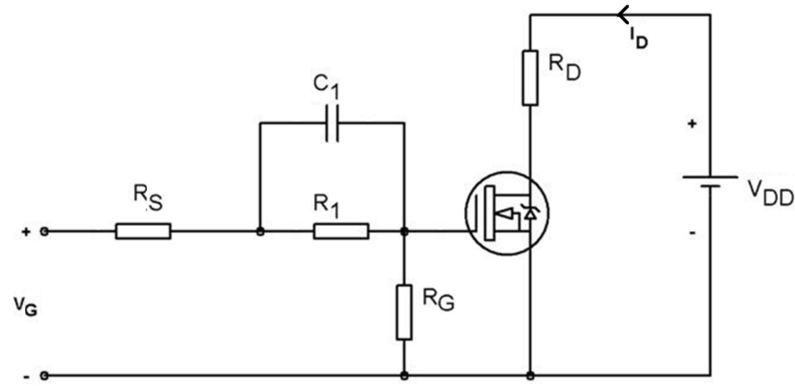
The above figures show the drain & transfer characteristics for the enhancement mode of N-channel power MOSFET is similar to the E-MOSFET. If there is an increase in the gate voltage then the channel resistance is reduced, therefore the drain current ID is increased. Hence the drain current ID is controlled by the gate voltage control. So that for a given level of VGS, ID is remaining constant through a wide range of VDS levels.

**Operation:**

- The V-MOSFET is an E-mode FET and there is no exists of the channel in between the drain & source till the gate is positive with respect to the source.
- If we consider the gate is positive with respect to the source, then there is a formation of the N-type channel which is close to the gate and it is in the case of the E-MOSFET.
- In the case of E-MOSFET, the N-type channel provides the vertical path for the charge carriers to flow between the drain and source terminals.
- If the VGS is zero or negative, then there is no channel of presence and the drain current is zero.

**Drive circuit:**

MOSFET's are voltage controlled devices and have very high input impedance. The gare draws a very small leakage current, on the order of nanoamperes.




The turn on time of an MOSFET depends on the charging timeof the input of gate capacitance. The turn on time can be reduced by connecting an RC circuit, as shown in figure to charge the gare capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is,

$$I_G = \frac{V_G}{R_S}$$

And the steady state value of gate voltage is

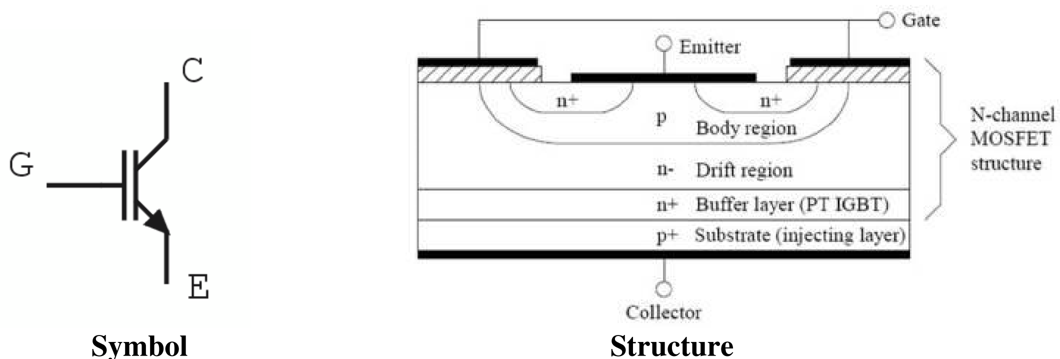
$$V_{GS} = \frac{R_G\, V_G}{R_S + R_1 + R_G}$$

Where $R_s$ is the internal resistance of gate drice source.

## ***IGBT***

A major limitation of Power MOSFET is the value of $R_{DS(ON)}$ increases as the voltage rating of the device is increased. This problem arises because the doping of the drain region of the MOSFET must be reduced as the voltage rating is increased. As the doping is reduced the conductivity of the device is decreased. The IGBT tries to overcome this limitation by using a forward biased P-N junction to inject minority carriers into this region so as to increase the conductivity.

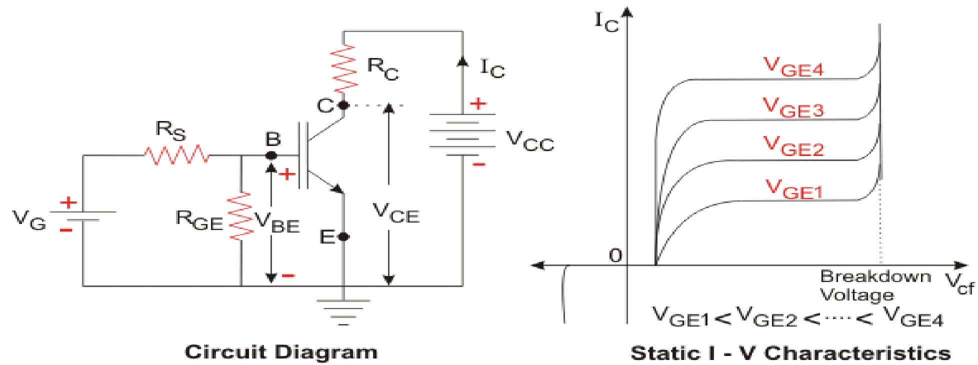
**Structure:**




**Symbol** **Structure**

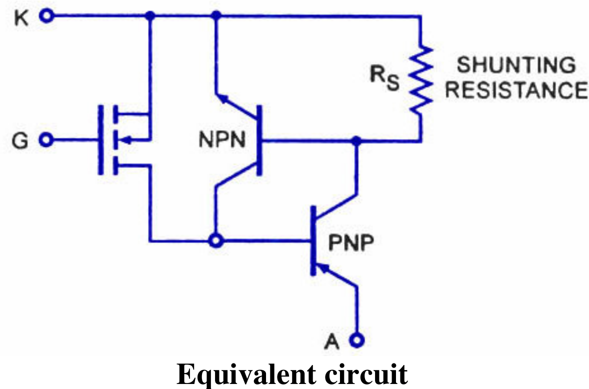
- The basic structure of an N-channel IGBT is as shown in figure above.
- Structurally, IGBT is almost identical to the MOSFET except for p+ injecting layer at the collector end.
- The n+ layer at the top is the source or emitter.
- The p+ layer at the bottom is the drain or collector.
- This layer is also referred to as injecting layer.
- The n+ layer separated from p+ layer by junction $J_1$ is called buffer layer.
- The IGBT's that are manufactured with this buffer layer are called punch through (PT) IGBT's.
- The IGBT's that are manufactured with buffer layer are called non-punch through (NPT) IGBT's.
- The n- layer is called drift region and the p layer adjoining this layer is the base region.

**Characteristics**




The graph is similar to that of a BJT except that the parameter which is kept constant for a plot is $V_{GE}$ because IGBT is a voltage controlled device unlike BJT which is a current controlled device. When the device is in OFF mode ($V_{CE}$ is positive and $V_{GE} < V_{GET}$) the reverse voltage is blocked by $J_2$ and when it is reverse biased, i.e. $V_{CE}$ is negative, $J_1$ blocks the voltage.

**Operation:**




**Equivalent circuit**

The IGBT is a four layer N-P-N-P device with an MOS-gated channel connecting the two N-type regions. In the normal mode of operation of an IGBT, a positive voltage is applied to the anode (A) relative to cathode (K). When the gate (G) is at zero potential with respect to K, no anode current $I_A$ flows for anode voltage $V_A$ below the breakdown level $V_{BF}$. When $V_A < _{VBF}$ and the gate voltage exceeds the threshold value $V_{GT}$, electrons pass into the N-region (base of the P-N-P transistor). These electrons lower the potential of the N-region, forward biasing the P+-N~ (substrate-epi-layer) junction, thereby causing holes to be injected from the P+ substrate into the N– epi-layer region. The excess electrons and holes modulate the conductivity of the high resistivity N-region, which dramatically reduces the on-resistance of the device. During normal operation, the shunting, resistor $R_S$ keeps the emitter current of the N-P-N transistor very low, which keeps α of N-P-N very low. However, for sufficiently large emitter current $I_A$ significant emitter injection may occur in the N-P-N transistor, causing α of N-P-N to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering emitter current $I_A$ below some holding value, as is typical of a thyristor.

***Comparison of power transistor, MOSFET and IGBT:***

| Device Characteristic | Power Bipolar | Power MOSFET | IGBT |
|---|---|---|---|
| Voltage Rating | High <1kV | High <1kV | Very High >1kV |
| Current Rating | High <500A | Low <200A | High >500A |
| Input Drive | Current, $h_{FE}$ 20-200 | Voltage, $V_{GS}$ 3-10V | Voltage, $V_{GE}$ 4-8V |
| Input Impedance | Low | High | High |
| Output Impedance | Low | Medium | Low |
| Switching Speed | Slow (uS) | Fast (nS) | Medium |
| Cost | Low | Medium | High |