{ Electronics }

20/July/2014

{Electronics}

Digital Electronics

* Boolean Algebra :-

It was developed by George Boolee by the help of switches [Relay circuits]. Boolean Algebra developed three theorems are called Basic theorem or Boolean Theorem.

1. NOT Theorem :-

$1 \longrightarrow 0$

$0 \longrightarrow 1$

$A \longrightarrow \bar{A}$

$\bar{A} \longrightarrow \bar{\bar{A}} = A$

2. AND Theorem (·) :-

$0 \cdot 0 = 0$	$0 \cdot A = 0$
$0 \cdot 1 = 0$	$1 \cdot A = A$
$1 \cdot 0 = 0$	$A \cdot A = A$
$1 \cdot 1 = 1$	$A \cdot \bar{A} = 0$

3. OR Theorem (+) :-

$0 + 0 = 0$	$0 + A = A$
$0 + 1 = 1$	$1 + A = 1$
$1 + 0 = 1$	$A + A = A$
$1 + 1 = 1$	$A + \bar{A} = 1$

* Distributive Theorem :-

$$U = (A+B).(A+C)$$
$$= A.A + A.C + A.B + B.C$$
$$= A + AC + AB + BC$$
$$= A[1 + C + B] + BC \quad = A.1 + BC$$

$$\boxed{U = A + BC} \quad \text{---} \quad (*)$$

Short Trick :-

When two brackets are available and first term of both brackets are same the we apply distributive theorem like this-

$$U = (A+B)(A+C)$$

$$U = A.A + B.C$$

$$\boxed{U = A + BC} \quad \text{---} \quad (**)$$

Ques For the given expression find the minimise equation.

$$y = (A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})$$

Soln

$$y = (A.A + B.\bar{B})(\bar{A}.\bar{A} + B.\bar{B})$$
$$y = (A + 0)(\bar{A} + 0)$$
$$= A.\bar{A} \quad = 0 \quad \underline{\text{Ans}}$$

Ques For the given expression find the minimise eqn.

$$y = (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)$$

Sol^{n} $y = (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)$

Let $A+B = x$

So,

$y = (x+C)(x+\bar{C})(A+\bar{B}+C)$

$y = (x.x + C\bar{C})(A+\bar{B}+C)$

$y = x(A+\bar{B}+C)$

$y = (A+B)(A+\bar{B}+C)$

Again let $\bar{B}+C = y$

So

$y = (A+B)(A+y)$

$y = A.A + B.y$

$y = A + B.[\bar{B}+C]$

$y = A + B\bar{B} + BC$

$\boxed{y = A+BC}$ Ans

* Short Trick -

$(A+B)(A+C) = A+BC$

$\underset{1}{A} + \underset{2.3}{BC} = (A+B)(A+C)$

$(1 + 2.3) = (1+2)(1+3)$

Qus Find the minimise expression of the given eq^{n}.

$y = B + \bar{B}C$

Sol^{n} $y = \underset{1}{B} + \underset{2.3}{\bar{B}C}$

$y = (B+\bar{B}C) = (B+\bar{B})(B+C)$

$y = B+C$ Ans

Ques Find the minimise equation of the given expression.

$$y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

Sol^n

$$y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$
$$= \bar{A}BC + A\bar{B}C + AB(\bar{C}+C) \quad \{\because (C+\bar{C}) = 1\}$$
$$= \bar{A}BC + A\bar{B}C + AB$$
$$= \bar{A}BC + A[B + \bar{B}C]$$
$$= \bar{A}BC + A(B+\bar{B})(B+C)$$
$$= \bar{A}BC + A(B+C)$$
$$= \bar{A}BC + AB + AC$$
$$= B(\bar{A}C + A) + AC$$
$$= B(A + \bar{A}C) + AC$$
$$= B(\bar{A}+A)(A+C) + AC$$
$$= B(A+C) + AC$$
$$y = AB + BC + AC \quad \underline{\text{Ans}}$$

Ques Find the minimise expression of the given equation. $y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$

Sol^n

$$y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$$
$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + BC(\bar{A}+A)$$
$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + BC$$
$$= \bar{A}\bar{B}C + B[C + \bar{A}\bar{C}]$$
$$= \bar{A}\bar{B}C + B(C+\bar{A})(C+\bar{C})$$
$$= \bar{A}\bar{B}C + B(C+\bar{A})$$
$$= \bar{A}\bar{B}C + BC + \bar{A}B$$
$$= C(\bar{A}\bar{B} + B) + \bar{A}B$$
$$= C(B+\bar{A}) + \bar{A}B$$
$$\boxed{y = \bar{A}C + BC + \bar{A}B} \quad \underline{\text{Ans}}$$

* Sum of Product (SOP) And Product of Sum (POS):-

1. Sum of Product (SOP):-

It is used variabl output of the digital circuit is 1. (high).

Example :- i/p → o/p

5 → 1

101 → 1

(A B̄ C)

9 → 1

1001 → 1

(A B̄ C̄ D)

2. Product of Sum (POS):-

It is used variable output of the digital circuit is zero.

e.g.:-

i/p → o/p

5 → 0

101 → 0

(Ā + B + C̄)

i/p → o/p

9 → 0

1001 → 0

(Ā + B + C + D̄)

Qus from the given table find the output minimise expression by using SOP.

A	B	y
0	0	1
0	1	0
1	0	1
1	1	1

Sol: ∵ SOP is written for the high output.

So

A	B	Y	
0	0	1	$\rightarrow \bar{A}\bar{B}$
0	1	0	
1	0	1	$\rightarrow A\bar{B}$
1	1	1	$\rightarrow AB$

$$Y_{SOP} = (\bar{A}.\bar{B}) + (A.\bar{B}) + (A.B)$$
$$\Rightarrow \bar{B}(\bar{A}+A) + AB$$
$$= \bar{B} + AB$$
$$= (\bar{B}+A)(\bar{B}+B)$$
$$\boxed{Y_{SOP} = A+\bar{B}} \quad \text{---- (I)}$$

for POS :-

Since POS written for the low output

So,

A	B	Y	
0	0	1	
0	1	0	$\rightarrow \bar{A}+\bar{B}$
1	0	1	
1	1	ϕ	

So,
$$\boxed{Y_{POS} = A+\bar{B}} \quad \text{---- (II)}$$

from equation (I) and (II)

$$\boxed{SOP_{exp.} = POS_{exp.}}$$

Ques from the given truth table find the minimise expression of output.

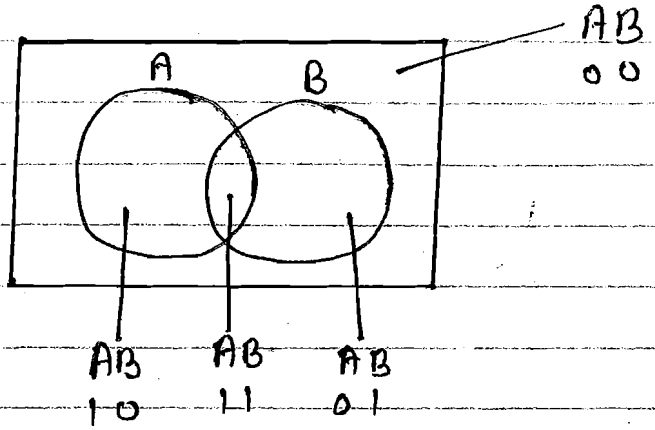
A B C	Y	
0 0 0	0	
0 0 1	0	
0 1 0	0	
0 1 1	1	$\longrightarrow \bar{A}BC$
1 0 0	0	
1 0 1	0	
1 1 0	1	$\longrightarrow AB\bar{C}$
1 1 1	0	

Sol^n

$$Y_{SOP} = \bar{A}BC + AB\bar{C}$$

$$\boxed{Y_{SOP} = B(\bar{A}C + A\bar{C})}$$ Ans

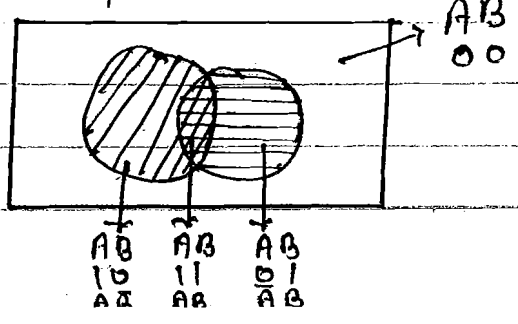
* Logical Venn Diagram :-



Ques From the given diagram find the minimise expression for the shaded regim by using SOP.

Sol^n

$$Y_{SOP} = A\bar{B} + AB + \bar{A}\bar{B}$$
$$= A(\bar{B} + B) + \bar{A}\bar{B}$$
$$= \underset{1}{A} + \underset{2.3}{\bar{A}\bar{B}}$$



$= (A + \bar{A})(A + B)$

$\boxed{Y_{SOP} = (A + B)}$ Ans $\quad \{ \because (A + \bar{A}) = 1 \}$

Ques From the given diagram find the output minimise expression for the shaded region by using SOP.

Soln

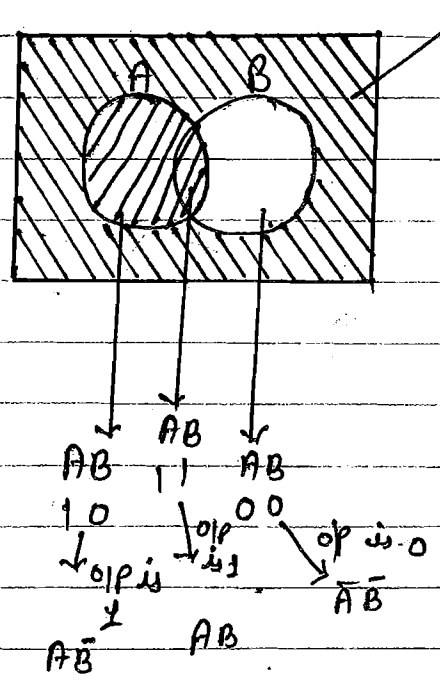
$Y_{SOP} = A\bar{B} + AB + \bar{A}\bar{B}$

$= A(\bar{B} + B) + \bar{A}\bar{B}$

$= \underset{1}{A} + \underset{2.3}{\bar{A}\bar{B}}$

$= (A + \bar{A})(A + \bar{B})$

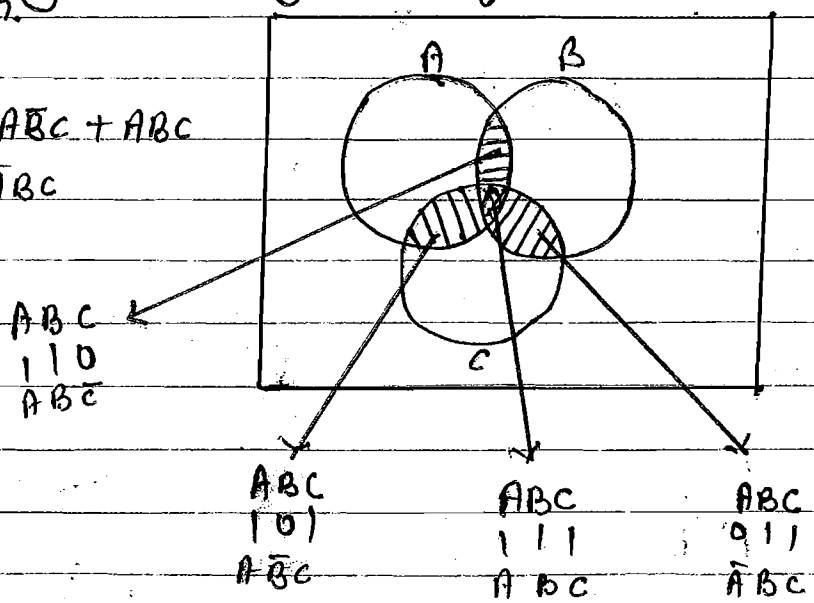
$\boxed{Y_{SOP} = A + \bar{B}}$ Ans



Ques For the given diagram find the minimise expression.

Soln:-

$Y_{SOP} = AB\bar{C} + A\bar{B}C + ABC + \bar{A}BC$



So $Y_{SOP} = AB\bar{C} + A\bar{B}C + BC(A + \bar{A})$

$$Y_{sop} = AB\bar{C} + A\bar{B}C + BC$$

$$= AB\bar{C} + C(B + A\bar{B})$$
(1 + 2.3)

$$= AB\bar{C} + C[(B+A)(B+\bar{B})]$$

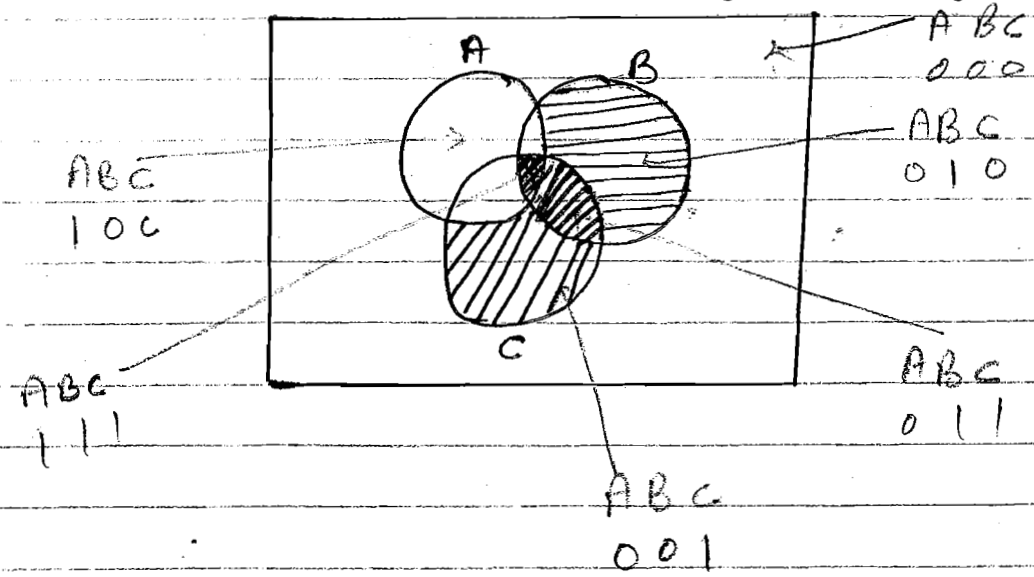
$$= AB\bar{C} + BC + AC$$

$$= B(C + A\bar{C}) + AC$$
(1 + 2.3)

$$= B[(C+A)(C+\bar{C})] + AC$$

$$\boxed{Y_{sop} = BC + AB + AC}$$ Ans

Ques Find the minimise expression for the given diagram



Note :-

1. Each term taken from the truth table for implimentation of SOP eqprassion is called Minterm.
   Minterm must include every variable.
   Minterm has dot (·) sign in between.
2. Each term taken from the truth table for the implimentation of POS expression it is called as Maxterm.
   Maxterm will have +ve sign in between and include every variable.

* Mathematical Representation of SOP and POS :-

for n variable the value assigned to the maximum number of 1's is given by $(2^n - 1)$.

SOP :-

Minterm = $\sum m(0, 2, 3)$

	A	B	Y
0 ←	0	0	1
1 ←	0	1	0 →
2 ←	1	0	1
3 ←	1	1	1

$(2^n - 1)$ where n is the no. of variable {here 2}

POS :-

Maxterm = $\prod M(1)$

- SOP is always equal to POS.

Ques For the given function $f(A,B,C) = \sum m(0,2,3,6)$ find the equivalent POS.

Soln

Here number of variable = 3

So

$2^3 - 1 = 8 - 1 = 7$

Equivalent POS is -

$= \pi M(1,4,5,7)$

Ans

Ques Find the equivalent POS of $f(A,B,C,D) = \sum m(0,2,3,6,7,11,13)$.

Soln Here number of variable = 4

So $2^4 - 1 = 15$

Equivalent POS :-

$= \pi M(1,4,5,8,9,10,12,14,15)$.

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Note :-

Representation of SOP or POS without reducing the number of variable is called Canonical form of representation.

Ques For the given expression $f(A,B,C) = A + \bar{B}C$ represents minterm of canonical form of SOP. And Identify no. of minterms presents.

Soln :-

$f(A,B,C) = A + \bar{B}C$

$$f(A,B,C) = A.1 + \bar{B}C.1$$
$$= A[B+\bar{B}][C+\bar{C}] + \bar{B}C[A+\bar{A}]$$
$$= A[BC + B\bar{C} + \bar{B}C + \bar{B}\bar{C}] + A\bar{B}C + \bar{A}\bar{B}C$$
$$= ABC + AB\bar{C} + \underline{A\bar{B}C} + A\bar{B}\bar{C} + \underline{A\bar{B}C} + \bar{A}\bar{B}C$$
$$f(A,B,C)_{sop} = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$$

Ans

There is 5 minterm.

II^nd Method :-

A	B	C	
0	0	0	
0	0	1	o/p → 1
0	1	0	
0	1	1	
1	0	0	o/p → 1
1	0	1	o/p → 1
1	1	0	o/p → 1
1	1	1	o/p → 1

$$\boxed{y_{sop} = ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C}$$

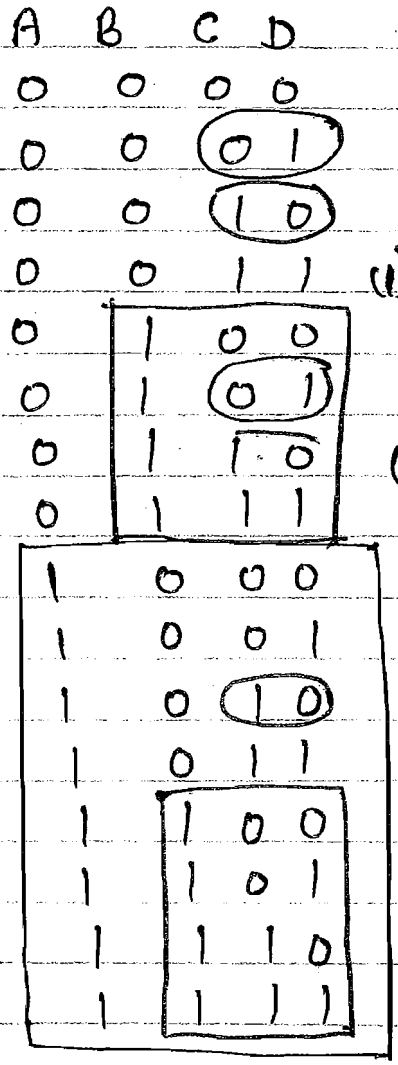
Ques For the given function find the number of minterms

(i) $f(A,B,C,D) = A + \bar{C}D$

(ii) $f(A,B,C,D) = B + C\bar{D}$

Soln:-

$$f(A,B,C,D) = A + \bar{C}.D$$



So no. of minterm = 10

(i) $f(A,B,C,D) = A + \bar{C}D$ = 10 minterm

(ii) $f(A,B,C,D) = B + C\bar{D}$ = 10 minterm

* Note :-

- for a single variable we have 4 types of truth tables so we have 4 types of Boolean expression.

e.g.

A	Y_1	Y_2	Y_3	Y_4
0	0	0	1	1
1	0	1	0	1

$2^{2^1} = 4$.

- So for n no. of variables no. of possible truth table or Boolean expression or switching expression is given by - = 2^{2^n}

Ques for 4-variable no. of possible boolean expression is given by -

Soln $2^{2^4} = 2^{16} = 2^{10} \times 2^6$

$= 1024 \times 64$

$= 65536$ Ans.

* Positive Logic and Negative Logic :-

- If higher values are assigned to higher voltages and lower values are assigned to lower voltages such a logic is called +ve logic.

e.g:-

logic 0 ——— 0V

logic 1 ——— +5V

- If the values are reverse the resultant logic will be negative logic.

e.g. -

logic 0 ——— +5V

logic 1 ——— 0V

The process of conversion of +ve logic to negative logic or vice-versa is called as "duality."

e.g:-

AND → +ve logic

A	B	Y (A.B)
0	0	0
0	1	0
1	0	0
1	1	1

OR → -ve logic

A	B	Y (A+B)
1	1	1
1	0	1
0	1	1
0	0	0

small → 10 = 1 (big)

0 1 = 1

big small

* Important Point for duality :-

(i) $0 \rightleftharpoons 1$

(ii) $\cdot \rightleftharpoons +$

(iii) Variable as it is.

Examples :-

$$A \cdot B \xrightarrow{\text{duality}} A + B$$

$$A + B \longrightarrow A \cdot B$$

$$\overline{A \cdot B} \longrightarrow \overline{A + B}$$

$$\overline{A + B} \longrightarrow \overline{A \cdot B}$$

$$(\bar{A}B + A\bar{B}) \longrightarrow (\bar{A} + B) \cdot (A + \bar{B})$$

$$= (\bar{A}A + \bar{A}\bar{B} + AB + B\bar{B})$$

$$= (\bar{A}\bar{B} + AB) \quad \{\because A\bar{A} = 0,\ B\bar{B} = 0\}$$

Ques Find the dual of $y = AB + CD$

Sol? $\boxed{y_D = (A + B) \cdot (C + D)}$ Ans

$y_{DD} = AB + CD = y$

Ques Find the dual of $y = AB + BC + AC$.

Sol?

$$y_D = (A + B) \cdot (B + C) \cdot (A + C)$$

$$= (B \cdot B + A \cdot C) \cdot (A + C)$$

$$= (B + AC) \cdot (A + C)$$

$$= A \cdot B + B \cdot C + A \cdot AC + A \cdot CC$$

$$= A \cdot B + B \cdot C + A \cdot C + A \cdot C$$

$\boxed{y_D = A \cdot B + B \cdot C + A \cdot C}$ Ans

→ self dual.

• If single time dual results same expression then it is called self dual expression.

Ques Find the dual of given expression -
$Y = (A+B)(B+C)(A+C)$.

Soln
$$Y = (A+B).(B+C).(A+C)$$

$$\boxed{Y_D = AB + BC + AC} \quad \text{---- (1)}$$

Since eqn (1) is self dual so

$Y = (A+B)(B+C)(A+C)$ is also self dual expression.

Ques Check wheather self dual or not ?
$Y = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

Soln
$$Y_D = (\bar{A}+\bar{B}).(\bar{B}+\bar{C}).(\bar{A}+\bar{C})$$
$$= (\bar{B}+\bar{A}).(\bar{B}+\bar{C}).(\bar{A}+\bar{C})$$
$$= (\bar{B}.\bar{B} + \bar{A}\bar{C}).(\bar{A}+\bar{C})$$
$$= (\bar{B} + \bar{A}\bar{C}).(\bar{A}+\bar{C})$$
$$= \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}.\bar{A}\bar{C} + \bar{A}.\bar{C}.\bar{C}$$
$$\boxed{Y_D = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}}$$

Self dual expression.

Q. $Y = (\bar{A}+\bar{B}).(\bar{B}+\bar{C}).(\bar{A}+\bar{C})$ check duality.

Soln It is also a self dual.

Current prefers resistance less path.

Note:-

- Duality of single variable:-

$A \xrightarrow{D} A$ (self dual)

$\bar{A} \xrightarrow{D} \bar{A}$ (self dual)

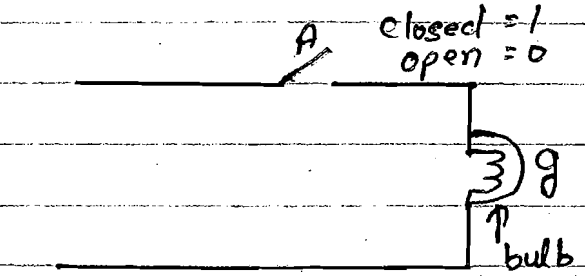
$2^{2^{1-1}} = 2^{2^0} = 2^1 = 2$ self dual expressions

- for n ~~nuber~~ number of variable number of possible self dual expression is given by

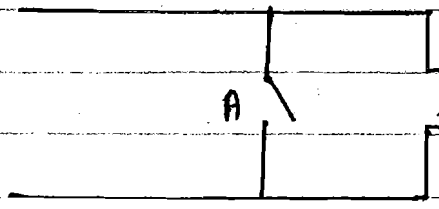
$= 2^{2^{n-1}}$.

{ SWITCHING CIRCUITS }

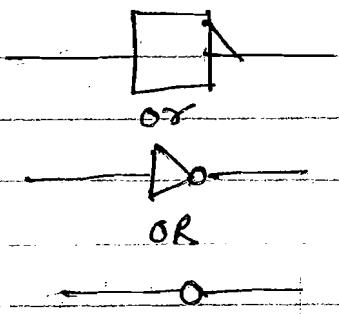
The circuit produces same input same output condition is called Buffer.
Common Collector configuration is also called Buffer.

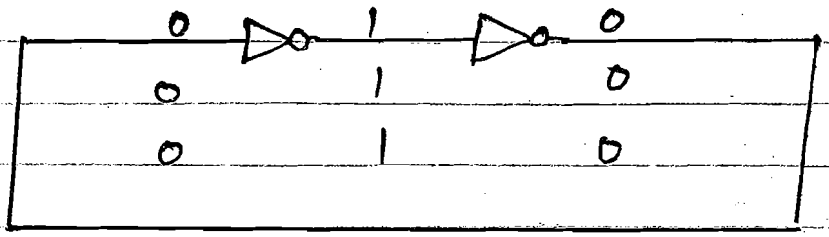


A	Y
0	0
1	1



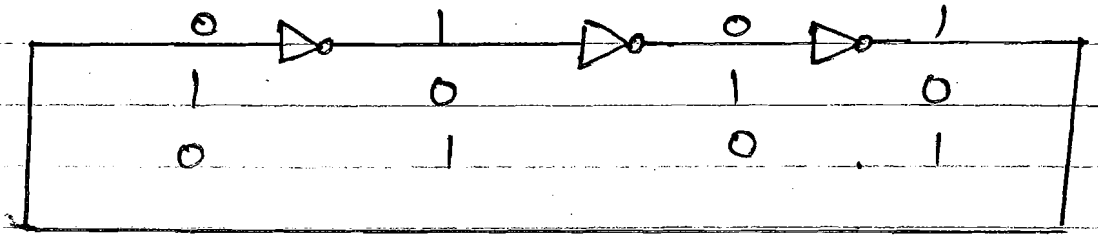
A	Y
0	1
1	0



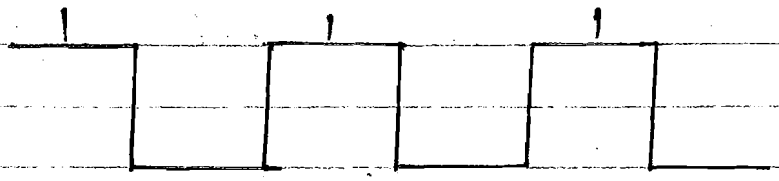


Bistable Multivibrator.

⇒ Even numbers of NOT gate with feedback is called as Bistable Multivibrator.

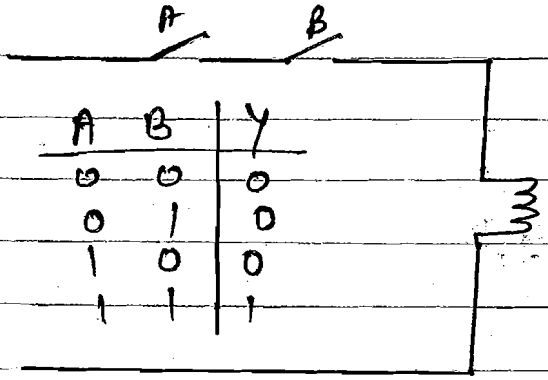


Astable Multivibrator. (Not stable



The output waveform of Astable multivibrator is square wave.

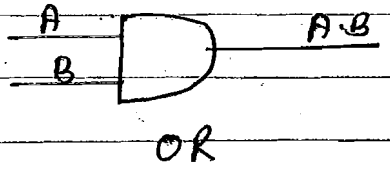
⇒ Odd numbers of NOT gate combination with feedback is called Astable Multivibrator.



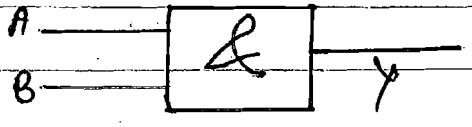
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate.

Equivalent Symbols:-

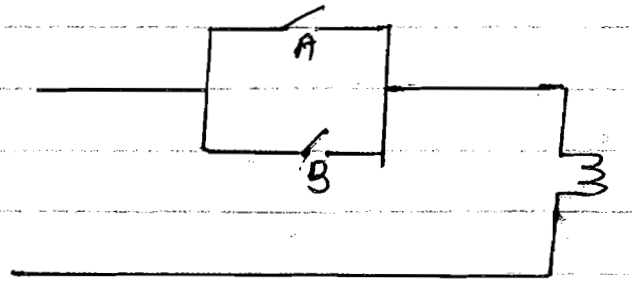


OR



Input Condition :- If any i/p = 0 then o/p = 0.

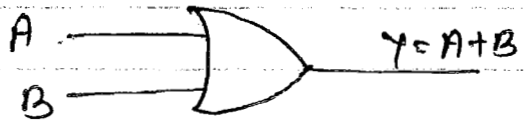
In AND Gate Switches are in series.



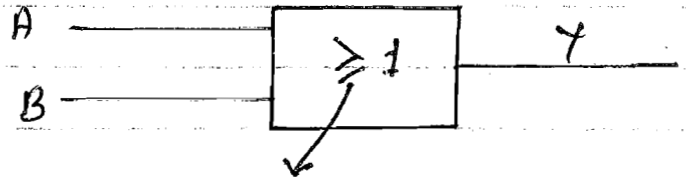
OR Gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Equivalant Circuit Symbols:-



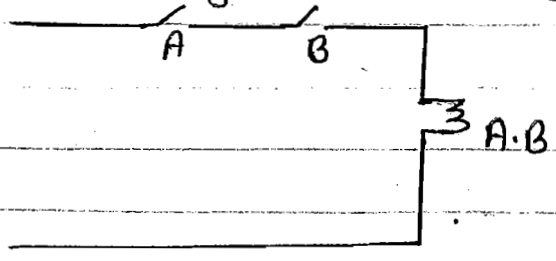
Rectangular form of representation:-

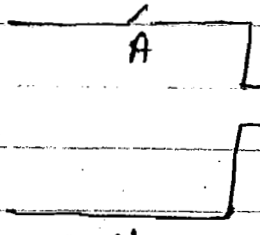


Means one or more than one input is 1 then output is 1.

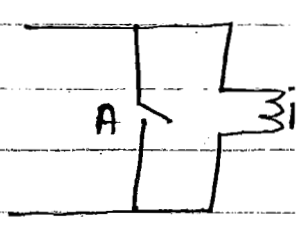
Universal Gates

* NAND and NOR gates are universal because any digital circuit can be implimented by using these gates.

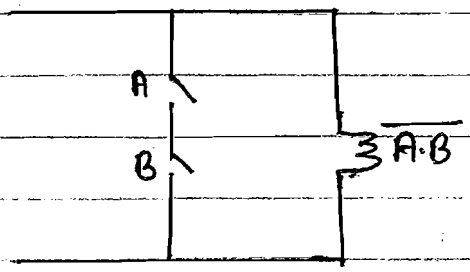


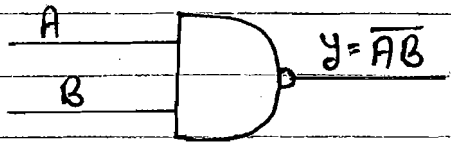


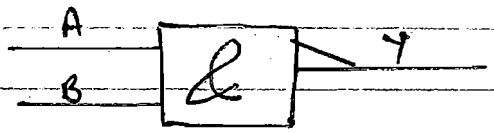
Buffer



NOT





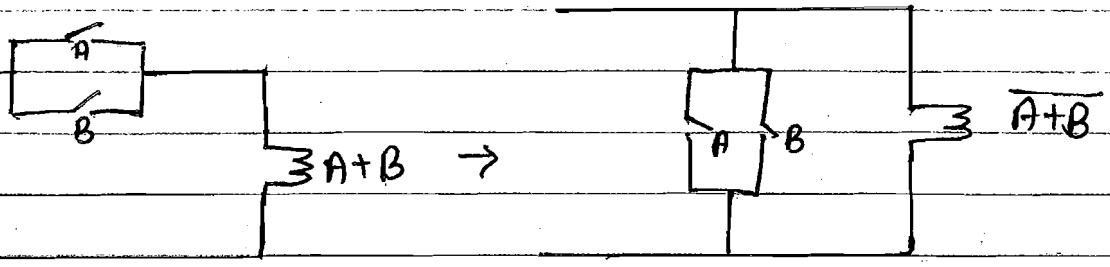


NAND Gate

A	B	A·B	$\overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

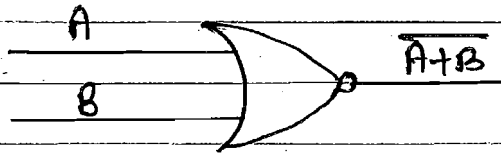
When any i/p is zero then o/p = 1.

* NOR :-

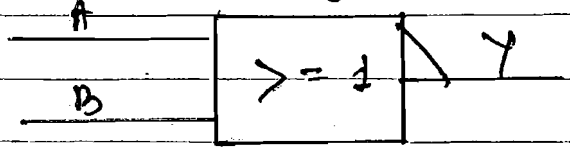


NOR

Equivalent Circuit Symbol :-



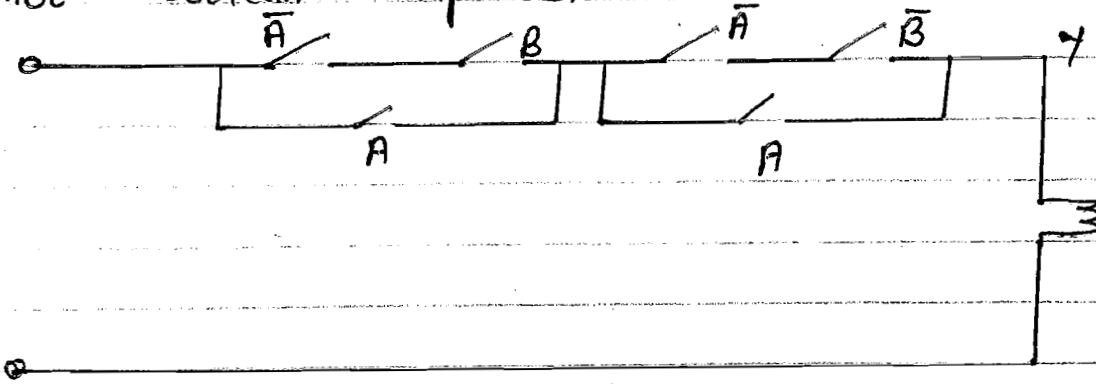
Equivalent rectangular representation :-



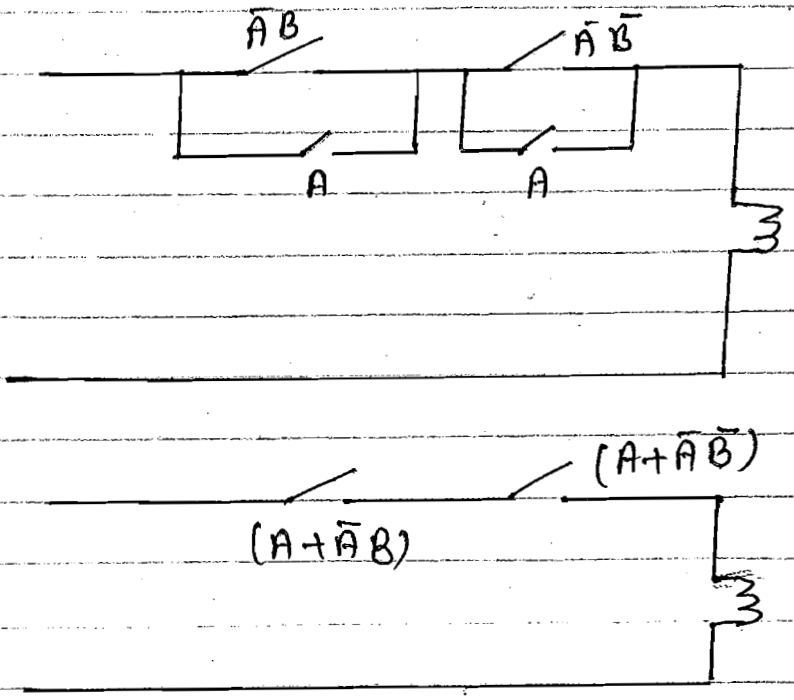
A	B	A + B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

If any i/p = 1 then o/p = 0

Ques For the given switch diagram find the o/p minimise Boolean expression.



Soln:



$Y = \underset{1+2.3}{(A+\bar{A}B)} \underset{1+2.3}{(A+\bar{A}\bar{B})}$

$= (A+B)(A+\bar{B})$

$= A.A + B.\bar{B}$

$= A + 0$

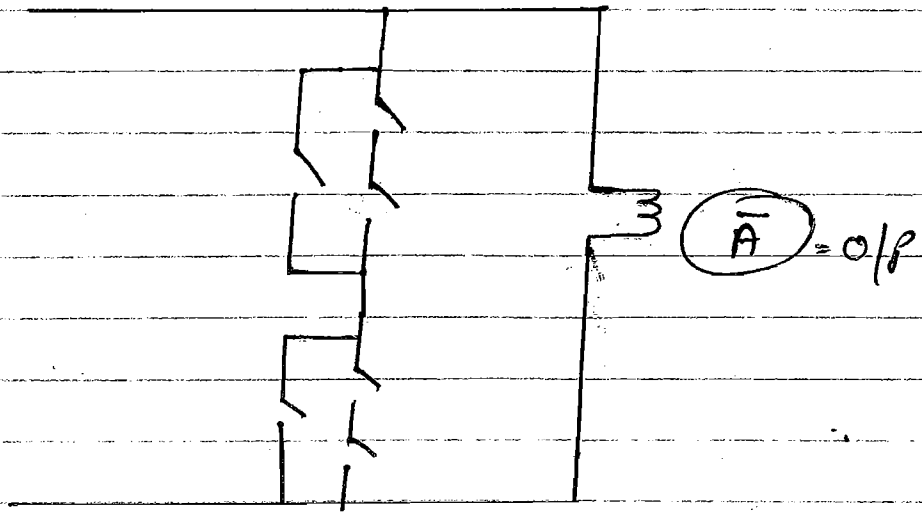
$= A$ Ans

o/p minimise expression.

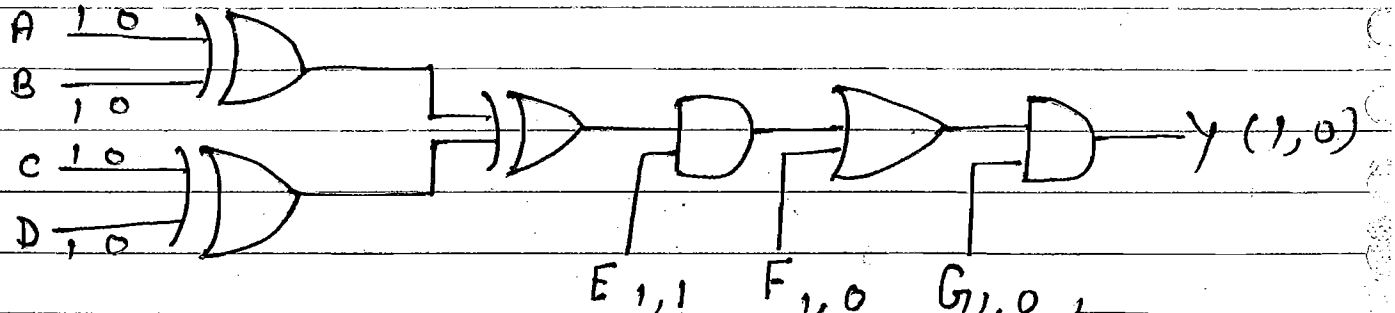
contain Bar. But when switches are in parallel with bulb then o/p contain Bar.

Ques For the given switch diagram find the o/p minimise expression.

Soln



Ques Calculate output Y for two different cases for which given circuit shown -



Soln Case I :-

$A = B = C = D = E = F = G = 1$

So o/p = 1

Case II :-

$A = B = C = D = 0$, $E = 1$, $F = G = 0$

So o/p = 0

* Arithmatic Circuit Gate :-

Ex-OR gate and Ex-NOR are arithmatic circuit gate because most of the arithmatic circuits utilises Ex-OR & Ex-NOR operations.

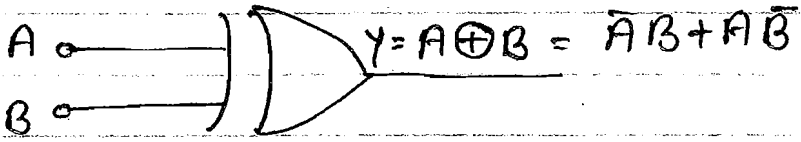
Ex-OR :-

Ex-OR = Exclusive OR = X-OR

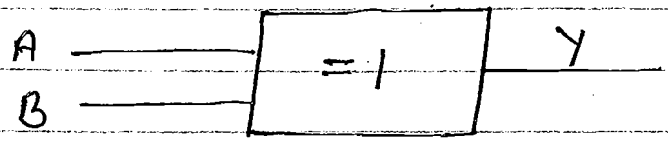
Symbol :-

⊕

- Circuit Symbol :-



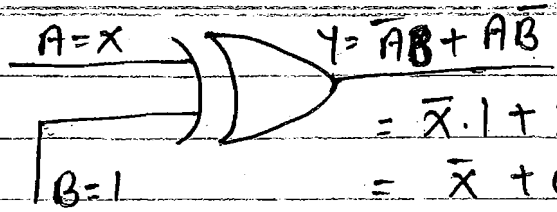
Equivalent circuit symbol of Rectangular ? :-



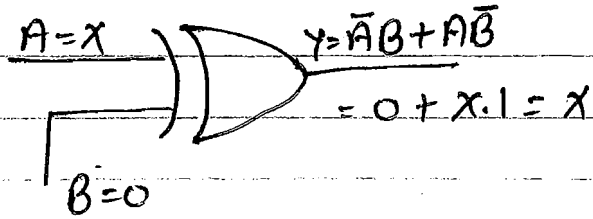
The disadvantage of X-OR gate is only two input X-OR operations are possible.

A	B	$Y = \bar{A}B + A\bar{B}$
0	0	0
0	1	1
1	0	1
1	1	0

for same input, output = 0, for different input output = 1.

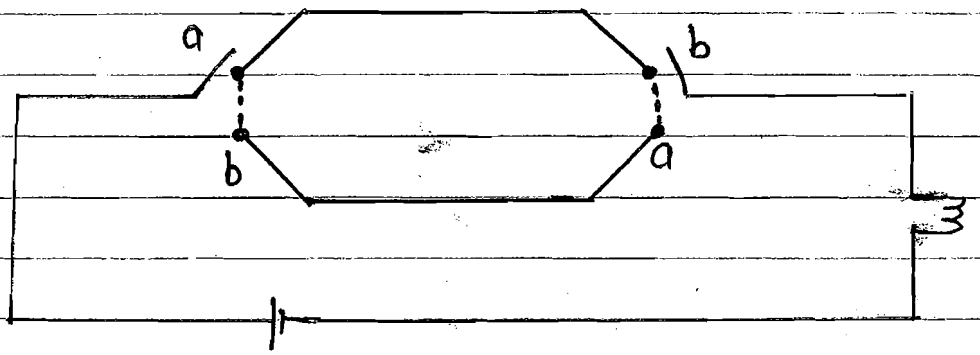


If one input of X-OR gate is 1. then output is complement of another input.

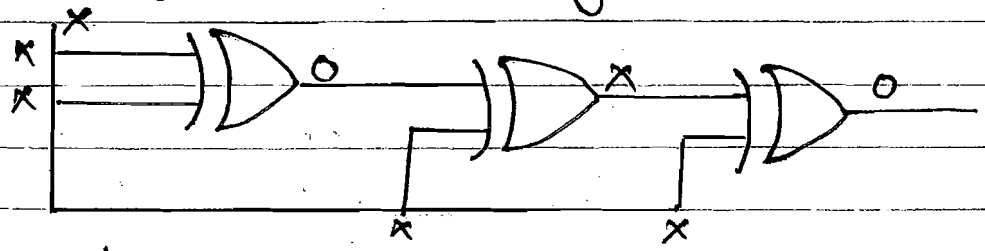


If any one input is zero then output is another input.

* Switching Diagram :-



Ques for the given circuit diagram determine the output Y.



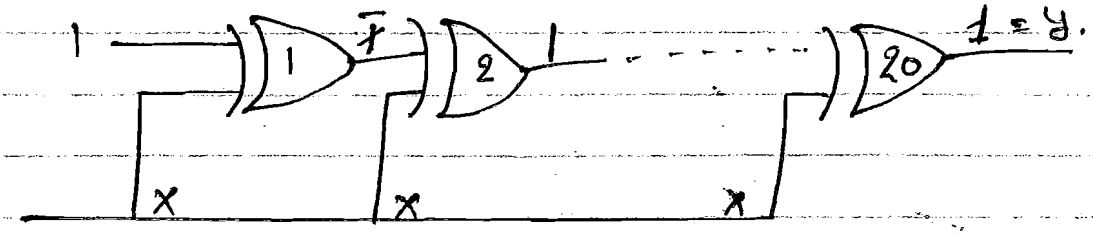
Ans So o/p y=0.

$\overline{A \cdot B} = \bar{A} + \bar{B}$

$\overline{A + B} = \bar{A} \cdot \bar{B}$ → Demorgan theorem.

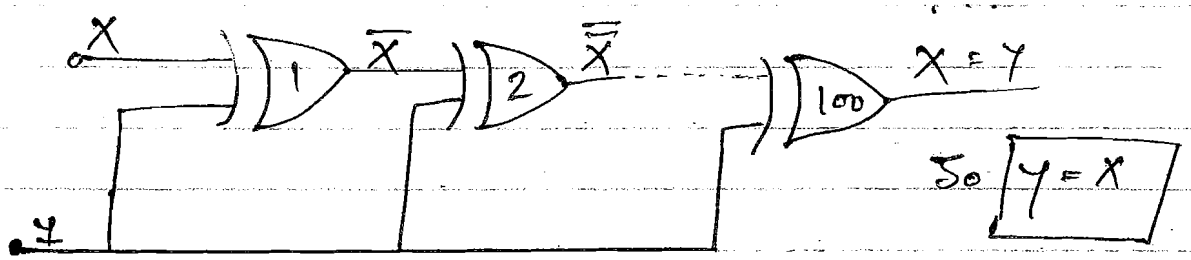
Ques for the given circuit diagram determine Y.

(a) x (b) $\bar{x}$ (c) 1 [✓] (d) 0



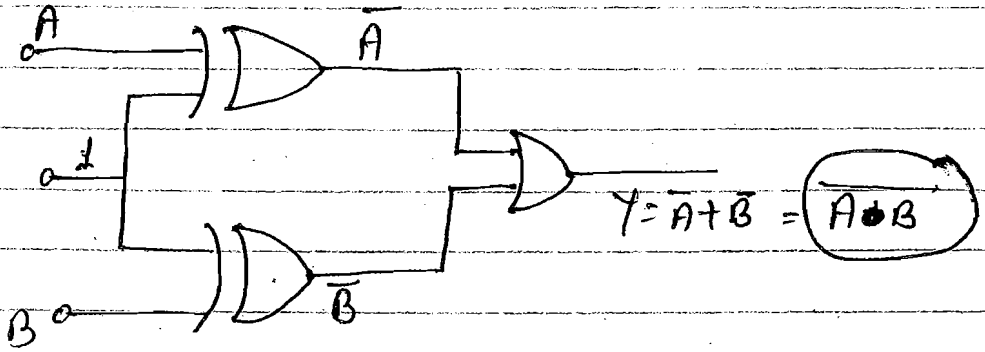
Ques for the given circuit diagram.

(a) x [~] b = $\bar{x}$ (c) 1 (d) 0



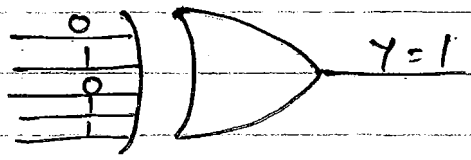
Ques for the given circuit diagram calculate o/p Y.

(a) $\overline{A+B}$ [✓] (b) $\overline{A \cdot B}$ [~] (c) $\bar{A} \cdot \bar{B}$ (d) $\bar{A} \cdot B$



A	B	$\bar{A} + \bar{B}$	$\overline{A \cdot B}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

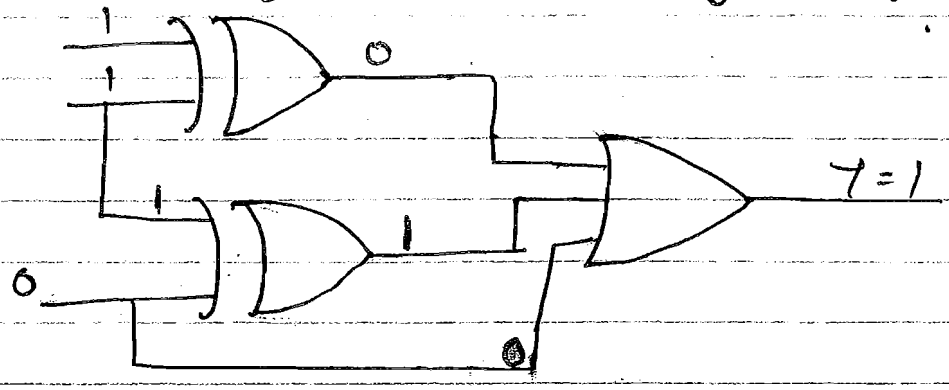
- Ex-OR is also called as odd function of 1. i.e. whenever odd numbers of i/ps are high then output = 1.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Ques for the given circuit diagram find Y = ?

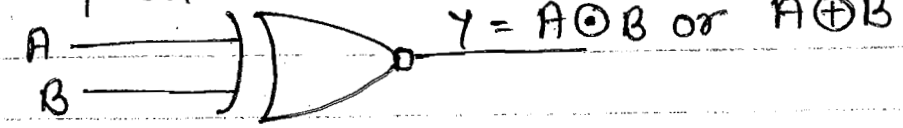
Ans.



So o/p Y = 1 Ans

* Ex- NOR Gate :-

Circuit Symbol :-



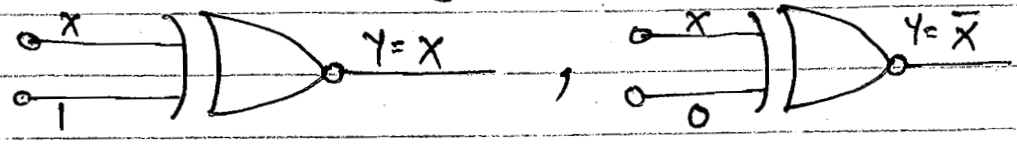
$$\overline{A \oplus B} = \overline{\bar{A}B + A\bar{B}}$$
$$= \bar{\bar{A}}\bar{B} + \bar{A}\bar{\bar{B}}$$
$$= AB + \bar{A}\bar{B}$$
$$= (A + \bar{B})(\bar{A} + B)$$
$$= A\bar{A} + AB + \bar{A}\bar{B} + \bar{B}B$$
$$= AB + \bar{A}\bar{B}$$

$$\boxed{\overline{A \oplus B} = A \odot B}$$

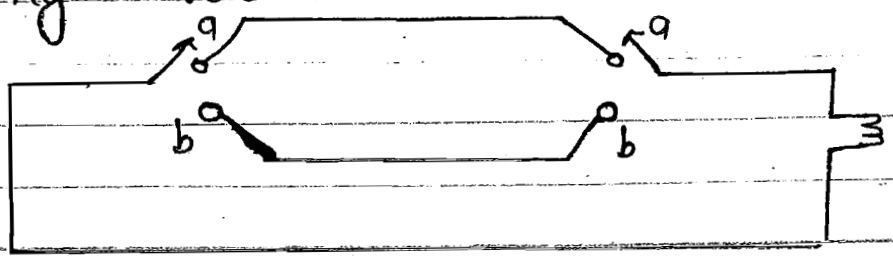
Truth Table :-

A	B	$A \oplus B$	$\overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Ex-NOR is also called equality detector. It is also called as coinsidence circuit or coinsidence gate.



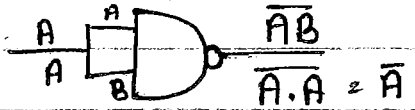
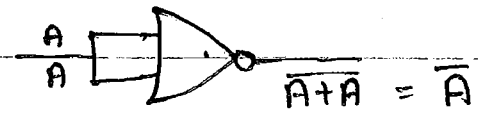
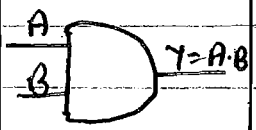
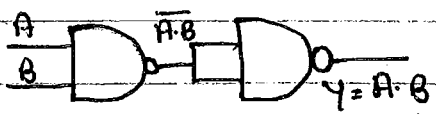
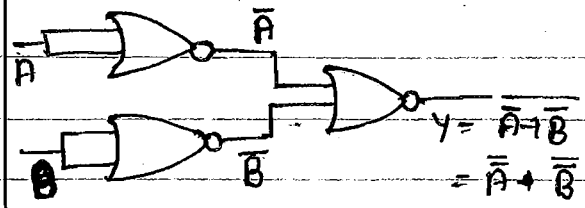
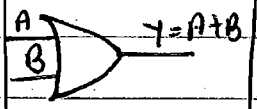
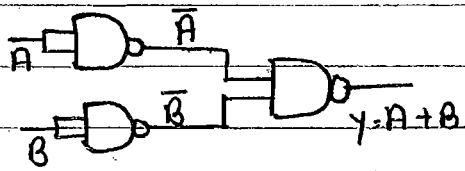
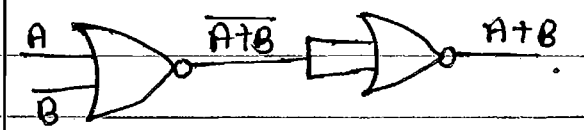
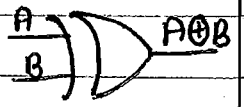
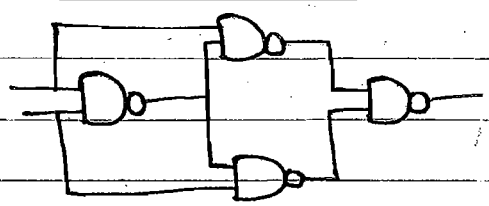
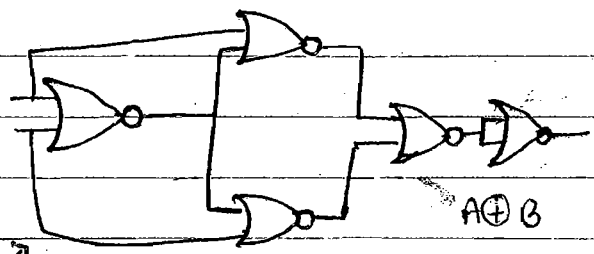
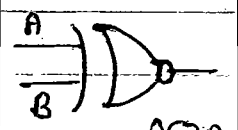
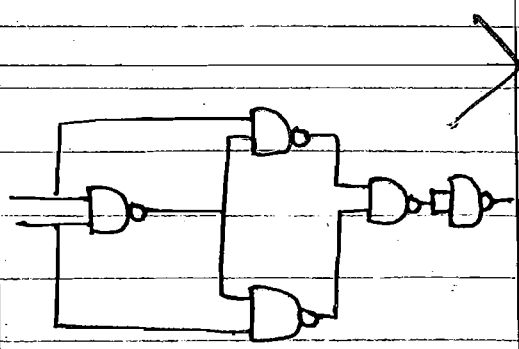
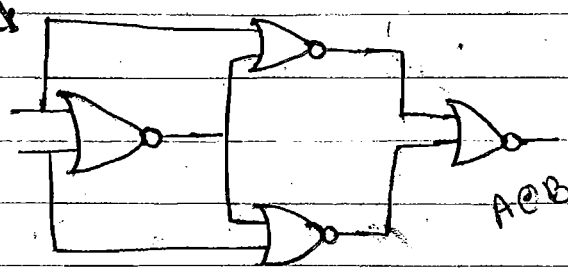
* Switching Circuit :-



1 0	0 1 □	⇒ 0
1 0	1 0 □	1, 1, 0, 0

* For the stairs case application the logic circuit is used for the control of bulb is X-OR (if X-OR is not available then X-NOR).

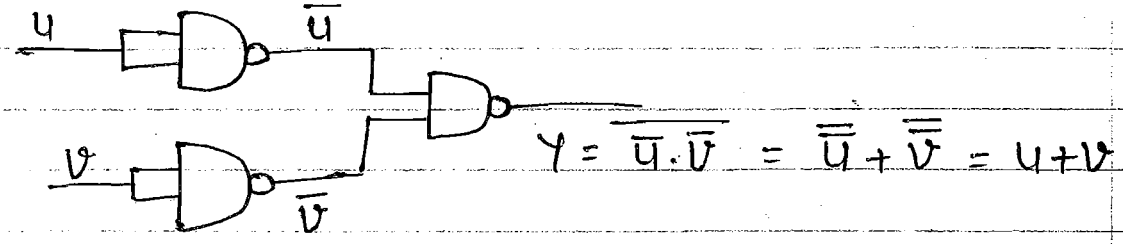
Universal Gates

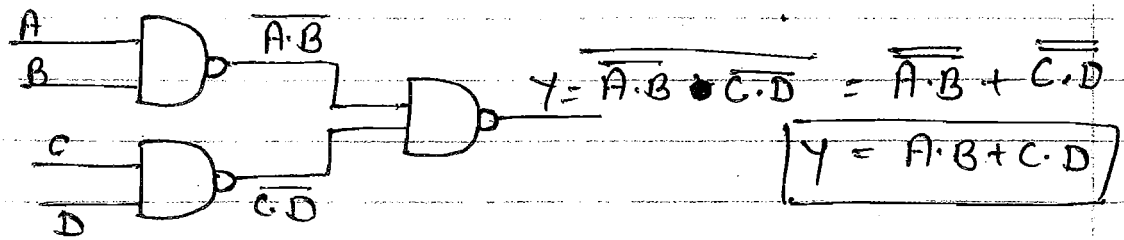
Gates	NAND	NOR
		
		
		
		
		

Qus Impliment $Y = AB + CD$ by using minimum number of two input NAND gate.

Sol^n

$$Y = \underbrace{AB}_{U} + \underbrace{CD}_{V}$$

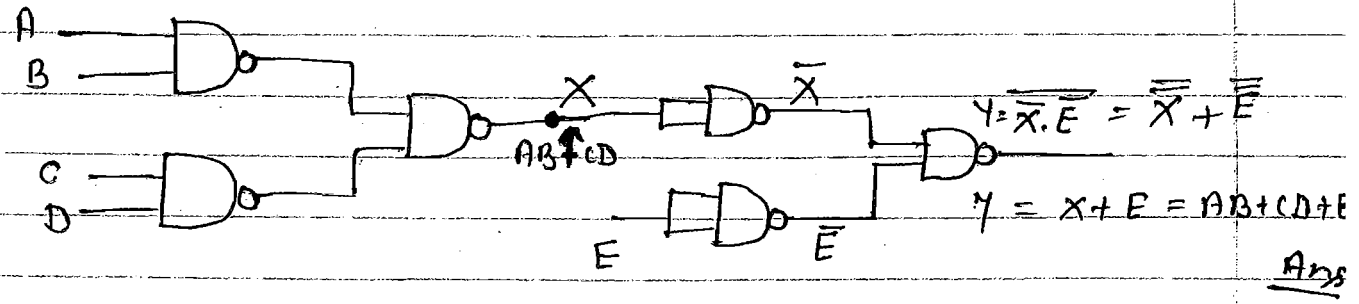




Qus Impliment $Y = AB + CD + E$

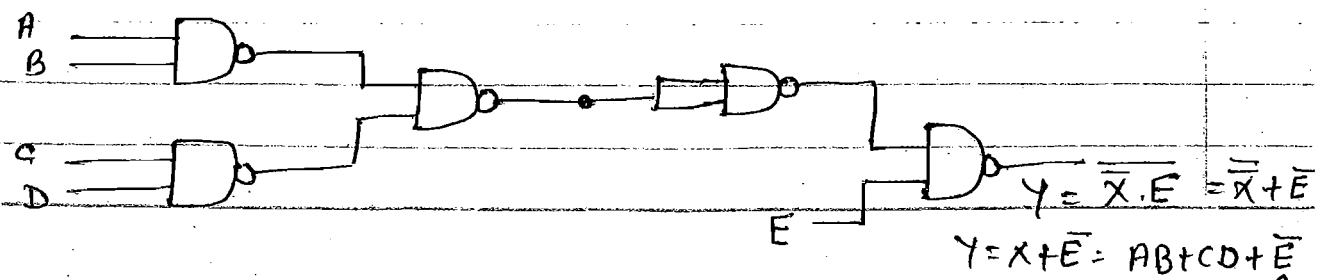
Sol^n

$$Y = \underbrace{AB + CD}_{X} + E$$



Ans

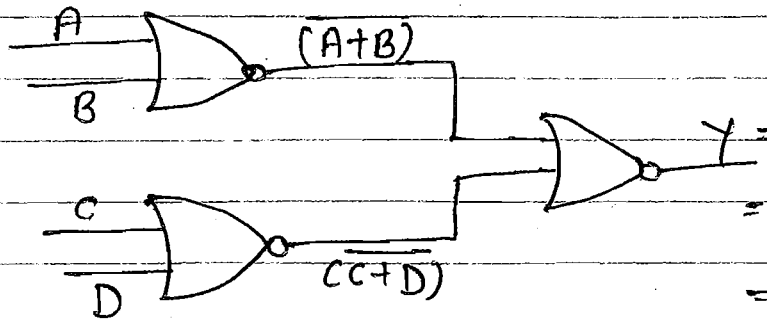
Qus Impliment $Y = AB + CD + \overline{E}$



An

Ques For the given expression $Y = (A+B).(C+D)$ by using minimum number of two input NOR gates.

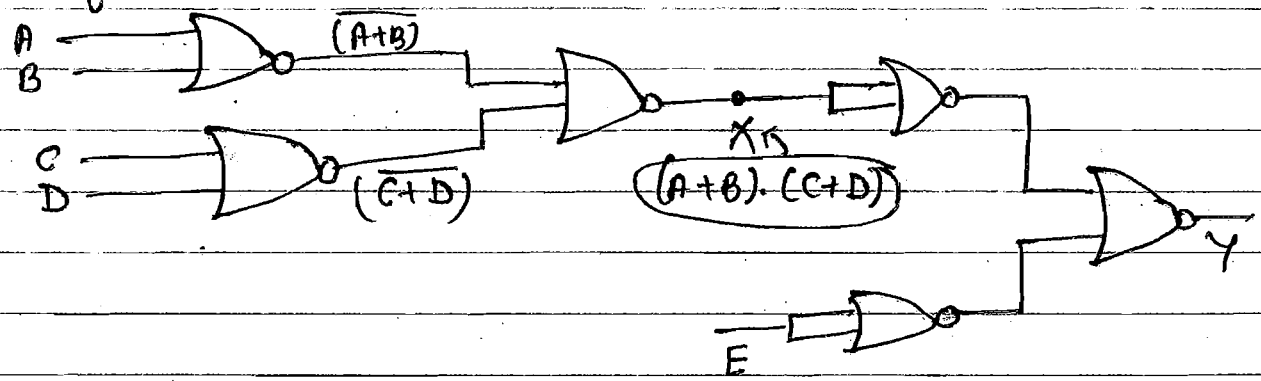
Sol^n $Y = (A+B).(C+D)$



$$Y = \overline{(\overline{A+B}) + C\overline{C+D}}$$
$$= \overline{(\overline{A+B})}.\overline{(\overline{C+D})}$$
$$= (A+B).(C+D)$$ Ans

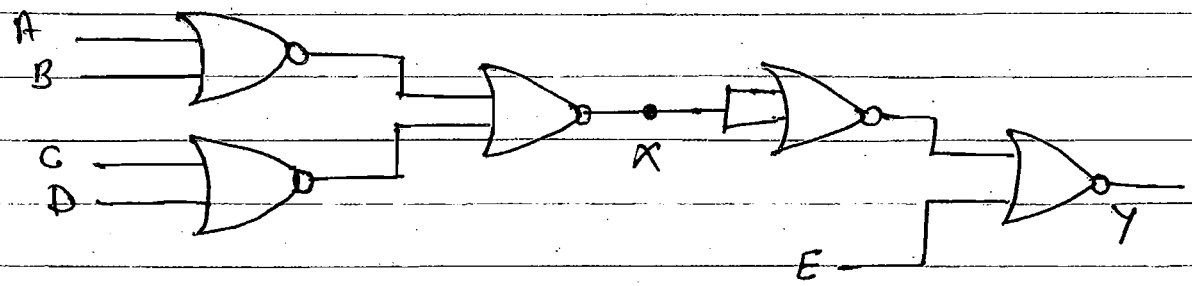
Ques For the given expression $Y = (A+B).(C+D).E$ by using minimum number of two input NOR gates.

Ans:



So $Y = (A+B).(C+D).E$

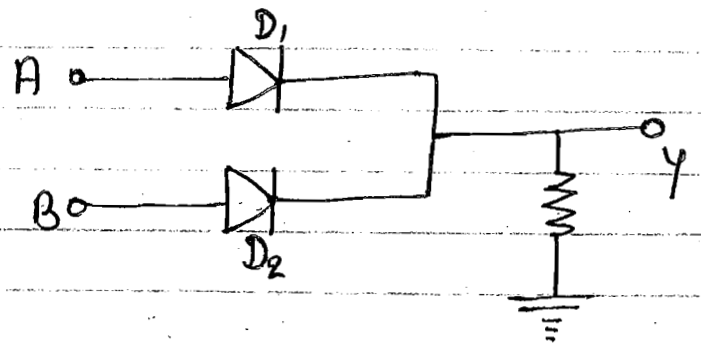
Ques Similarly impliment $Y = (A+B).(C+D).\bar{E}$.



$$Y = (A+B).(C+D).\bar{E}$$

Gates	NAND	NOR
NOT	1	1
AND	2	3
OR	3	2
Ex-OR	4	5
Ex-NOR	5	4

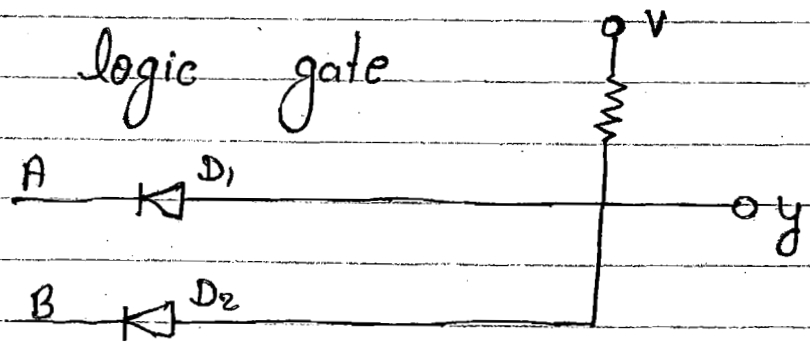
Gates by using diodes



A	B	D_1	D_2	Y
0	0	R.B	R.B	0
0	1	R.B	F.B	1
1	0	F.B	R.B	1
1	1	F.B	F.B	1

So Gate is OR Gate

Ques Identify the logic gate

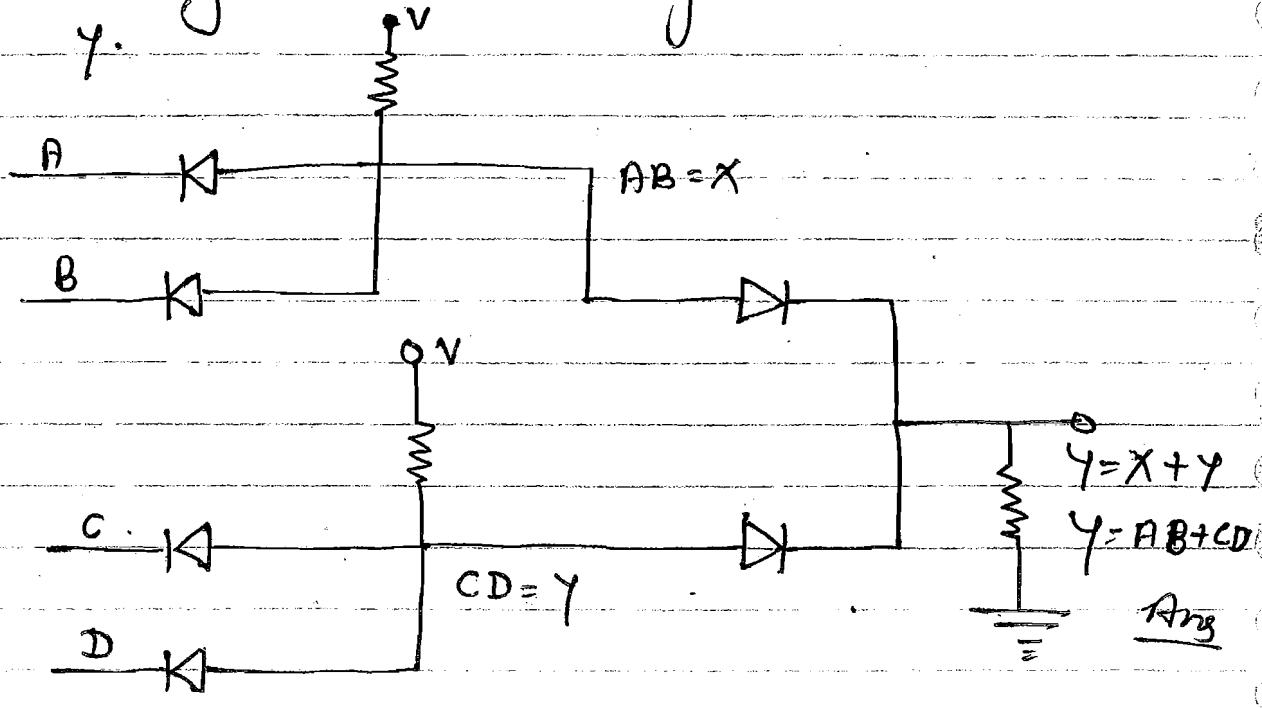


Sol"

A	B	D_1	D_2	Y
0	0	F.B.	F.B.	0
0	1	F.B	R.B.	0
1	0	R.B.	F.B	0
1	1	R.B	R.B	1

So Gate is AND gate.

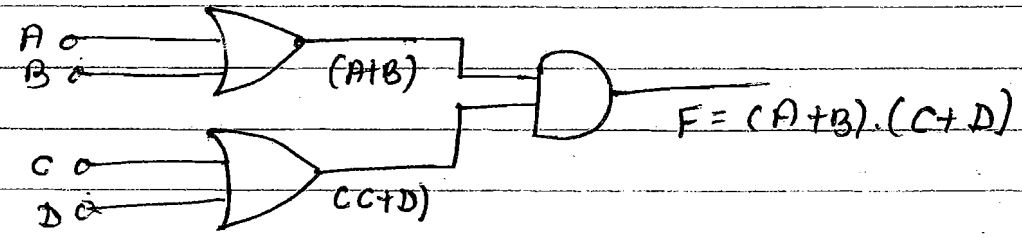
Qus for the given circuit diagram determine o/p Y.



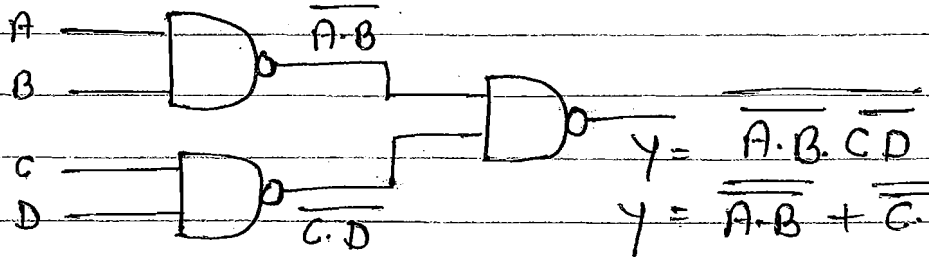
Ans

Qus for the given circuit diagram shown in figure. output expression is F replace every logic gate by using NAND gate. the resultant expression will be ?

(a) F (b) F_D [✓] (c) $\overline{F_D}$ (d) $\overline{F}$

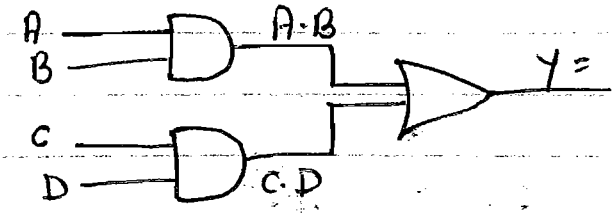


Sol:-



Self dual.

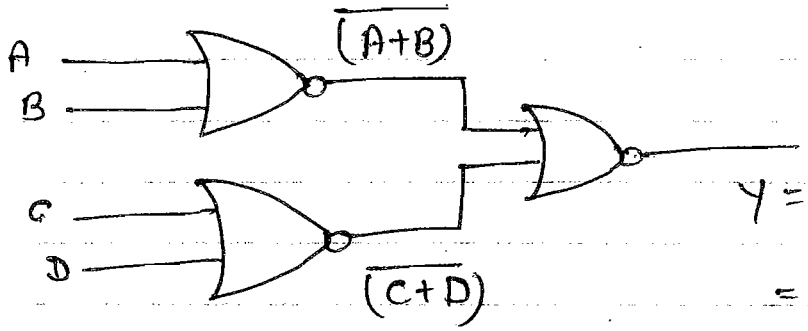
Ques for the given circuit diagram shown



Replace every gate by NOR gate the resultant expression will be-

(a) F (b) F_D [✓] (c) $\bar{F}_D$ (d) $\bar{F}$

Soln-



$Y = \overline{(\overline{A+B}) + (\overline{C+D})}$

$= \overline{(\overline{A+B})} \cdot \overline{(\overline{C+D})}$

$= (A+B) \cdot (C+D)$

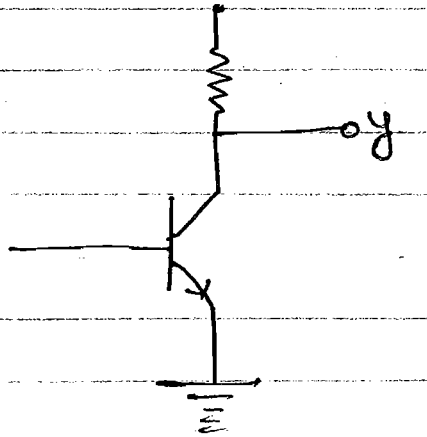
— Self dual.

Ans

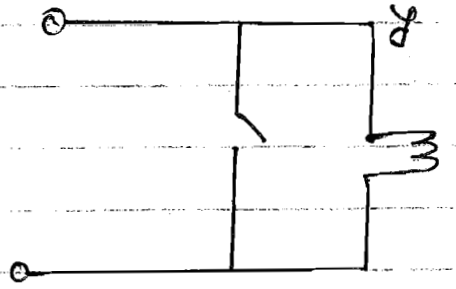
23/July/2014

Logic Gates by using Transistor

Ques for the given circuit diagram identify the logic gate

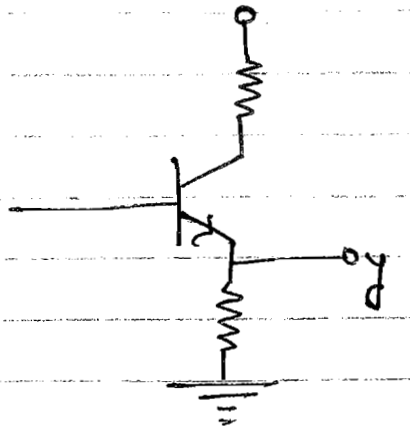


Ans Here the transistor is replaced by a switch we get -

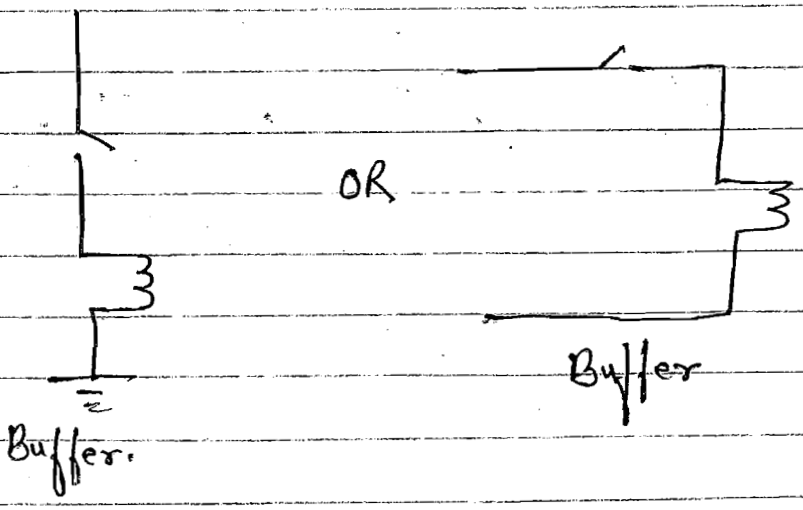


NOT Gate.

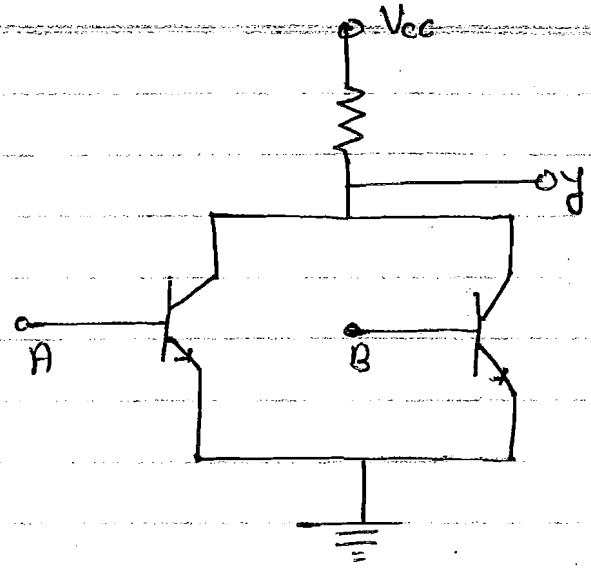
Ques For the given circuit diagram identify the logic gate



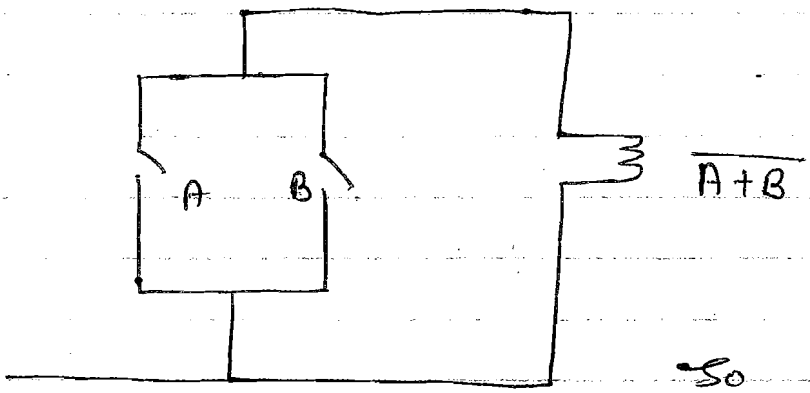
Soln



Ques For the given circuit diagram identify the gate.

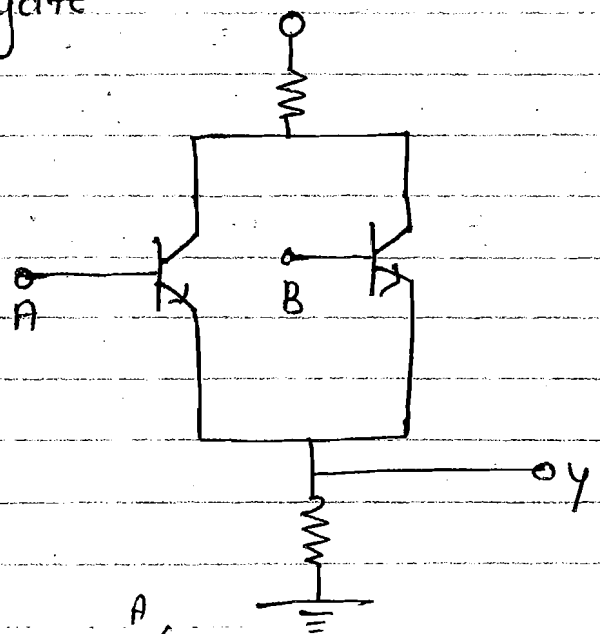


Soln

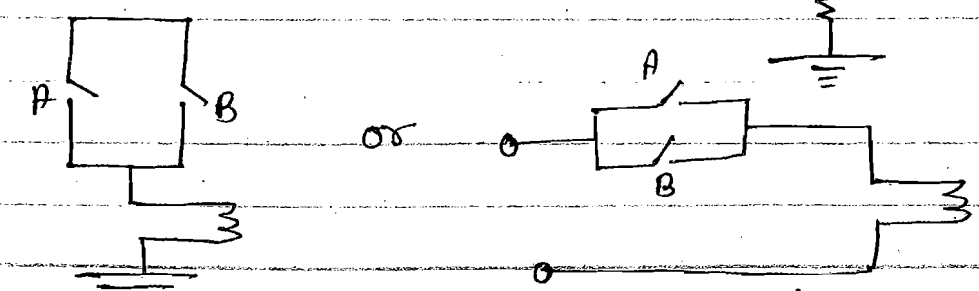


So NOR Gate.

Ques Identify the gate



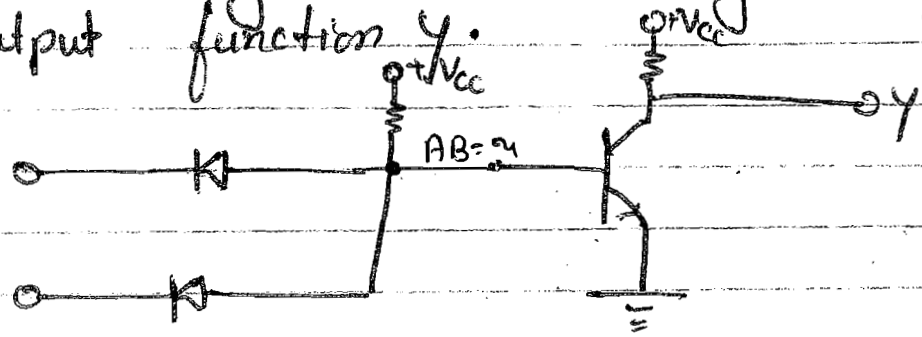
Soln



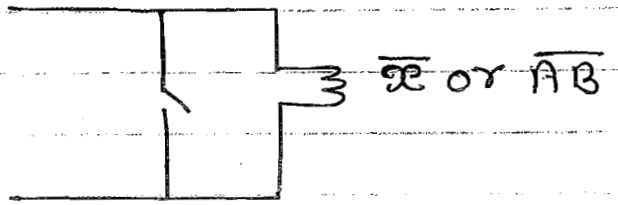
OR Gate

OR Gate.

Ques | For the given circuit diagram find the output function Y.



Sol^n



Logic Circuits

Universal gates are used to impliment logic circuits, which are further clasified into -

1. Combinational Circuits
2. Sequencial Circuits.

1 Combinational Circuits :-

In combinational circuits there is no feedback presents between output and input hence no memory like capacity develops.

e.g. Half Adder, Full Adder, Half Subtractor, Full Subtractor, Multiplexer, Demultiplexer, Comparator etc.

2. Sequencial Circuits :-

In sequential circuits feedback is present, hence memory capacity develops.

e.g. - Flip-Flop, Bistable Multivibrator, Register, Counter.

* Combinational Circuit :-

Steps for Combinational Circuits design.

(i) Identify the number of input and output lines.

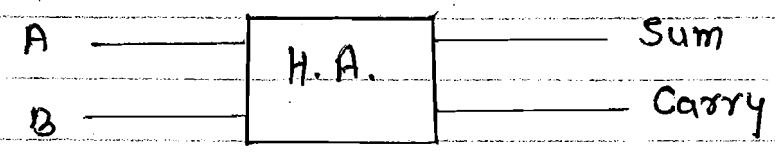
(ii) Develop the Truth table

(iii) Minimise the expression by using SOP & POS

(iv) Implimend the logic circuit by using universal gate.

* Half Adder :-

It is also called as 2-bit addition



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

SOP expression of sum (y_1) -

$$y_{1(sum)} = \bar{A}B + A\bar{B}$$

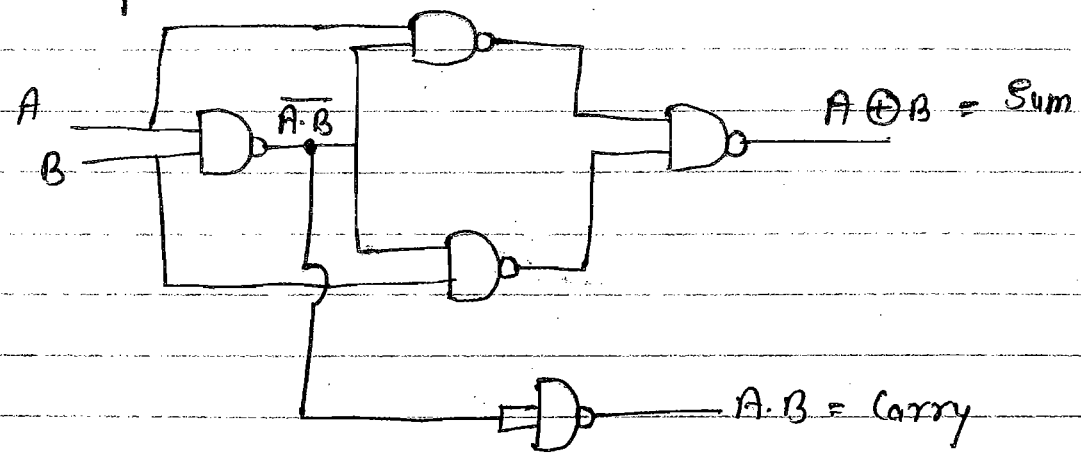
$$y_{1(sum)} = A \oplus B \quad \text{— (I)}$$

SOP expression of carry (y_2) -

$$y_{2(carry)} = A.B. \quad \text{— (II)}$$

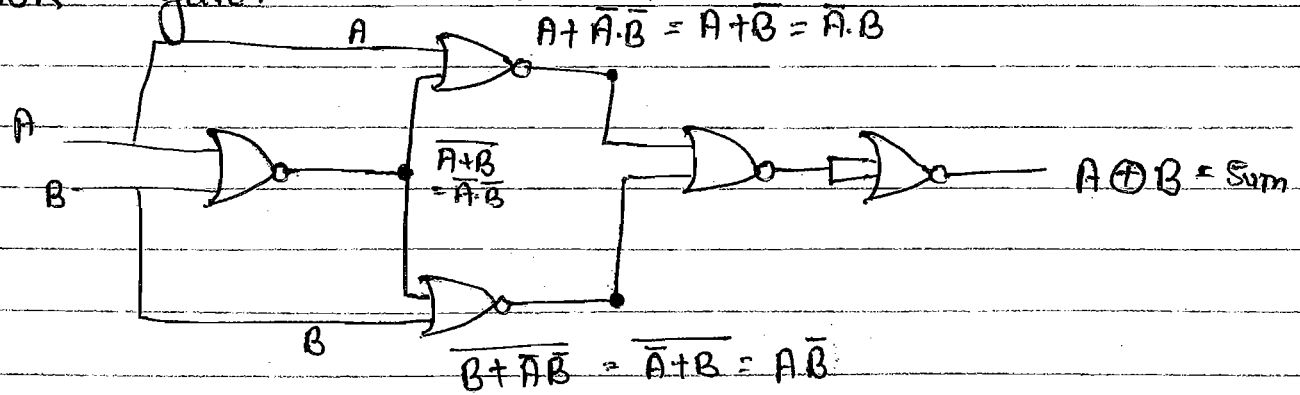
Ques Impliment H.A. by using minimum number of two input NAND Gate.

Soln



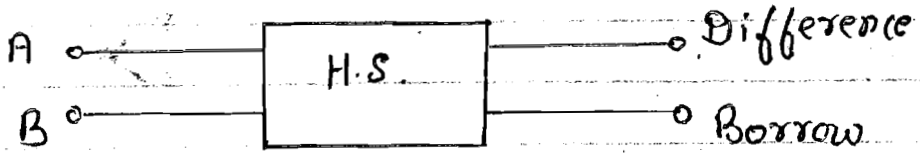
Ques Implimunt H.A. by using minimun numbers of NOR gate.

Soln



* Half Subtractor :-

It is also called as two- bit subtraction.



Impliment Truth Table :-

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

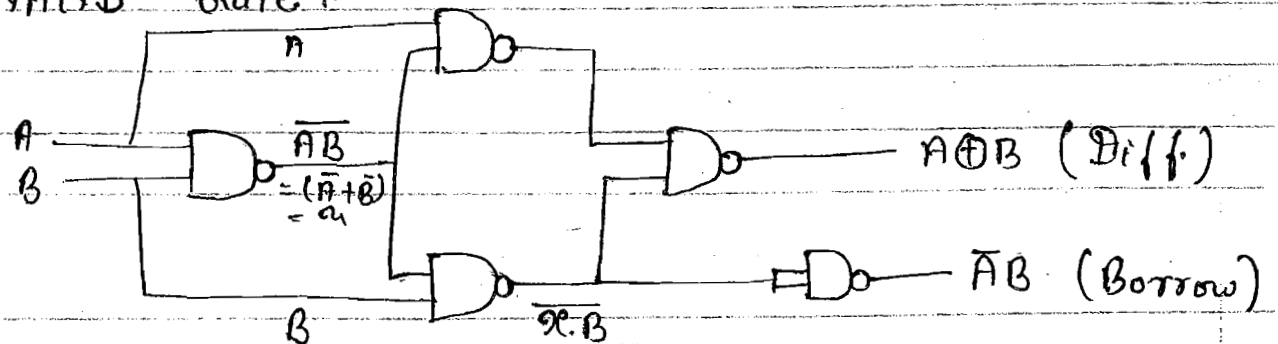
SOP for Difference :-

$$y_{Diff.} = \bar{A}B + A\bar{B} = A \oplus B$$

SOP for Borrow :-

$$y_{(Borrow)} = \bar{A}B$$

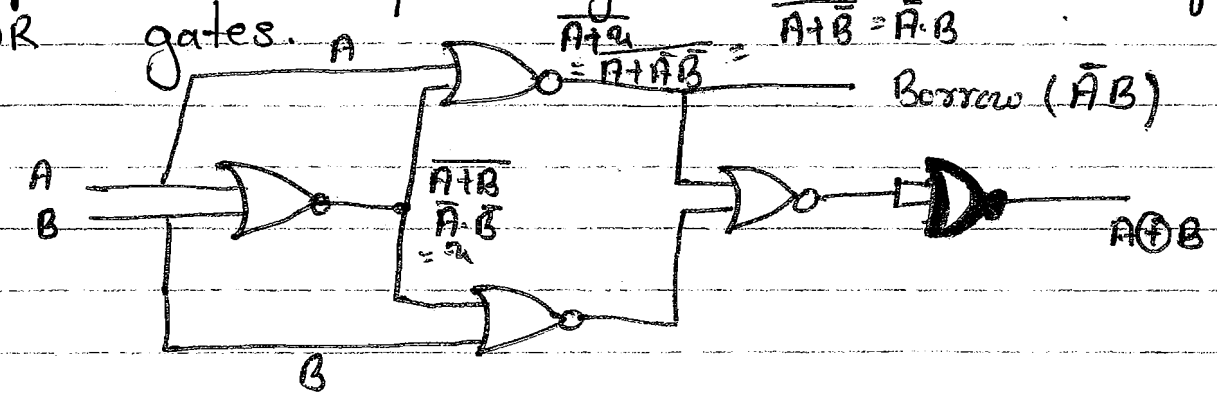
Impliment H.S. by using minimum number of NAND Gate :-



$$\overline{x \cdot B}$$
$$\overline{(\bar{A}+\bar{B}) \cdot B}$$
$$= \overline{\bar{A}B + \bar{B}B}$$
$$= \overline{\bar{A}B}$$

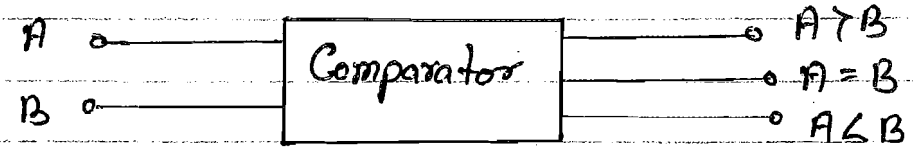
Ques Impliment H.S. by using minimum number of NOR gates.

Sol^{n}



- H.A./H.S. ⟶ NAND/NOR ⟶ S

* Comparator {Single bit}:-



Impliment Truth Table:-

		Y_1	Y_2	Y_3
A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

SOP for A > B:-

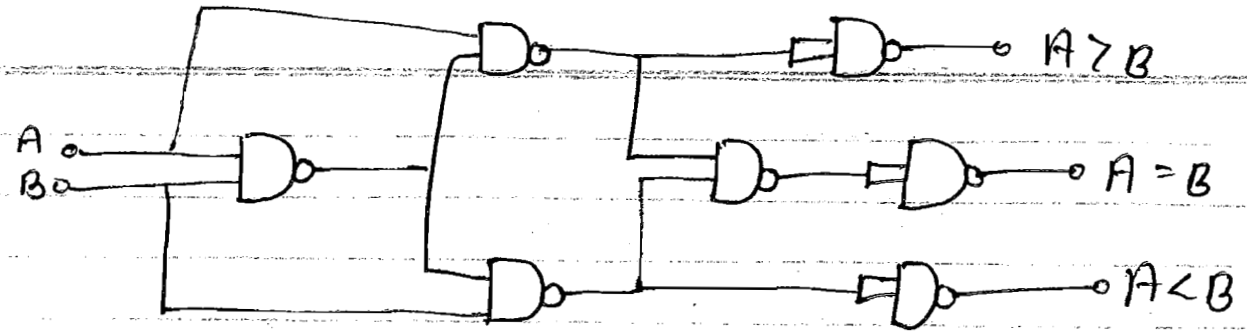
$$Y_1 = A\bar{B} \quad \text{——} (I)$$

SOP for A = B:-

$$Y_2 = \bar{A}\bar{B} + AB = A \odot B \quad \text{——} (II)$$

SOP for A < B:-

$$Y_3 = \bar{A}B \quad \text{——} (III)$$



Circuit Diagram of Comparator.

Ques Write the expression for 2-bit Comparator.

Soln

For A = B

$\overbrace{A_2\ A_1}^{A}$ $\quad$ $\overbrace{B_2\ B_1}^{B}$

like 19 = 19

Here 1 = 1 & 9 = 9

Analogus,

$$(A_2 = B_2)\ \&\ (A_1 = B_1)$$

$$= \boxed{(A_2 \odot B_2) \cdot (A_1 \odot B_1)}$$

For A > B :-

$\overbrace{A_2\ A_1}^{A}$ $\quad$ $\overbrace{B_2\ B_1}^{B}$

like 19 > 19 or 29 > 19

Analogus,

$$(A_2 > B_2)\ \text{or}\ (A_2 = B_2)\ \&\ (A_1 > B_1)$$

$$= \boxed{(A_2 \cdot \overline{B}_2) + (A_2 \odot B_2) \cdot (A_1 \cdot \overline{B}_1)}$$

For A < B :-

$\overbrace{A_2\ A_1}^{A}$ $\quad$ $\overbrace{B_2\ B_1}^{B}$

like 19 < 29 or 17 < 19

$= A_2 < B_2) \text{ OR } (A_2 = B_2) \text{ \& } (A_1 < B_1)$

$= \boxed{\bar{A}_2 B_2 + (A_2 \odot B_2) \cdot \bar{A}_1 B_1}$

Ques Write the expression for 3-bit comparator.

Soln:

for $A = B$:- $\overbrace{A_3\ A_2\ A_1}^{A}$ $\overbrace{B_3\ B_2\ B_1}^{B}$

like 199 199

$= (A_3 = B_3) \text{ \& } (A_2 = B_2) \text{ \& } (A_1 = B_1)$

$= \boxed{(A_3 \odot B_3) \cdot (A_2 \odot B_2) \cdot (A_1 \odot B_1)}$

for $A > B$:- $\overbrace{A_3\ A_2\ A_1}^{A}$ $\overbrace{B_3\ B_2\ B_1}^{B}$

like 200 or 119
199 117

or 197
107

$= (A_3 > B_3) \text{ or } (A_3 = B_3) \text{ \& } (A_2 > B_2) \text{ or } (A_3 = B_3) \text{ \& } (A_2 = B_2) \text{ \& } (A_1 > B_1)$

$= \boxed{A_3 \bar{B}_3 + (A_3 \odot B_3) \cdot (A_2 \bar{B}_2) + (A_3 \odot B_3) \cdot (A_2 \odot B_2) \cdot A_1 \bar{B}_1}$

for $A < B$ $\overbrace{A_3\ A_2\ A_1}^{A}$ $\overbrace{B_3\ B_2\ B_1}^{B}$

* General Expression for n-bit :-

$\underbrace{A_n\ A_{n-1} - - - \cdots A_1}_{A}$

$\underbrace{B_n\ B_{n-1} - - - - B_1}_{B}$

For $A = B$:-

$$(A_n \odot B_n).(A_{n-1} \odot B_{n-1}) - - - - (A_1 \odot B_1)$$

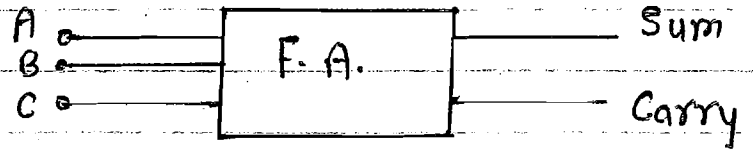
For $A > B$:-

$$A_n \bar{B}_n + (A_n \odot B_n).(A_{n-1}.\bar{B}_{n-1}) + - - - (A_n \odot B_n).(A_{n-1} \odot B_{n-1}) - - - - A_1.\bar{B}_1$$

For $A < B$:-

* Full Adder :-

Full Adder is called as 3-bit addition.



Truth Table :-

A B C	SUM	CARRY
0 0 0	0	0
0 0 1	1	0
0 1 0	1	0
0 1 1	0	1
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	1	1

SOP for sum :-

$$Y_{sum} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$
$$= \bar{A}[B \oplus C] + A[\overline{B \oplus C}]$$

let $B \oplus C = X$

So $Y_{sum} = \bar{A}X + A\bar{X}$

$$= A \oplus X$$

$$\boxed{Y_{sum} = A \oplus B \oplus C}$$

SOP for Carry :-

$$y_{carry} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}BC + AB\bar{C} + AC(B+\bar{B})$$

$$= \bar{A}BC + A(\underset{3.2}{B\bar{C}} + \underset{1}{\bar{C}})$$

$$= \bar{A}BC + A[B+C]$$

$$= \bar{A}BC + AB + AC$$

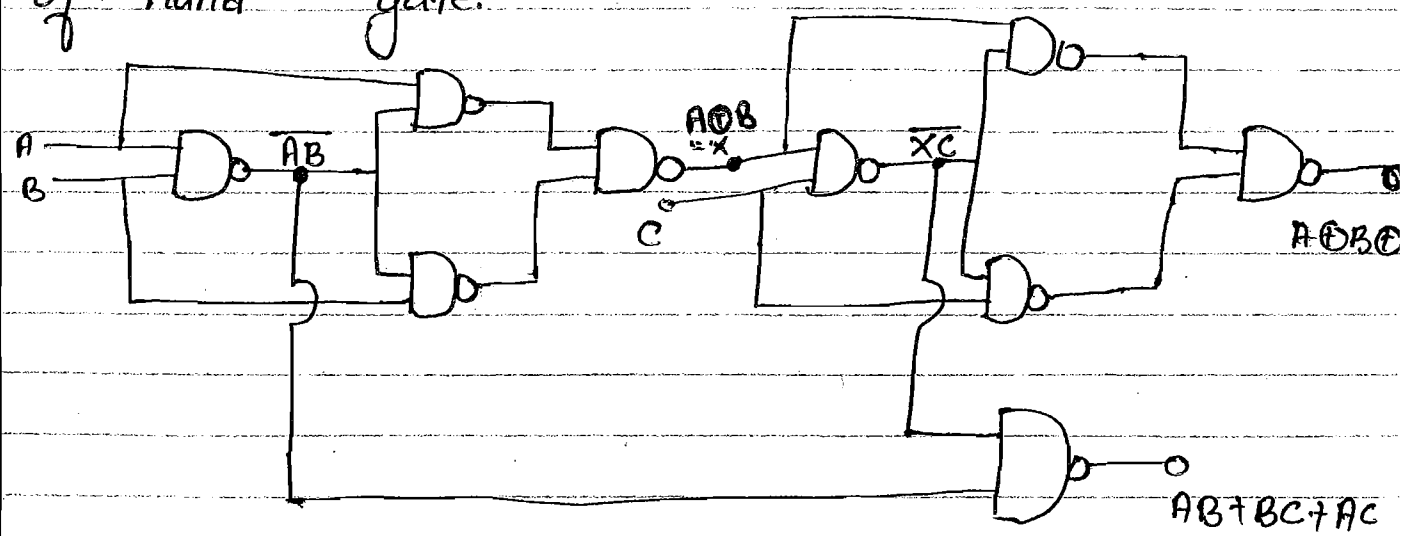
$$= B(\underset{3.2}{\bar{A}C} + \underset{1}{A}) + AC$$

$$= B(A+C) + AC$$

$$\boxed{y_{carry} = AB + BC + AC}$$

Qus Impliment full adder by using minimum numbe of nand gate.

Soln



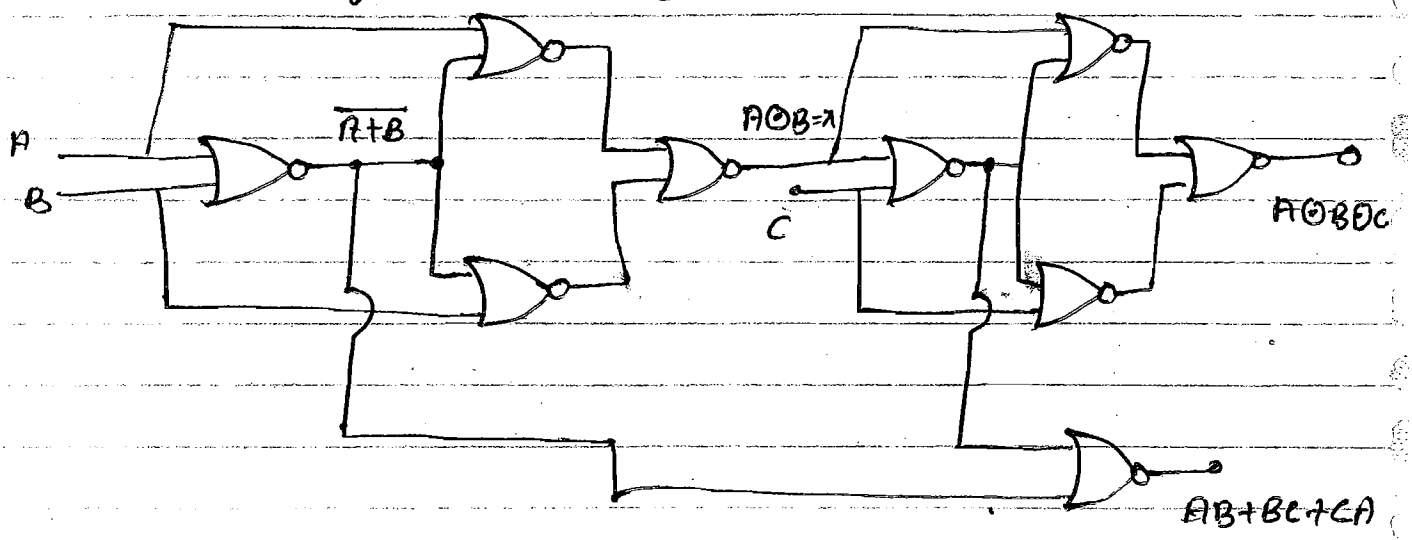
Sum = $A \oplus B \oplus C$

Carry = $AB + BC + AC$

$\overline{(A \oplus B).C}$ =

Ques Impliment Full Adder by using minimum number of NOR gate.

Soln



Note :-

for three input $A \odot B \odot C$ is equivalent to $A \odot B \odot C$ with respect to output.

Ques Find the output minimise expression for three input functions if majority number of inputs are high output is assumed of high.

Soln

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1 → $\bar{A}BC$
1	0	0	0
1	0	1	1 → $A\bar{B}C$
1	1	0	1 → $AB\bar{C}$
1	1	1	1 → ABC

$Y_{SOP} = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= \bar{A}BC + A\bar{B}C + AB \quad = \bar{A}BC + A(B+\bar{B}C) = \bar{A}BC + AB + AC$

$= B(A+\bar{A}C) + AC \quad = B(A+C) + AC = AB + BC + AC$

$Y_{SOP} = AB + BC + AC$ Ans

Ques For the previous ques. output is high when minority number of inputs are high.

Sol^n

A	B	C	Y	
0	0	0	1	$\rightarrow \bar{A}\bar{B}\bar{C}$
0	0	1	1	$\rightarrow \bar{A}\bar{B}C$
0	1	0	1	$\rightarrow \bar{A}B\bar{C}$
0	1	1	0	
1	0	0	1	$\rightarrow A\bar{B}\bar{C}$
1	0	1	0	
1	1	0	0	
1	1	1	0	

$$
\begin{aligned}
Y_{SOP} &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} \\
&= \bar{A}\bar{B}(\bar{C}+C) + \bar{A}B\bar{C} + A\bar{B}\bar{C} \\
&= \bar{A}\bar{B} + \bar{A}B\bar{C} + A\bar{B}\bar{C} \\
&= \bar{A}[\bar{B} + B\bar{C}] + A\bar{B}\bar{C} \\
&= \bar{A}[\bar{B}+\bar{C}] + A\bar{B}\bar{C} \\
&= \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{A}B\bar{C} \\
&= \bar{A}\bar{B} + \bar{C}[\bar{A} + A\bar{B}] \\
&= \bar{A}\bar{B} + \bar{C}[\bar{A}+\bar{B}]
\end{aligned}
$$

$$\boxed{Y_{SOP} = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}}$$ Ans

Ques Find the o/p minimise expression for output is 1 if input is atleast 3 and maximum is 6.

Sol^n

	A	B	C	Y
0 ←	0	0	0	0
1 ←	0	0	1	0
2 ←	0	1	0	0

3 ←	0	1	1	1	→ $\bar{A}BC$
4 ←	1	0	0	1	→ $A\bar{B}\bar{C}$
5 ←	1	0	1	1	→ $A\bar{B}C$
6 ←	1	1	0	1	→ $AB\bar{C}$
7 ←	1	1	1	0	

$$Y_{SOP} = \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$
$$= \bar{A}BC + A\bar{B} + AB\bar{C}$$
$$= \bar{A}BC + A[\bar{B} + B\bar{C}]$$
$$= \bar{A}BC + A[\bar{B} + \bar{C}]$$

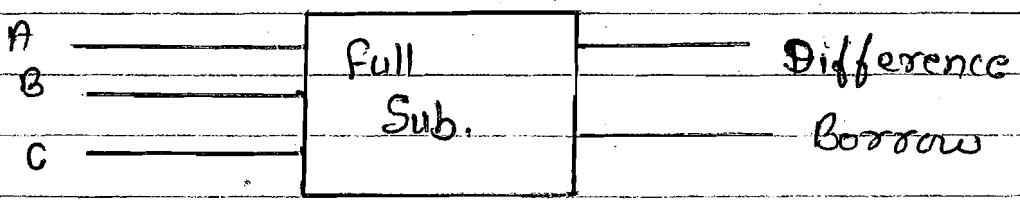
$$Y_{SOP} = \bar{A}BC + A\bar{B} + A\bar{C}$$ Ans

25/July/2014

* Full Subtractor :- [3-bit] :-

Full subtractor is called as 3-bit subtraction.

Symbol :-



Truth Table :-

	A	B	C	D	B
	0	0	0	0	0
$\bar{A}\bar{B}C$ ←	0	0	1	1	1 → $\bar{A}\bar{B}C$
$\bar{A}B\bar{C}$ ←	0	1	0	1	1 → $\bar{A}B\bar{C}$
	0	1	1	0	1 → $\bar{A}BC$
$A\bar{B}\bar{C}$ ←	1	0	0	1	0

	1	0	1	0	0
	1	1	0	0	0
ABC ←	1	1	1	1	1 → ABC

SOP for ~~Sum~~ Difference :-

$$y_{sum} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{A}(\bar{B}C + B\bar{C}) + A[\bar{B}\bar{C} + BC]$$
$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

let $B + C = X$

So,

$$y_{sum} = \bar{A}X + A\bar{X}$$
$$= A \oplus X$$

$$\boxed{y_{sum} = A \oplus B \oplus C}$$

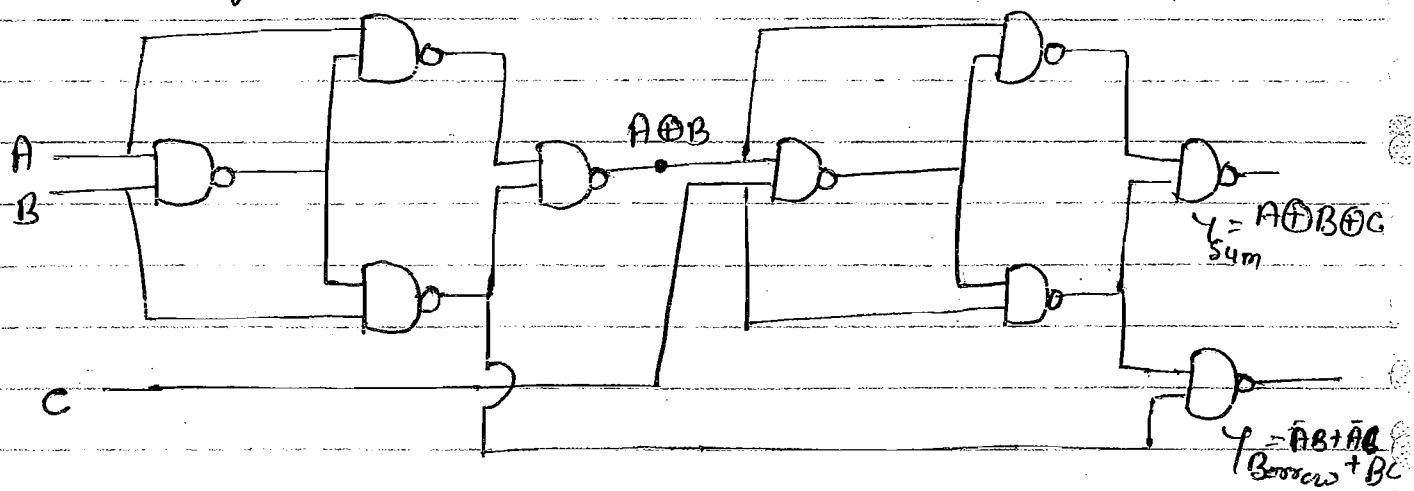
SOP for Borrow :-

$$y_{Borrow} = \bar{A}\bar{B}.C + \bar{A}B\bar{C} + \bar{A}BC + ABC$$
$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + BC(A + \bar{A})$$
$$= \bar{A}\bar{B}C + B(C + \bar{A}\bar{C}) \quad \{\because A + \bar{A} = 1\}$$
$$= \bar{A}\bar{B}C + B(C + \bar{A})(C + \bar{C}) \quad \{\because C + \bar{C} = 1\}$$
$$= \bar{A}\bar{B}C + BC + \bar{A}B$$
$$= \bar{A}(B + \bar{B}C) + BC$$
$$= \bar{A}(B + \bar{B})(B + C) + BC$$
$$= \bar{A}(B + C) + BC \quad \{\because B + \bar{B} = 1\}$$

$$\boxed{y_{Borrow} = \bar{A}B + \bar{A}C + BC}$$ Ans

Q. Implement full subtractor by using min^m no. of NAND Gates.-

Soln



Full Subtractor by using NAND Gate.

* Note :-

FA / FS ⟶ NAND / NOR ⟶ 9

Ques Implement full subtractor by using min^m no. of NOR Gates.-

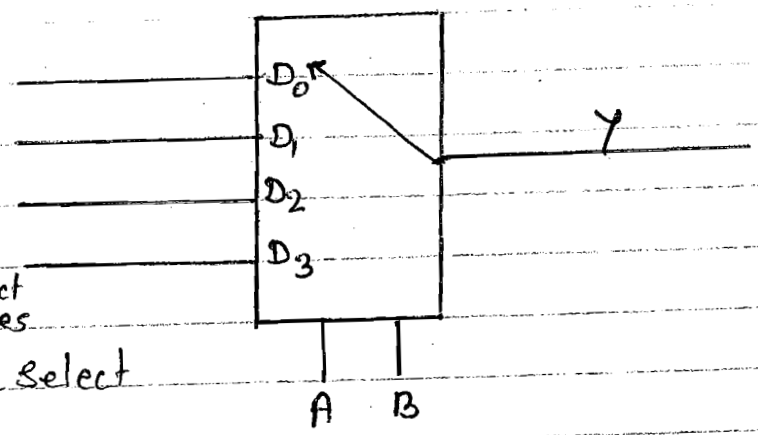
Soln

Multiplexer

A divice which select single output line from multiple number of input lines and display it at output.

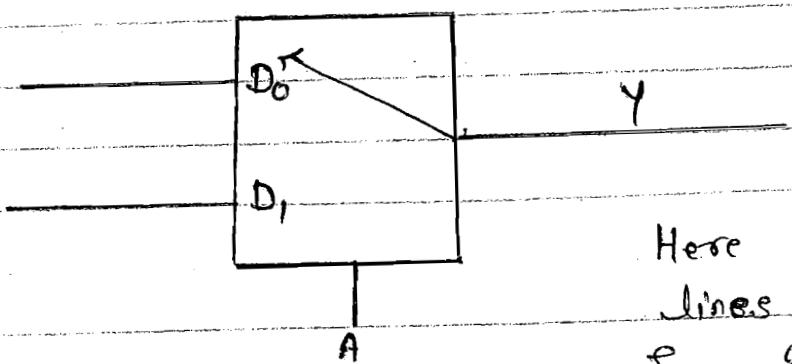
- The internal structure of Mux is a rotatory switch (Commutator).
- It is used for parallel to serial conversion.
- It is also called as universal combinational circuit.

Diagram :-



Since Here
4 input lines
So,
$4 = 2^{②}$ ← Select lines
So, there is 2 select lines (A, B)

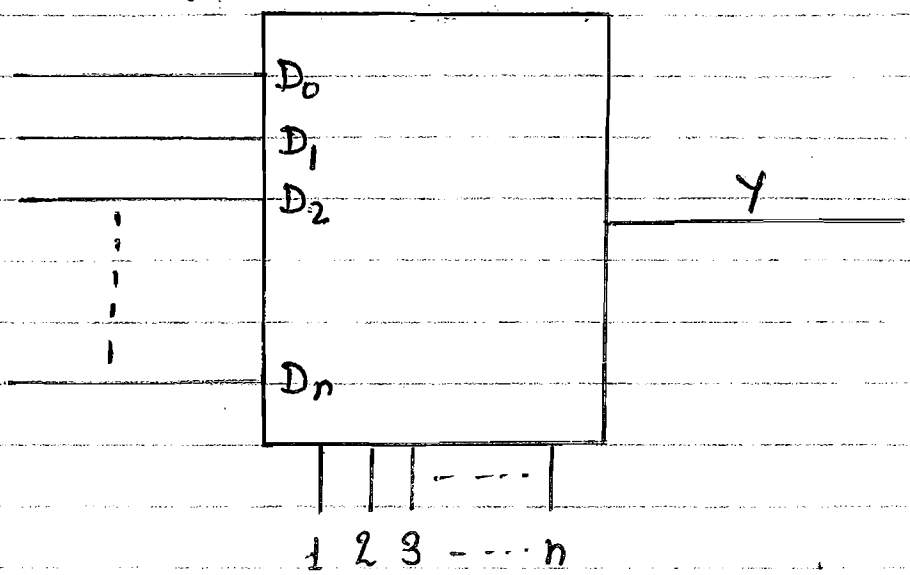
[4x1 Mux]



Here two Inpu
lines ← Select l
So, $2^{①}$

[2x1 Mux] So Here 1 select line.

Similarly for N inputs :-



Here numbers of input lines = N

So

$$N = 2^n$$

(N) ← No. of input lines

(n) ← No. of select line

- A device having 2^n input lines with 'n' number of select line to select single input and display at the output:-

$$N = 2^n$$
$$\log N = \log 2^n$$
$$\log N = n \log 2$$

Since here binary numbers are used so base of logarithem is 2.

$$\log_2 N = n \log_2 2$$

or

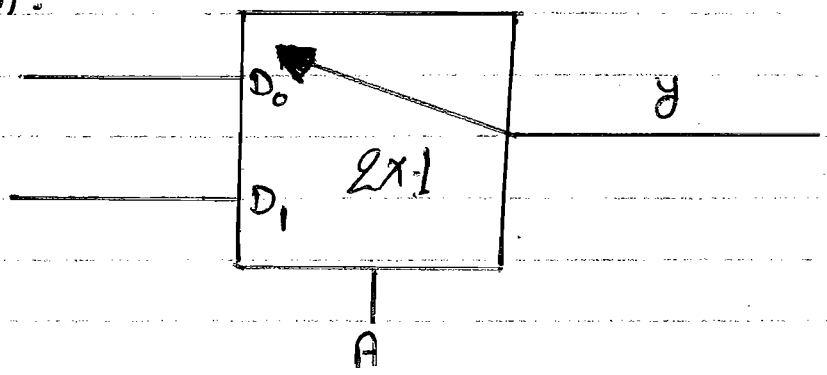
$$\log_2 (N) = (n)$$

No. of input lines — No. of select lines

since $\log_n n = 1$

* 2X1 Multiplexer :-

Diagram :-



SOP (Actual) :-

	A	B	Y
$\bar{A}\bar{B}$ ←	0	0	1
$\bar{A}B$ ←	0	1	0
$A\bar{B}$ ←	1	0	1
AB ←	1	1	1

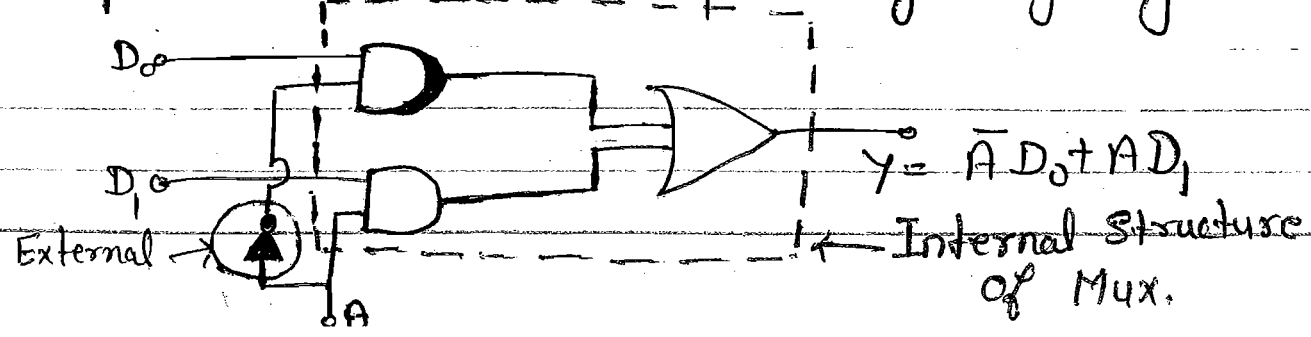
Due to this resop we can not take o/p.

$Y = \bar{A}\bar{B}\cdot 1 + \bar{A}B\cdot 0 + A\bar{B}\cdot 1 + AB\cdot 1 = \bar{A}\bar{B} + A\bar{B} + AB$

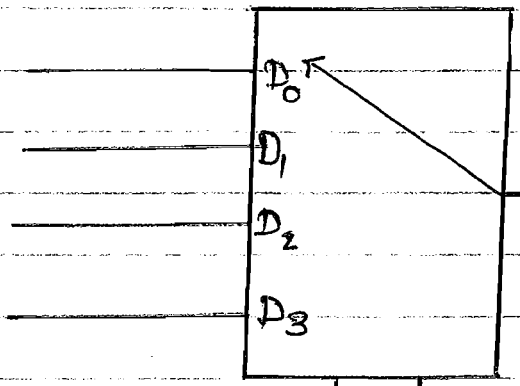
	A	Y
$\bar{A}D_0$ ←	0	D_0
AD_1 ←	1	D_1

$$Y = \bar{A}D_0 + AD_1$$

Qus Implement 2x1 Mux by using logic gates :-



* 4x1 Multiplexer :-



$$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$$

	A	B
0 ←	0	0
1 ←	0	1
2 ←	1	0
3 ←	1	1

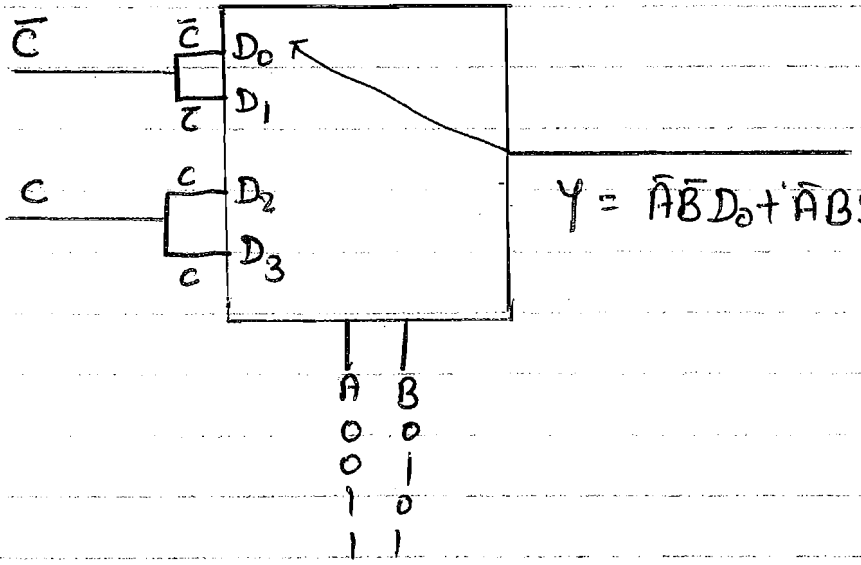
	A	B	Y
$\bar{A}\bar{B}$ ←	0	0	D_0
$\bar{A}B$ ←	0	1	D_1
$A\bar{B}$ ←	1	0	D_2
AB ←	1	1	D_3

So $\boxed{Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3}$

* Minimisation of logic expression by using Mux :-

- Type I :-

Ques Find the output minimise expression for the given Mux circuit.

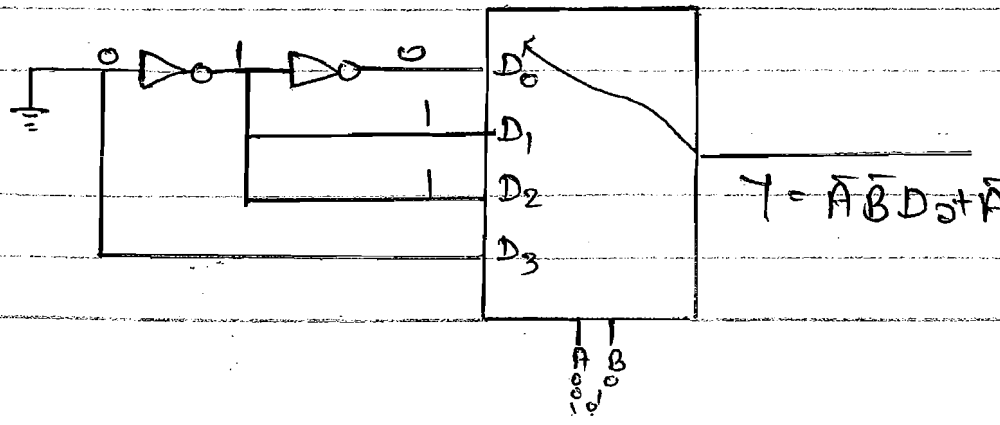


$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$

Sol"

$$y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + ABC$$
$$y = \bar{A}\bar{C}(\bar{B}+B) + AC(\bar{B}+B)$$
$$y = \bar{A}\bar{C} + AC$$
$$\boxed{y = A \odot C}$$

Ques For the given circuit diagram find the minimise expression.



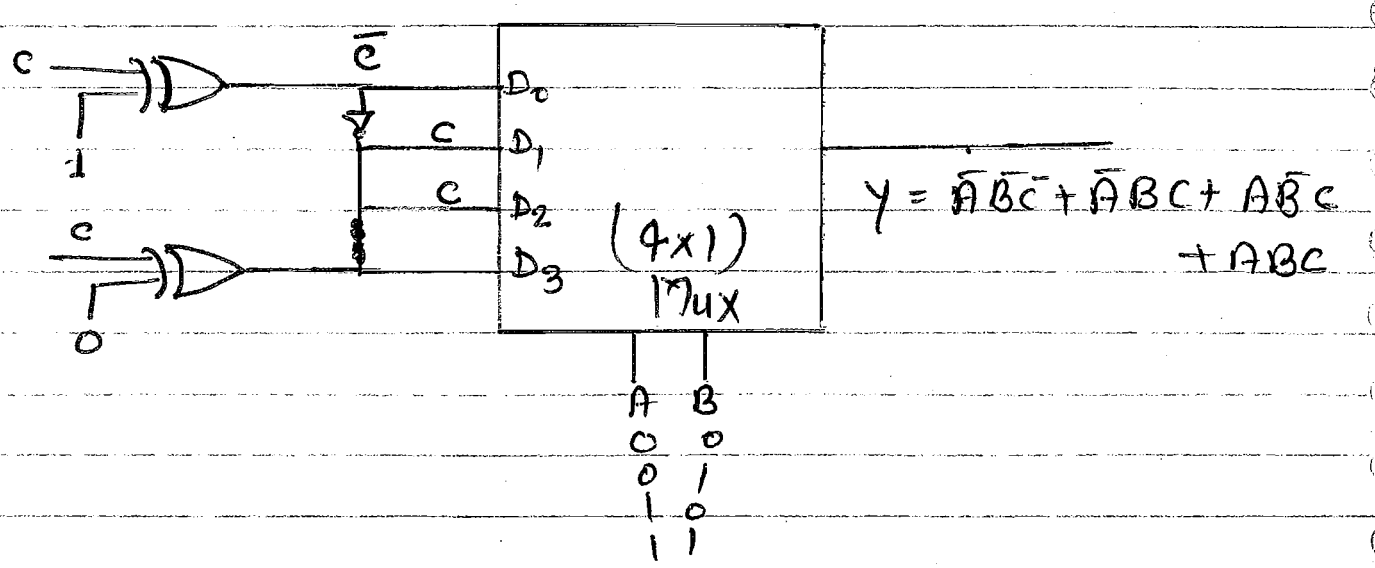
$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + AB$

Sol^n

$$y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$$
$$= \bar{A}\bar{B}\cdot 0 + \bar{A}B\cdot 1 + A\bar{B}\cdot 1 + AB\cdot 0$$
$$= \bar{A}B + A\bar{B}$$

$$\boxed{y = A \oplus B}$$

Q. For the given circuit diagram find minimise expression.



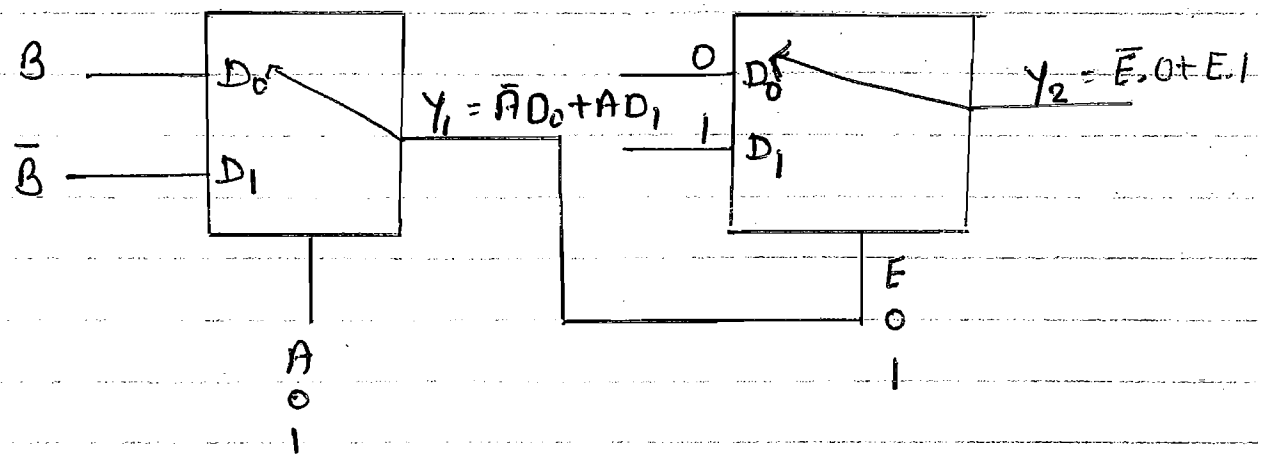
Sol^n

$$y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + ABC$$
$$y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + AC(\bar{B}+B)$$
$$y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + AC$$
$$y = \bar{A}\bar{B}\bar{C} + (\underset{3.2}{\bar{A}B} + \underset{1}{A})C$$
$$y = \bar{A}\bar{B}\bar{C} + C(A+B)(A+\bar{A})$$

$$\boxed{y = \bar{A}\bar{B}\bar{C} + AC + BC}$$

Ques Find the output expression y.

Sol^n



$$y_1 = \bar{A}D_0 + AD_1$$
$$y_1 = \bar{A}B + A\bar{B}$$
$$y_1 = A \oplus B = E \text{ (Sel}_y$$

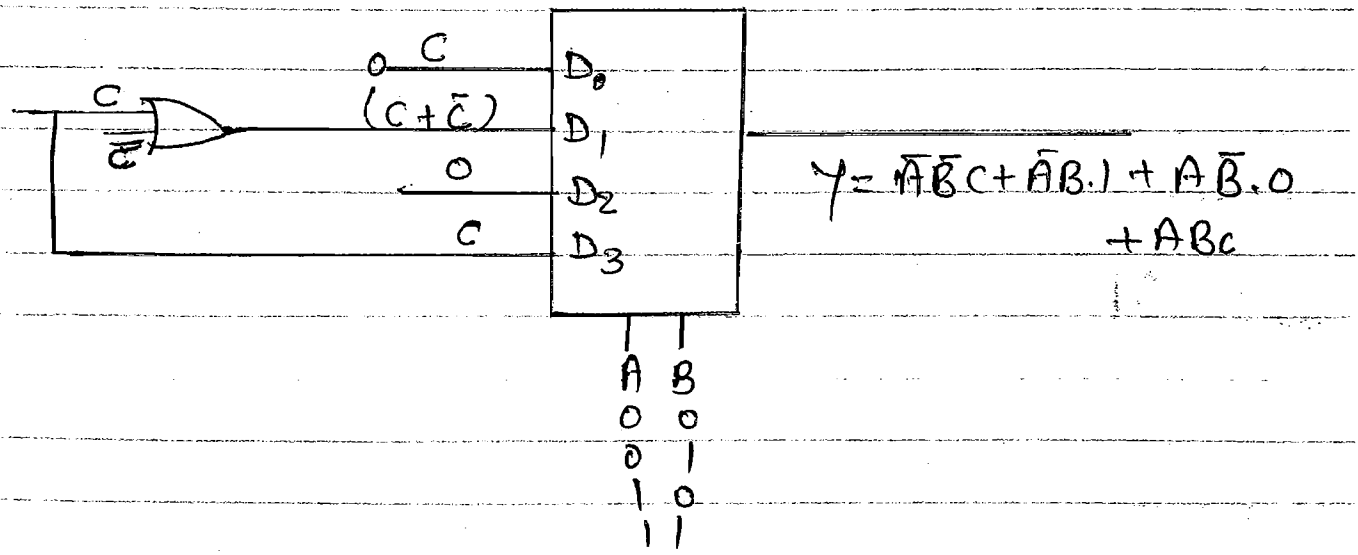
So $y_2 = \bar{E}.0 + E.1$

$$y_2 = \overline{A \oplus B}.0 + A \oplus B.1$$

$$\boxed{y_2 = A \oplus B}$$

Ans

Qus Find the output minimise expression.



Sol^{n}

$$y = \bar{A}\bar{B}C + \bar{A}B(C+\bar{C}) + A\bar{B}\cdot 0 + ABC$$

$$= \bar{A}\bar{B}C + \bar{A}B\cdot 1 + ABC$$

$$= \bar{A}(B + \underset{1+2.3}{\bar{B}C}) + ABC$$

$$= \bar{A}(B+C) + ABC$$

$$= \bar{A}B + \bar{A}C + ABC$$

$$= \bar{A}B + C[\underset{1}{\bar{A}} + \underset{2.3}{AB}]$$

$$= \bar{A}B + C[\bar{A}+B]$$

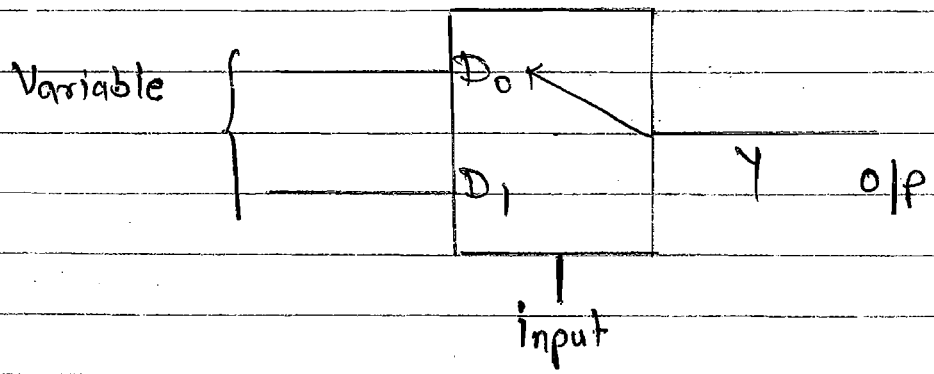
$$\boxed{y = \bar{A}B + \bar{A}C + BC}$$

Ans

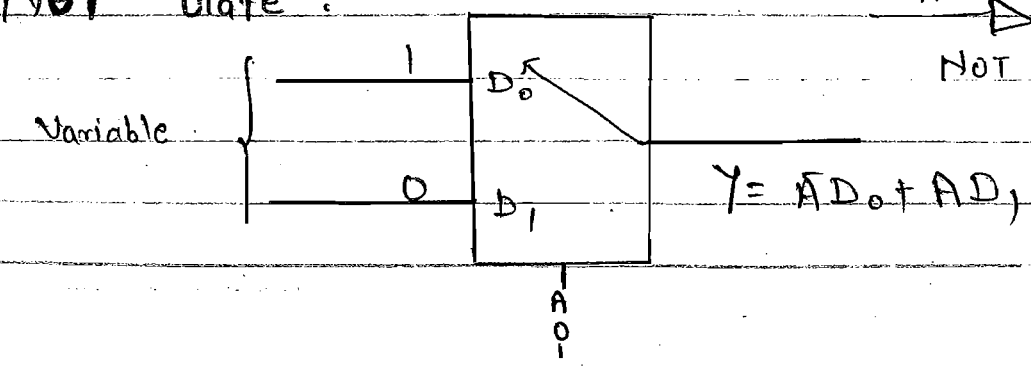
- Type II :-

* Implementation of logic circuits by using Mux.

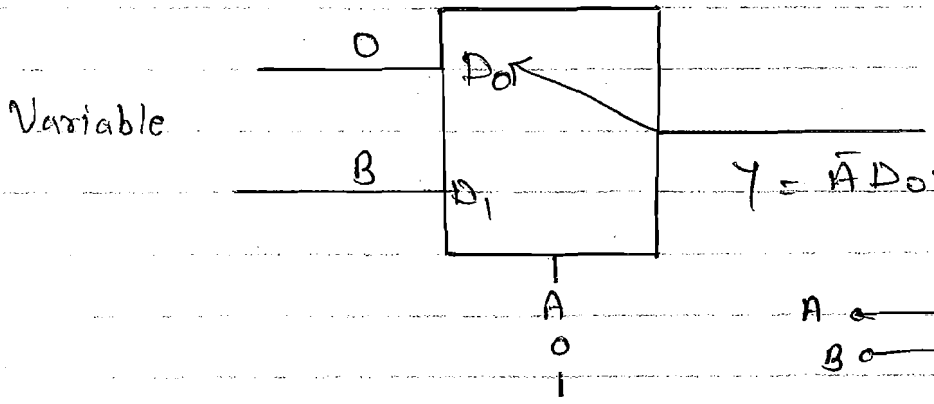
2 x 1 Mux :-

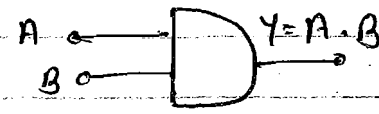


1. NOT Gate :-



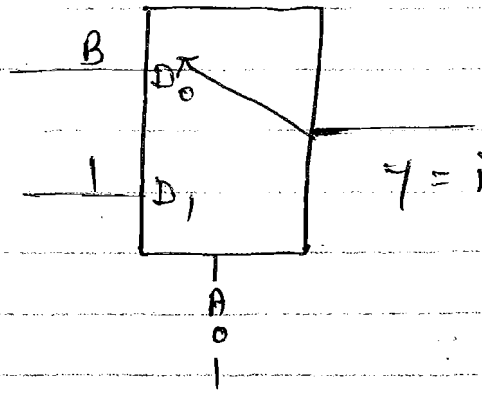
2. AND Gate :-

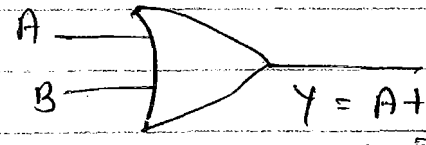




AND Gate.

3. OR - Gate :-



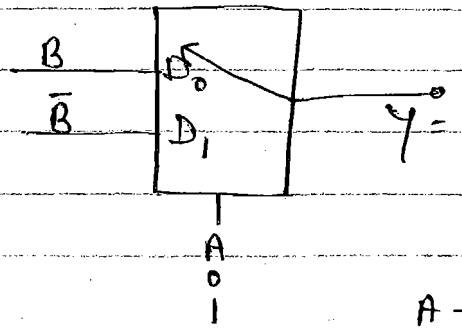


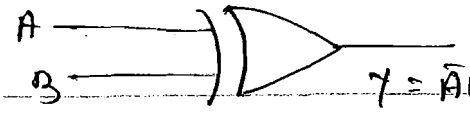
$= A + \bar{A}B$

$= (A+\bar{A})(A+B)$

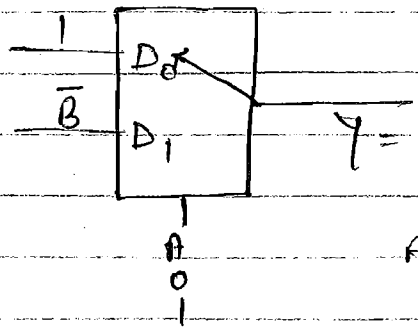
$= (A+B)$

4. Ex-OR Gate :-

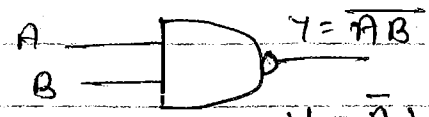




5. NAND Gate :-



$Y = \bar{A}D_0 + AD_1$



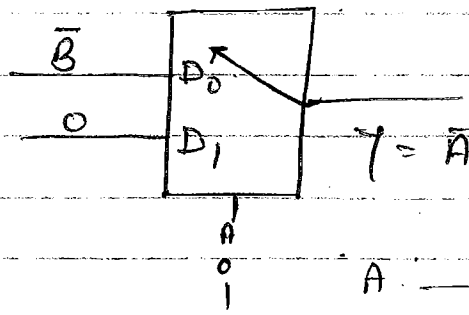
$Y = \overline{AB}$

$Y = \bar{A} + \bar{B}$

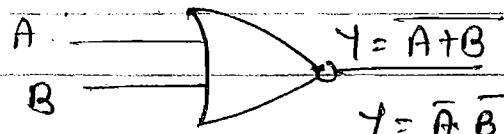
$Y = \bar{A} + A\bar{B}$

$Y = \bar{A} + \bar{B}$

6. NOR Gate :-



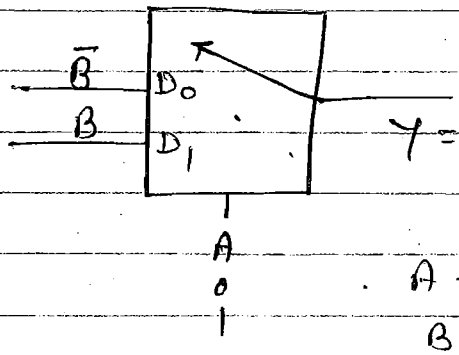
$Y = \bar{A}D_0 + AD_1$



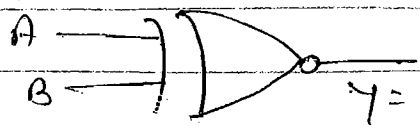
$Y = \overline{A+B}$

$Y = \bar{A}\,\bar{B}$

7. Ex- NOR Gate :-



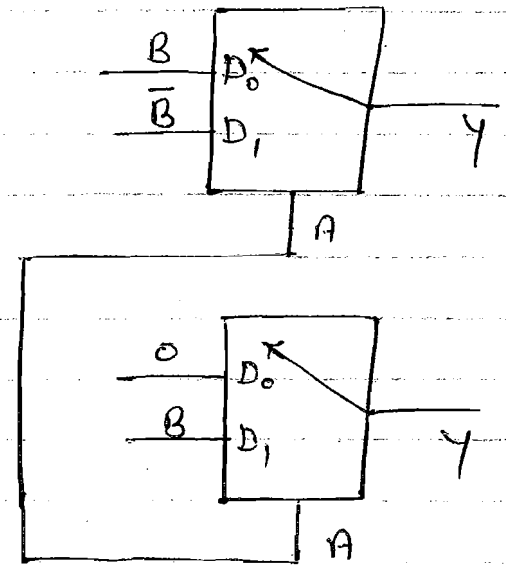
$Y = \bar{A}D_0 + AD_1$



$Y = \bar{A}\bar{B} + AB$

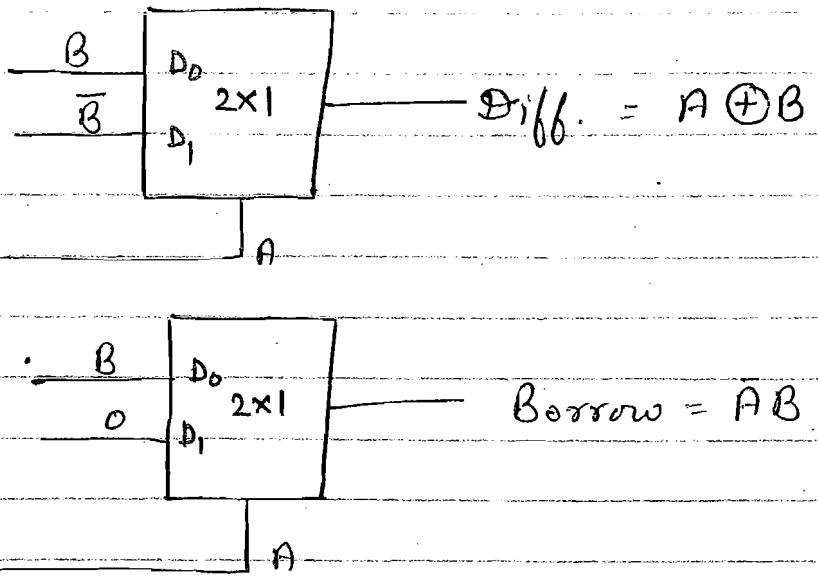
Ques Impliment half adder by using 2×1 mux.

Soln



Ques Impliment half subtractor by using 2×1 Mux.

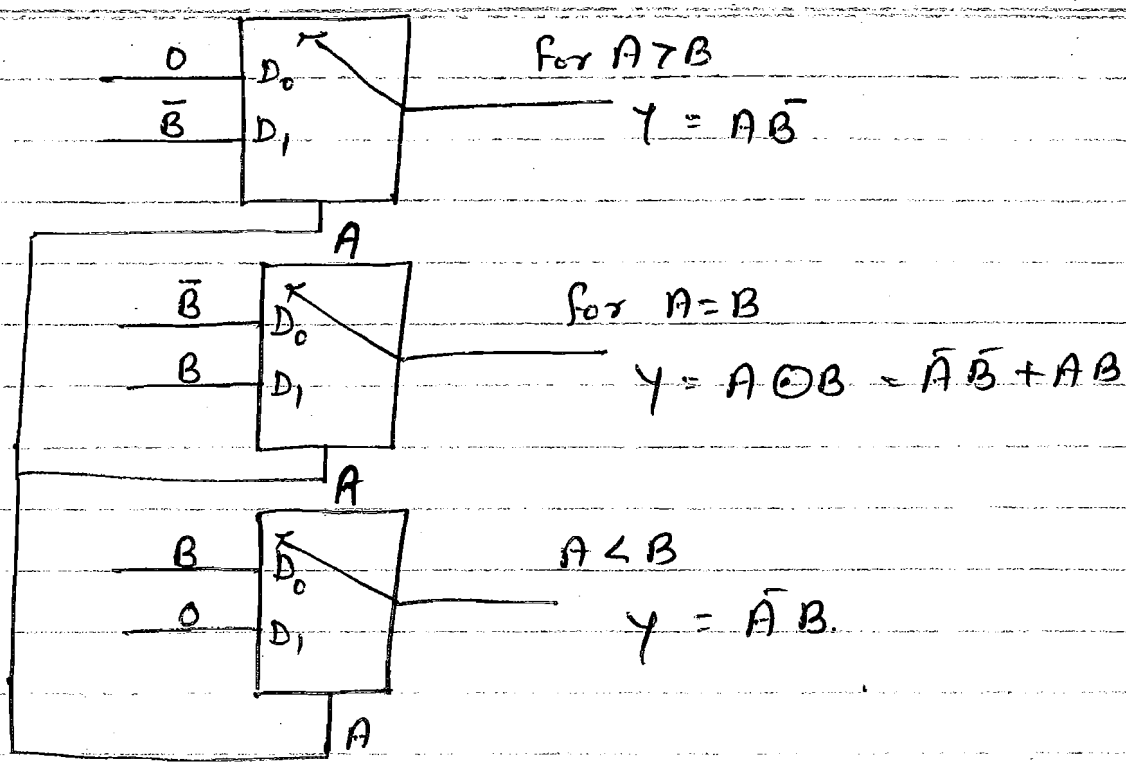
Ans



Ques By Using 2×1 Mux impliment single bit comparator.

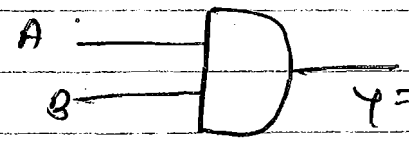
Soln

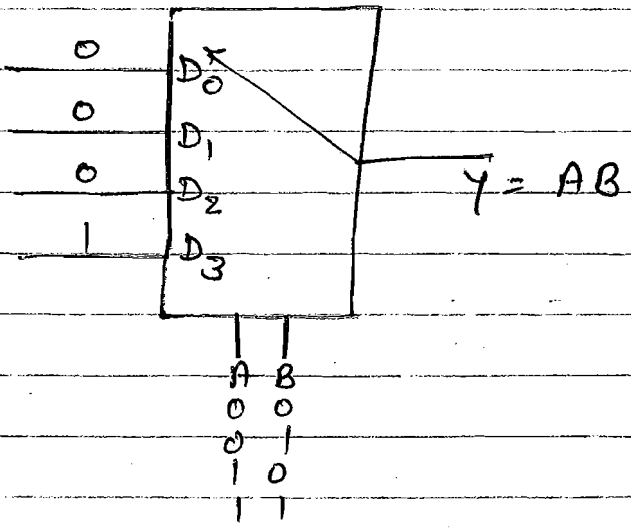
∵ Single bit comparator has 3 o/ps (for A>B, A=B & A<B) So we use 3, 2×1 Mux.



2. Construct gate by using 4x1 Muxs.

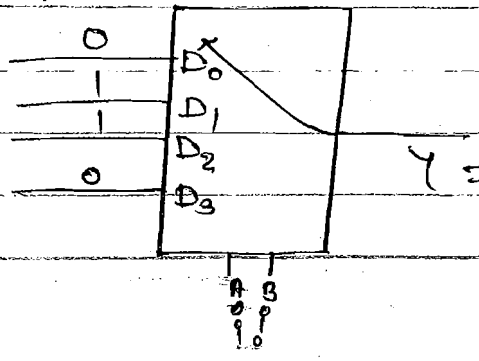
1 AND Gate :-



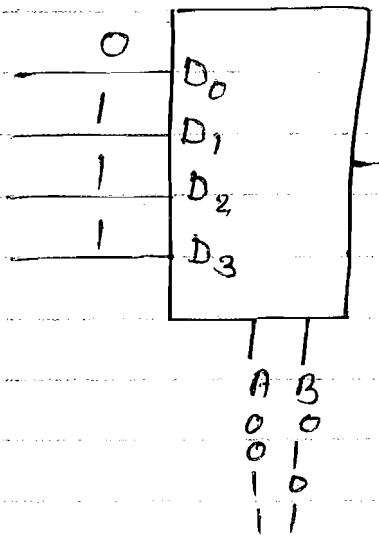


A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2. Ex-OR Gate :-



3 OR Gate :-

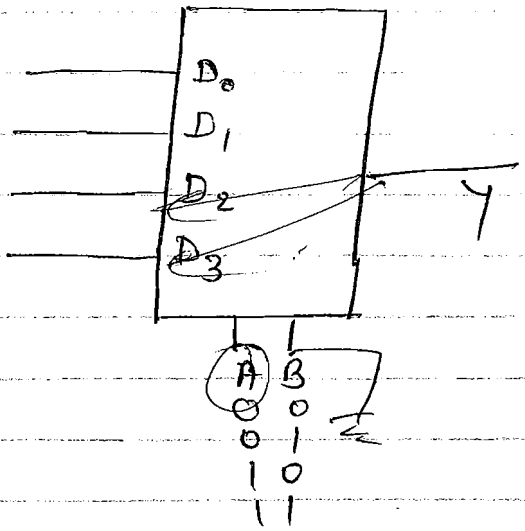


$Y = \bar{A}B + A\bar{B} + AB = \bar{A}B + A(\bar{B}+B)$

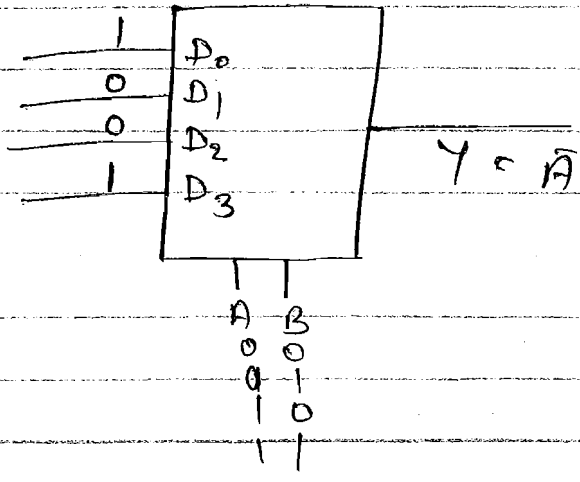
$= \bar{A}B + A = (\bar{A}+A)(A+B)$

$Y = A + B$

4. NOT Gate :-

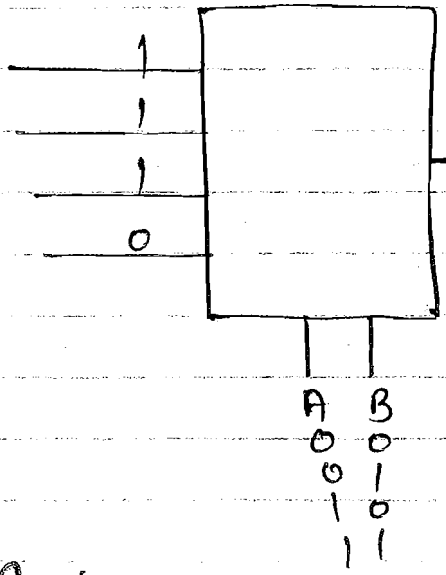


5. Ex-NOR Gate -



$Y = \bar{A}\bar{B} + AB$

6. NAND Gate :-

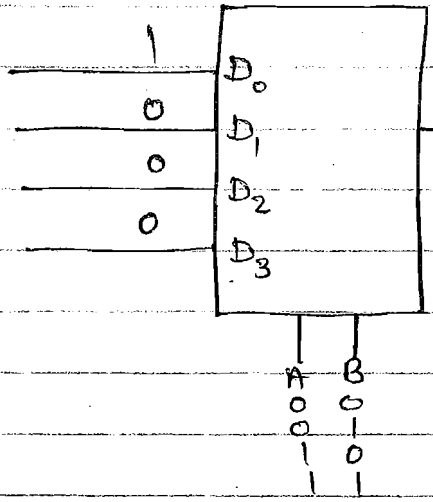


$Y = \bar{A}\bar{B} + \bar{A}B + A\bar{B} = \bar{A}(\bar{B}+B) + A\bar{B}$

$Y = \bar{A} + A\bar{B} = (\bar{A}+A)(\bar{A}+\bar{B})$

$Y = \overline{AB}$ $\left\{ \because \bar{A}+A = 1 \right.$ & $\left. \bar{A}+\bar{B} = \overline{AB} \right.$

7. NOR Gate :-



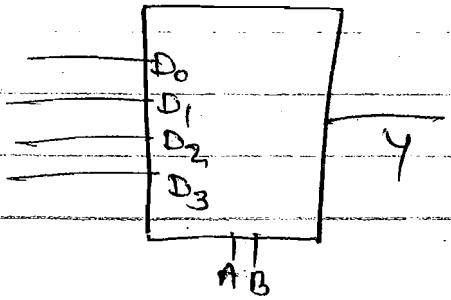
$Y = \bar{A}.\bar{B} = \overline{(A+B)}$

* Type III :-

Identification of number of Mux required for the implimentation of higher order mux by using lower order Mux.

Ques Impliment 4x1 Mux by using 2x1 Mux.

Soln

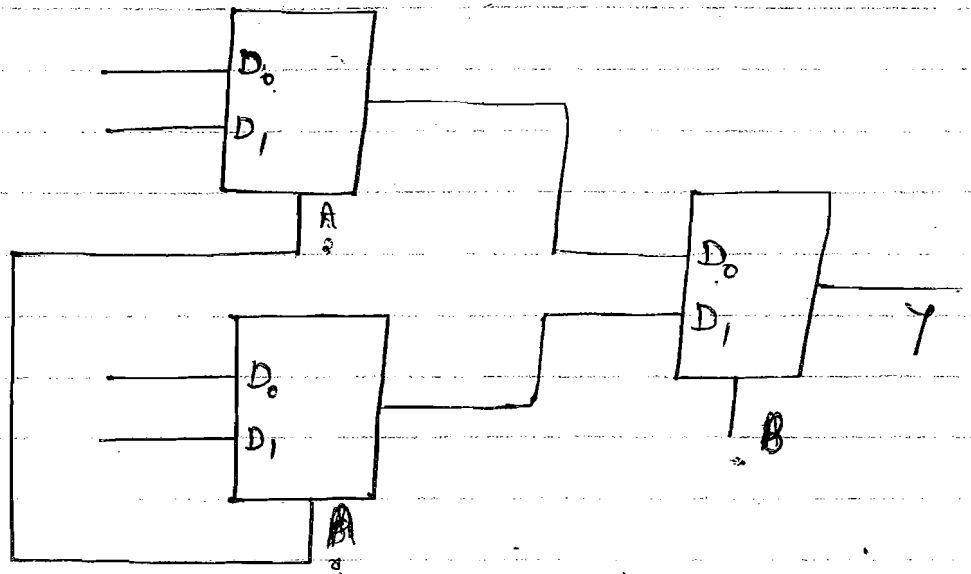


4x1 → 2x1 : $2+1=3$

8x1 → 2x1 : $4+2+1=7$

16x1 → 2x1 : $8+4+2+1=15$

Similarly, $2^n \times 1 \longrightarrow 2^n - 1. \longrightarrow 2 \times 1$



4 x 1 (Mux)

Ques Impliment 8x1 Mux by using 4x1 Mux.

Soln

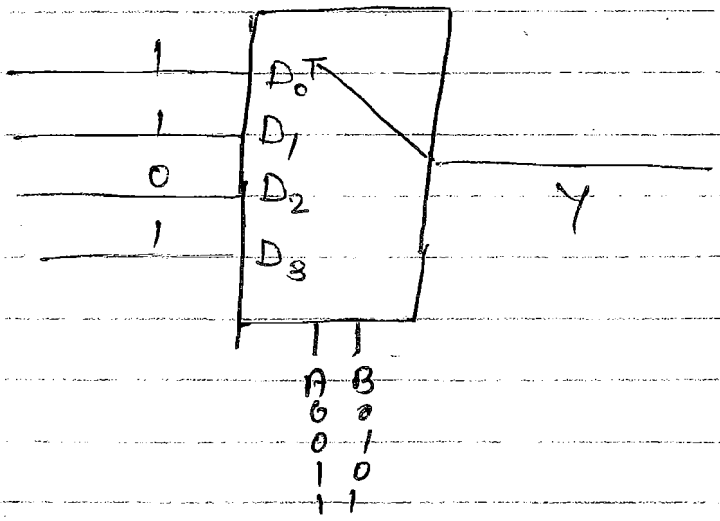
26/July/2014

Type - IV

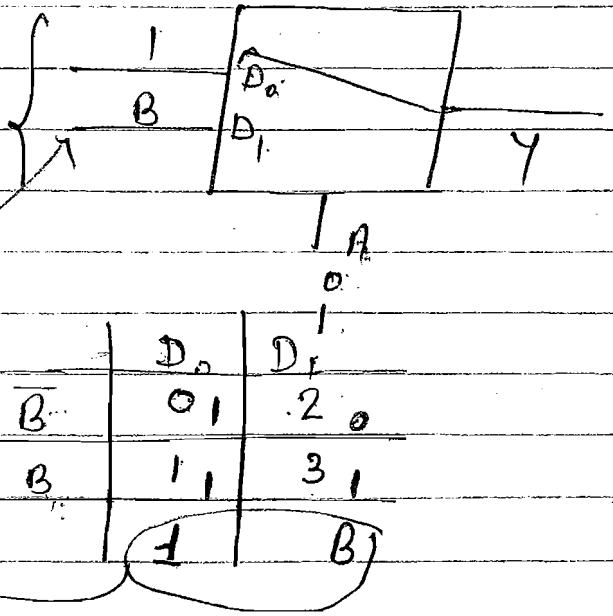
Implimentation of higher order function by using lower order Mux.

Ques Impliment $f(a,b) = \Sigma m(0,1,3)$ by using 4x1 mux. and 2x1 mux.

Soln



For 2x1 mux:-



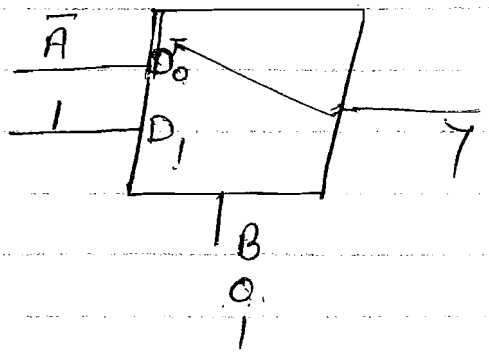
A	B
0	0
0	1
1	0
1	1

Ques Impliment $f(a,b) = \Sigma(0,1,3)$ by using 2x1 mux by select line B.

Here value of A=0 so it is 0 no. box in $\bar{A}$
Again when B=1 then rotatory switch goes to D_1, here value of A=0 so it will fill in $\bar{A}$ and it is 1 no. box

A	B
0	0
0	1
1	0
1	1

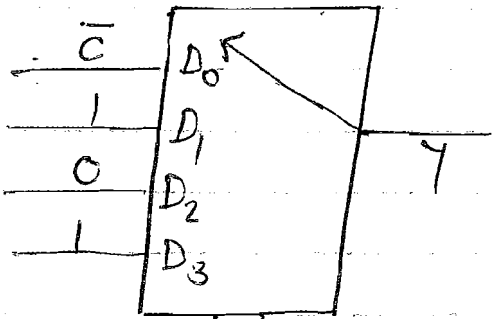
Soln



	D_0	D_1
$\bar{A}$	0,	1,
A	2,	3,
	$\bar{A}$	1

Qus For the given function $f(a,b,c) = \Sigma m(0,2,3,6,7)$ impliment the function by using 4x1 Mux.

Soln



	A	B
0 ←	0	0
1 ←	0	0
2 ←	0	1
3 ←	0	1
4 ←	1	0
5 ←	1	0
6 ←	1	1
7 ←	1	1

	C
0 ←	0
1 ←	1
2 ←	0
3 ←	1
4 ←	0
5 ←	1
6 ←	0
7 ←	1

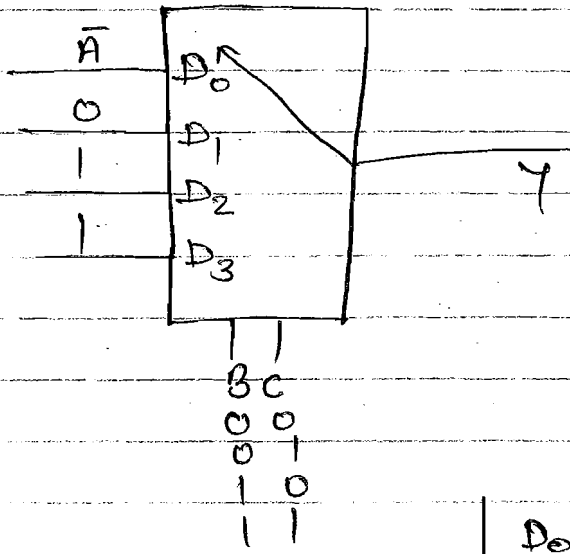
	D_0	D_1	D_2	D_3
$\bar{C}$	0,	2,	4,	6,
C	1,	3,	5,	7,
	$\bar{C}$	1	0	1

- **Note :-**

Either substitute 1 in the required box or incircle the desired number is also 1.

Ques Repeat the previous ques use BC be the select line.

Soln

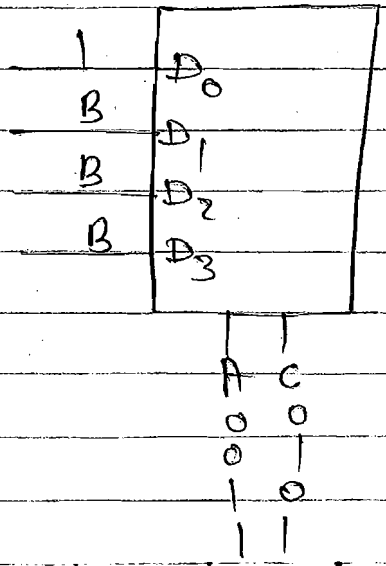


A	B	C	
0	0	0	→ 0
0	0	1	→ 1
0	1	0	→ 2
0	1	1	→ 3
1	0	0	→ 4
1	0	1	→ 5
1	1	0	→ 6
1	1	1	→ 7

	D_0	D_1	D_2	D_3
$\bar{A}$	0,	1,	2,	3,
A	4,	5,	6,	7,
	0	0	1	1
	$\bar{A}$	0	1	1

Ques Repeat the same ques us AC be the select line.

Soln

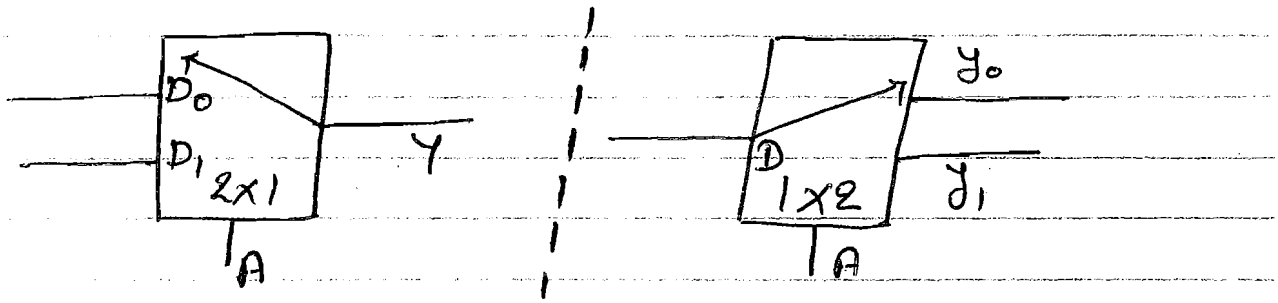


A	B	C	
0	0	0	→ 0
0	0	1	→ 1
0	1	0	→ 2
0	1	1	→ 3
1	0	0	→ 4
1	0	1	→ 5
1	1	0	→ 6
1	1	1	→ 7

	D_0	D_1	D_2	D_3
$\bar{B}$	0	1	4	5
B	2	3	6	7
	1	B	B	B

* De-Mux :-

The outer surface of the De-Mux is the mirror image of Mux. The internal structure of De-Mux is equivalent to Decoder.

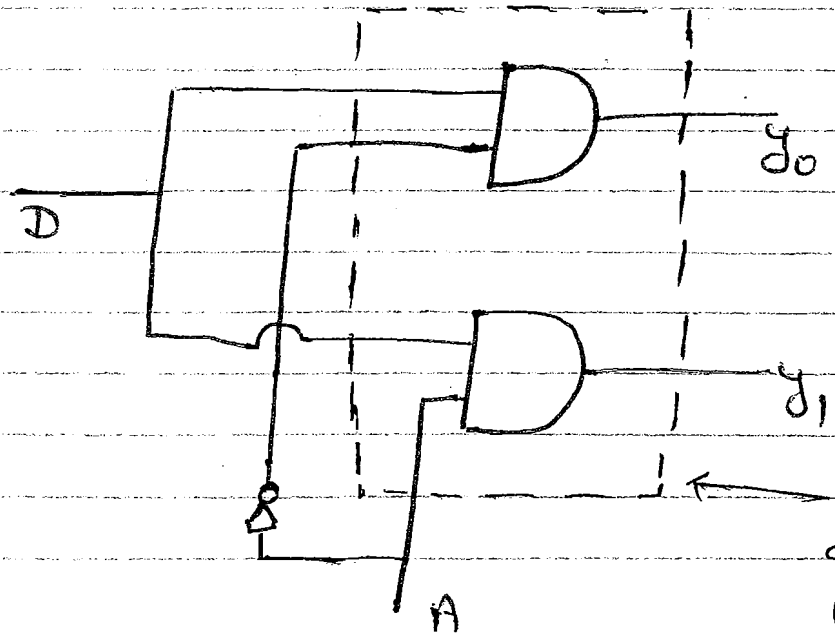


Mux | De-Mux

$$(y_0)_{SOP} = \bar{A}D$$

$$(y_1)_{SOP} = AD$$

D	y_0	y_1
0	D	0
1	0	D



← Internal Structure of De-Mux contains only AND gate.

1x4 $\xrightarrow[2+1=3]{}$ 1x2 Demux

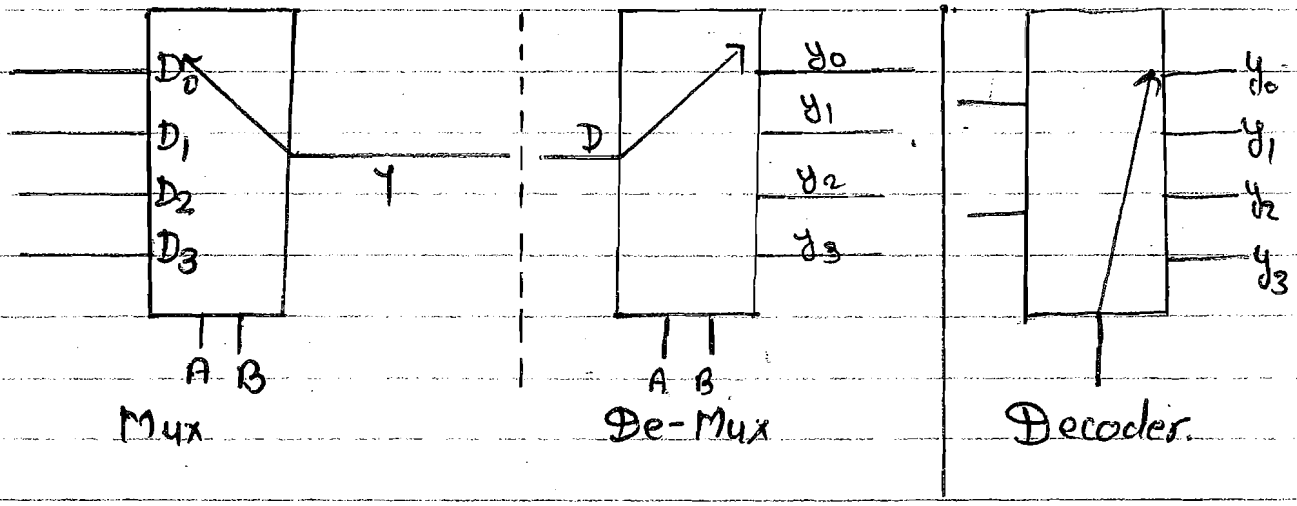
1x16 $\xrightarrow[4+1=5]{}$ 1x4

Imp for Gate

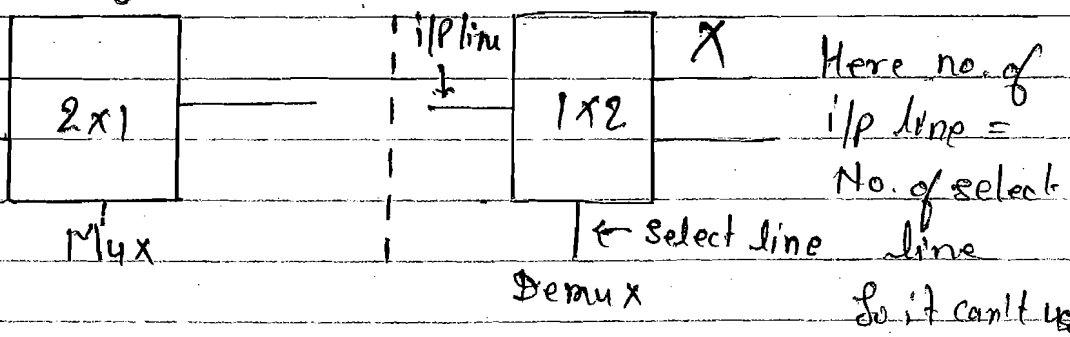
* Decoder :-

The I.C. developed for decoder can be used as De-Mux because internal structures are same.

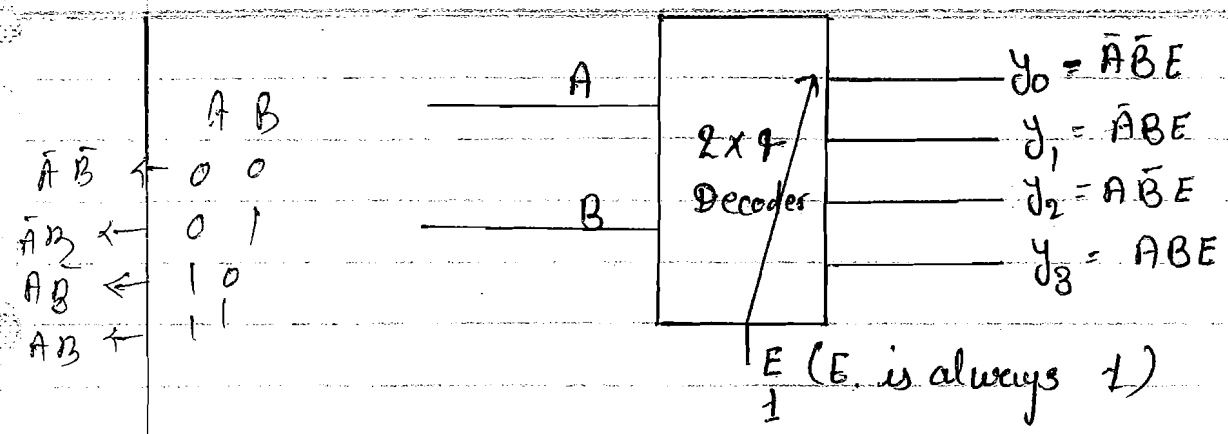
A De-Mux can be exchanged into decoder by interchanging input lines and select line provided the number of input lines should not be equal to number of select line.



We can't construct 1x2 DeMux because in 1x2 Demux no. of input lines = no. of select line.



- Therefore the lowest possible decoder is 2x4 decoder.



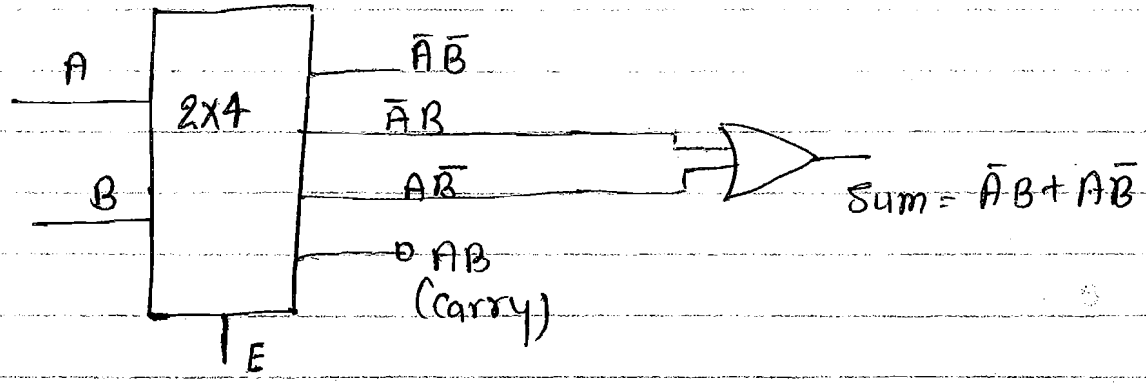
{ 2x4 Decoder }

Ques Impliment half adder by using 2x4 Decoder

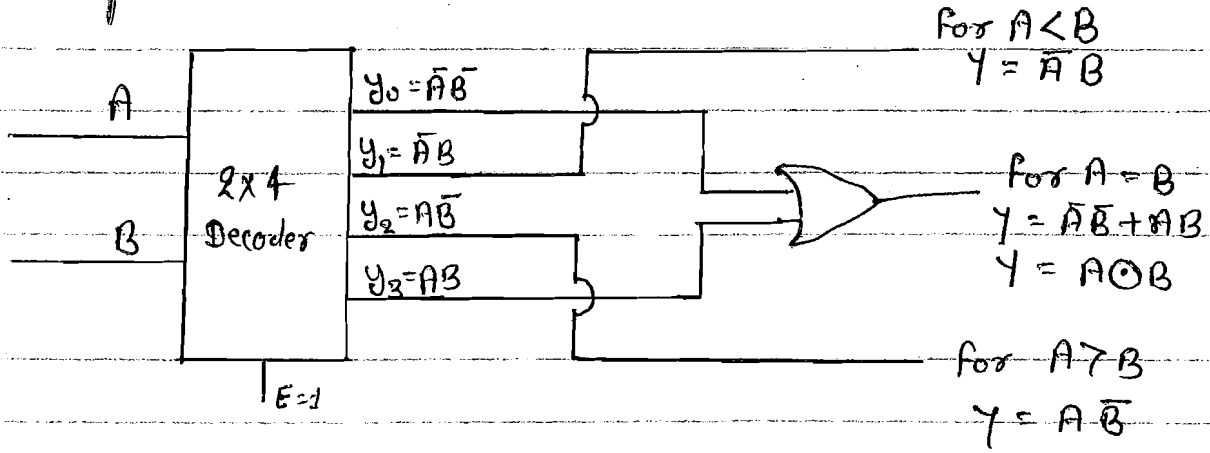
Sol^n

$$\text{Sum} = A \oplus B = \bar{A}B + A\bar{B}$$

$$\text{Carry} = A.B$$



Ques By using 2x4 decoder impliment single bit comparator.

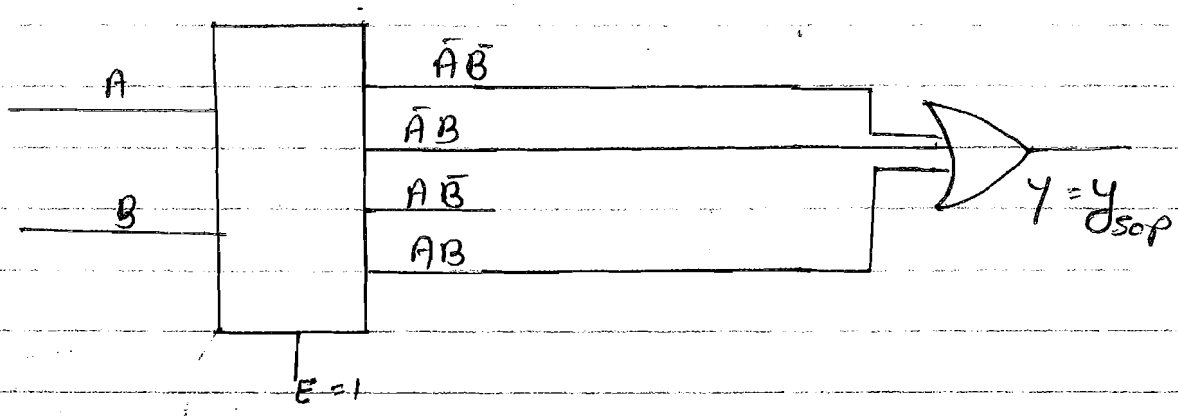


Ques By using 2x4 decoder implement the function $f(A,B) = \Sigma m(0,1,3)$.

Sol^n

A	B	Y	
0	0	1	$\rightarrow \bar{A}\bar{B}$
0	1	1	$\rightarrow \bar{A}B$
1	0	0	
1	1	1	$\rightarrow AB$

$$Y_{SOP} = \bar{A}\bar{B} + \bar{A}B + AB$$



- **Note :-**
  Decoder is non universal because external gates are used.

* **Order of Decoder :-**

Mux	Demux	Decoder
4x1	1x4	$2 \times 4 = 2 \times 2^2$
8x1	1x8	$3 \times 8 = 2 \times 2^3$
nx1	1xn	$n \times 2^n$

order of decoder.

$y_{carry} = AB + BC + AC = \bar{A}BC + AB\bar{C} + A\bar{B}C + ABC$

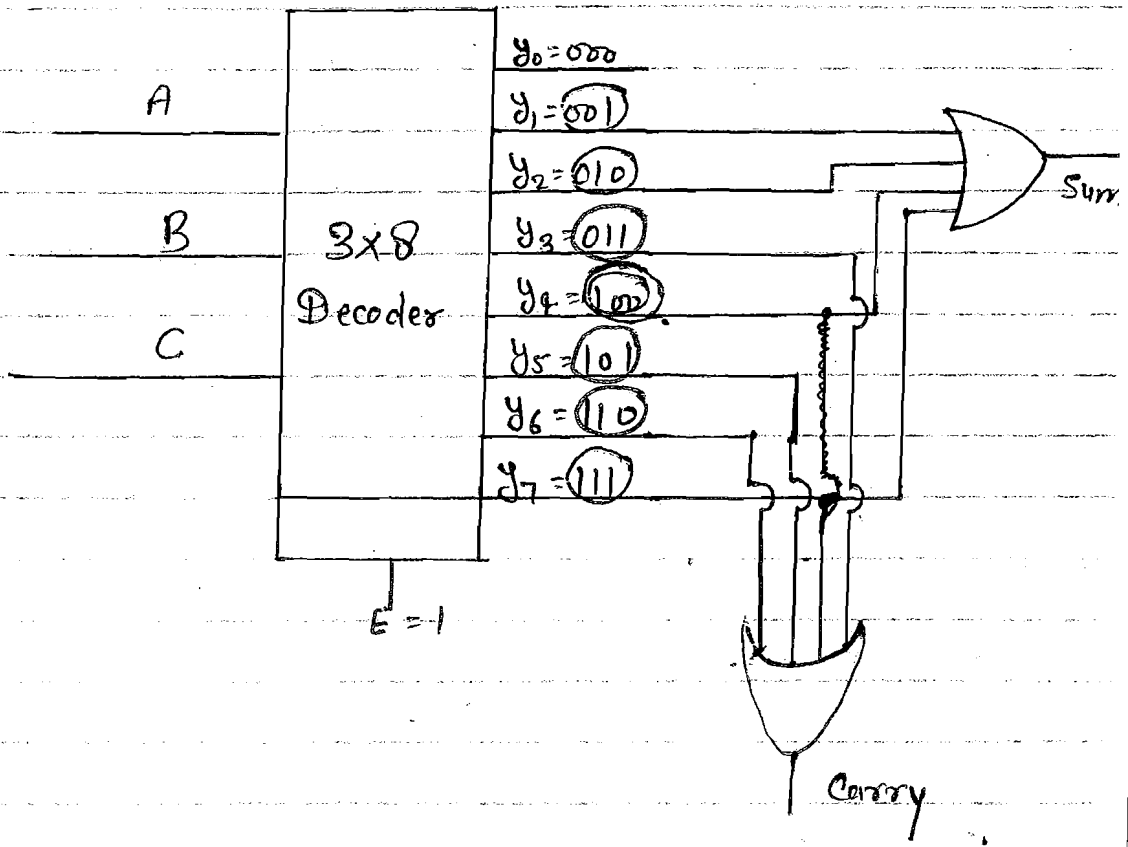
Full Subtractor

$y_{Diff.} = A \oplus B \oplus C = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$y_{Borrow} = \bar{A}B + \bar{A}C + BC = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$

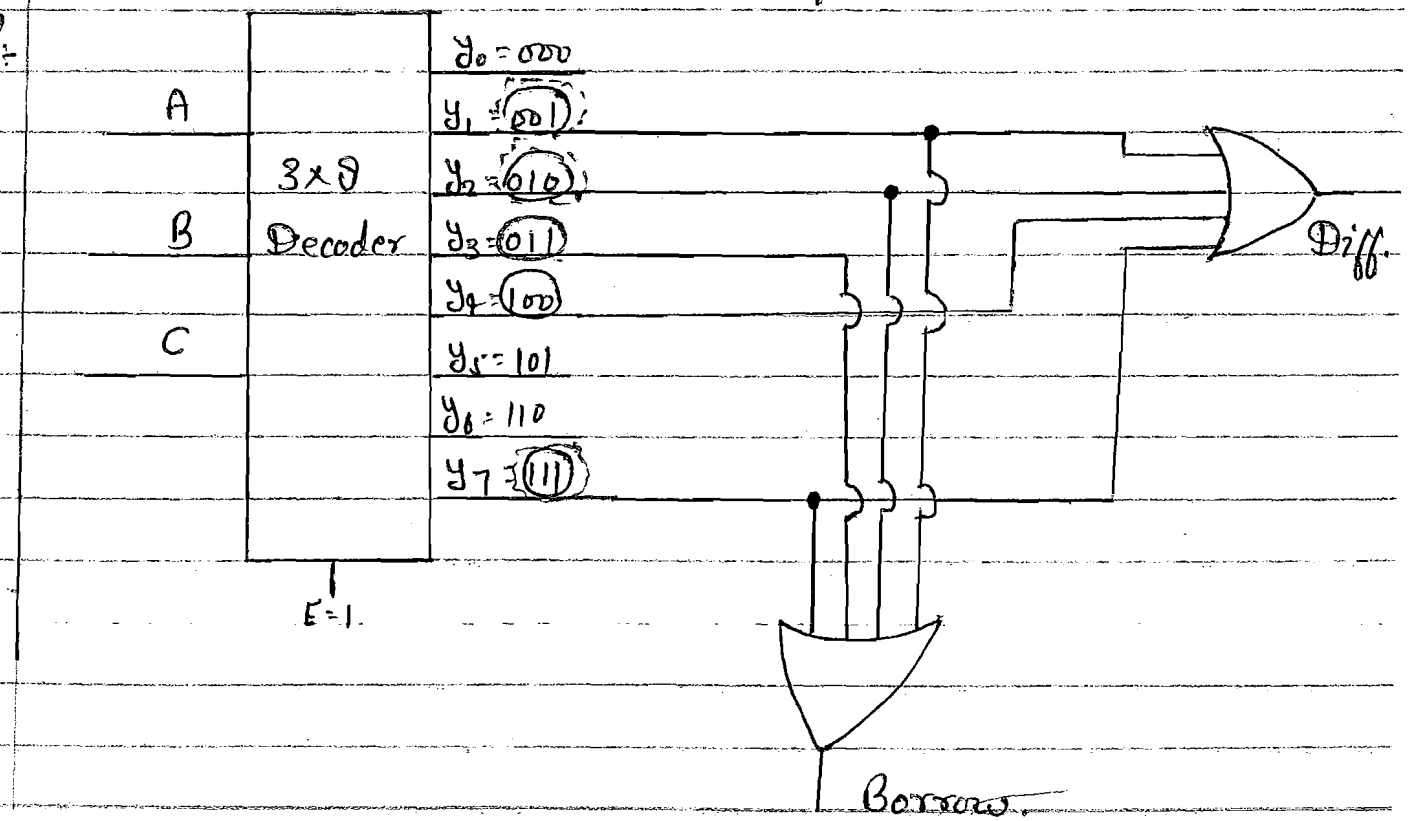
Ques Impliment full adder by using 3x8 decoder

Soln



Ques Impliment full subtrator by using 3x8 decode

Soln:-



05/Aug/2014

Codes

Gray Code :-

The outer boundary of K-map is designed on the basis of Gray Code.

- It is called unweighted code.

Weighted Code :-

If each and every bit is having significant positional value then such code is called as weighted code.

ex- (i) 8421
(ii) 5211
(iii) 3321

If each and every bit does not have significant positions such codes are called as unweighted code.

e.g. Gray Code, Excess-3 code.

- Gray Code is also called as unit distance code.
- Gray code is also called as cyclic code.

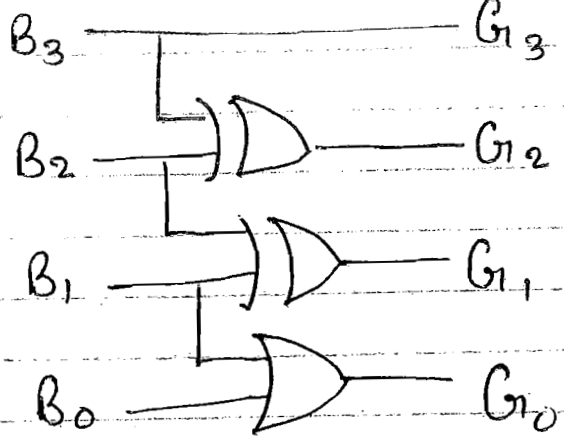
* Basic formation of Gray Code :-

B_3	B_2	B_1	B_0
1	1	0	1
G_3	G_2	G_1	G_0
1	0	1	1

In the binary to gray conversion M.S.B. written as it is and side by side ex-OR operation is perform (Sum is taken Carry is discarded)

B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0	
0 ⊕	0 ⊕	0 ⊕	0	0	0	0	0	← 1-bit difference so it is unit dis. code.
0 ⊕	0 ⊕	0 ⊕	1	0	0	0	1	
0 ⊕	0 ⊕	1 ⊕	0	0	0	1	1	
0 ⊕	0 ⊕	1 ⊕	1	0	0	1	0	

Circuit Diagram :-



(4-bit Binary to gray conversion)

- For n-bit binary to gray conversion the number of Ex-OR gate will be (n-1).
- Ex-OR follow Cyclic property.

e.g. $A \oplus B = C$

$1 \quad 0 \quad 1$

$B \oplus C = 1$

$0 \quad 1 = A$

$A \oplus C = 0$

$1 \quad 1 = B$

} So Ex-OR follow Cyclic property

Karnaugh Map / K-Map :-

It is also called as graphical representation of Boolean expression.

The disadvantage of Boolean Algebra (SOP & POS) is, it is applicable for 1 or 0 but K-map is applicable for 1 or 0 or X (d/ϕ) (don't care)

- K-map is applicable for 2-variable, 3-variable & 4-variable.

1. 2-Variable :-

A B
0 0 → 0
0 1 → 1
1 0 → 2
1 1 → 3

A \ B	0	1
0	0	1
1	2	3

2. 3-Variable :-

	A	B	C	
0 ←	0	0	0	
1 ←	0	0	1	
2 ←	0	1	0	
3 ←	0	1	1	
4 ←	1	0	0	
5 ←	1	0	1	
6 ←	1	1	0	
7 ←	1	1	1	

MSB, Ex-OR

A \ BC	00	01	10	11
0	0	1	3	2
1	4	5	7	6

3: 4-Variable :-

A B C D
0 0 0 0
⋮
1 1 1 1

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

Grouping of K-Map :-

Maximum size of grouping in the k-map will have maximum priority.

- In case of grouping the relation used is 2^n. Where n represents integers.

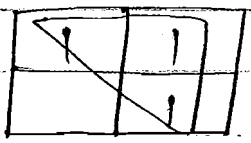
2^n $n = 0$, $2^0 = 1$ [individual] $\leftarrow$ min^m

$n = 1$ $2^1 = 2$ [Pair]

$n = 2$ $2^2 = 4$ [Quad]

[Maximum priority] $n = 3$ $2^3 = 8$ [Oct]

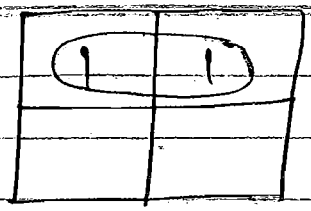
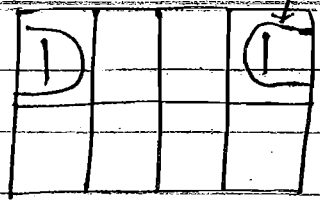
e.g. :-



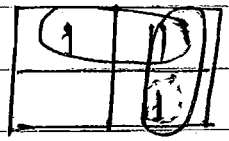
invalid.

* In case of k-map diagonal grouping is in-valid.

End grouping.

e.g :- ①  ② 

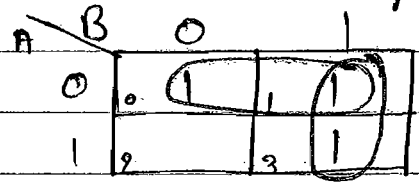
End grouping is valid in k-map.

③ 

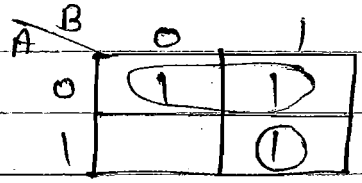
Note :-

In the k-map grouping the used value can be used repeated no. of times provided is condition is that, the no. of groups should not exceed as compared to previous.

Ques For the given function $f(A,B) = \sum m(0,1,3)$ find the minimise expression.

Sol^n 

$Y = \bar{A} + B$

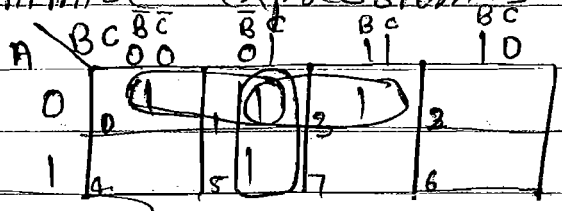


$\bar{A} + AB$

$(\bar{A}+A)(\bar{A}+B)$

$Y = \bar{A} + B$

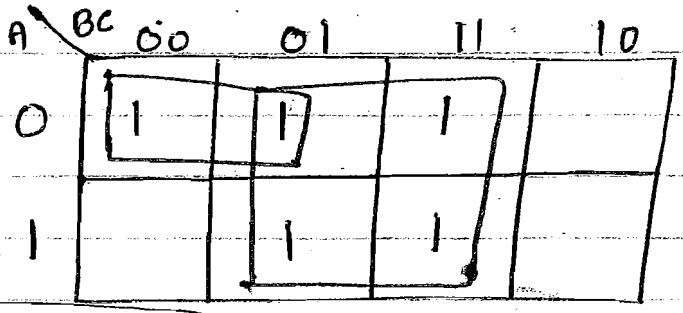
Ques For the given function $f(A,B,C) = \sum m(0,1,3,5)$ find the minimise expression.

Sol^n 

$Y = \bar{A}\bar{B} + \bar{B}C + \bar{A}C$

Ques for the given k-map find the output minimise expression.

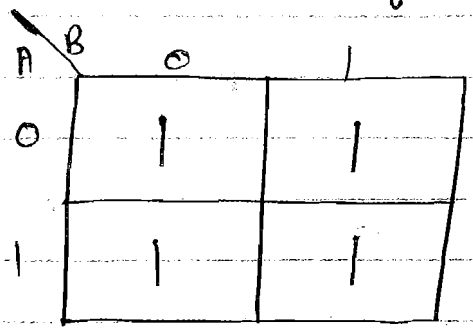
Soln



$Y = \bar{A}\bar{B} + C$

Ques for the given k-map find the o/p minimise expression.

Soln

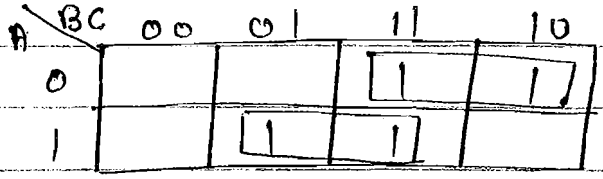


$f = 1$

If all boxes contains 1 then o/p = 1.
If all boxes contains 0 then o/p = 0
If all boxes contains X then o/p = X.

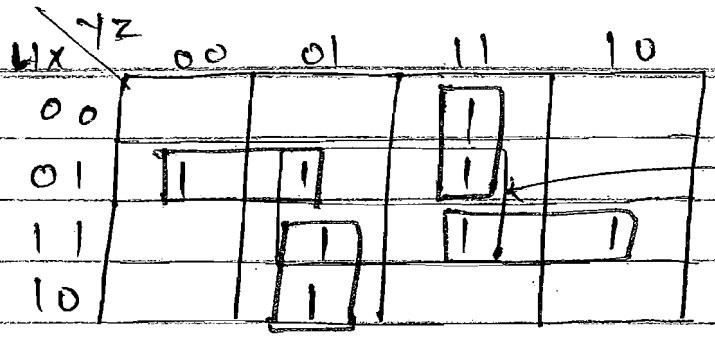
Ques for the given k-map find the o/p minimise expression.

Soln



$Y = \bar{A}B + AC$

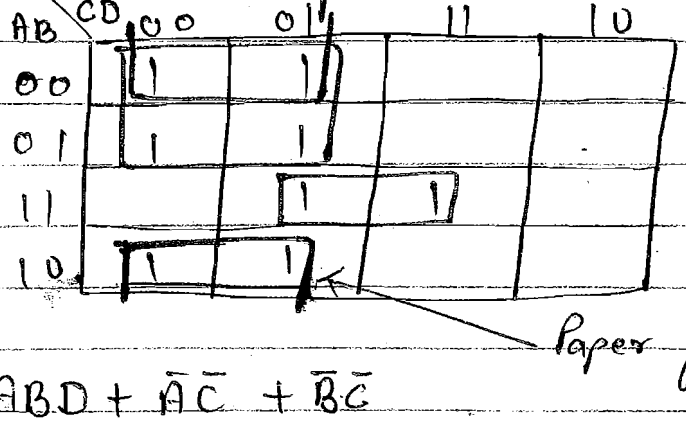
Ques for the given k-map find the minimise expression.



$$y = \bar{W}X\bar{Y} + W\bar{Y}Z + WX\bar{Y} + WXY$$

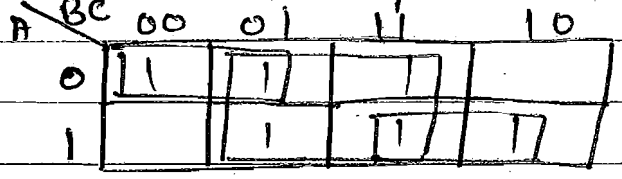
Ques Find the minimise expression

Sol^n



$$y = ABD + \bar{A}\bar{C} + \bar{B}\bar{C}$$

Ques Find the minimis expression.



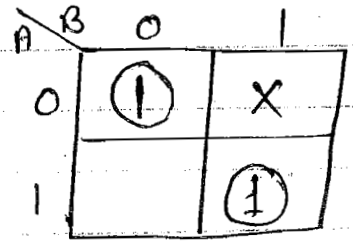
Sol^n

$$y = \bar{A}\bar{B} + C + AB$$

* Don't Care Condition :- [d, x, ϕ]

It is mainly used in counter design By using don't care the number of universal gate required reduces drastically.

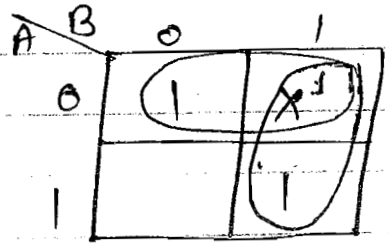
Don't care can be assumed as 1 or 0 bassed on the requirement.



$Y = \bar{A}\bar{B} + AB$

(Without don't care)

(max^n no. of gates required to construct)



$Y = \bar{A} + B$

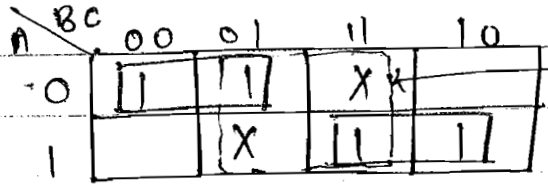
(With don't care)

(min^m no. of gates required to constru

AB	A ⊙ B	$\bar{A} + B$
0 0	1	1
0 1	0	1
1 0	0	0
1 1	1	1

Ques For the given K-map find the minimise expression.

Soln

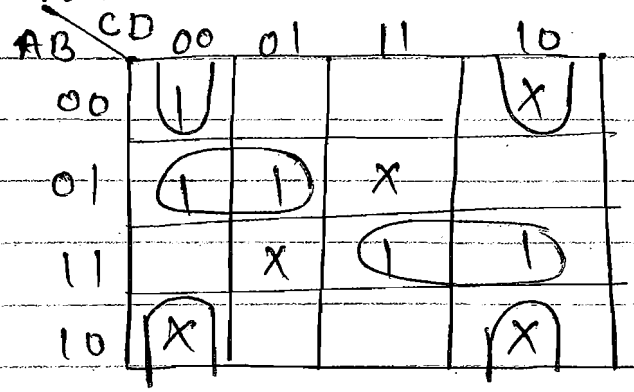


returned group.

$Y = \bar{A}\bar{B} + AB$

Ques For the given K-map find the minimise expression.

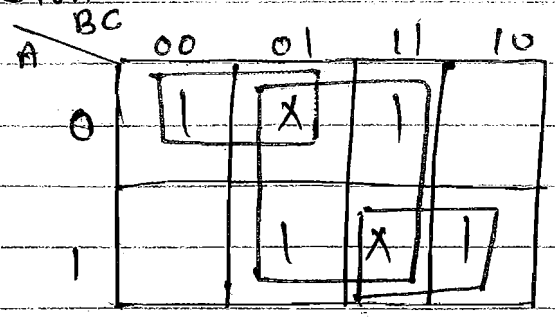
Sol^n



$$Y = \bar{A}B\bar{C} + ABC + B\bar{C}\bar{D}$$

Ques For the given K-map find the minimise expression.

Sol^n

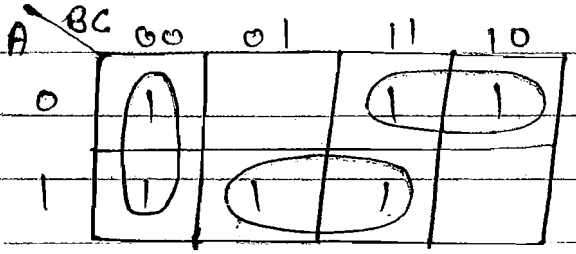


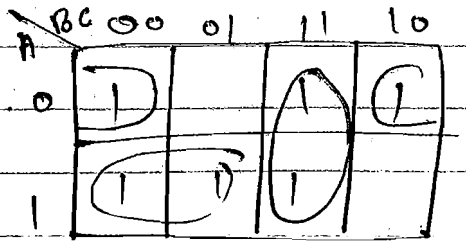
$$Y = C + \bar{A}\bar{B} + AB$$

Ques For the given K-map find the minimise expression.

A B C
0 1 0

$Y_1 = 1$
$Y_2 = 1$





$$Y_1 = \bar{B}\bar{C} + AC + \bar{A}B$$

$$Y_2 = BC + \bar{A}\bar{C} + AB$$

*(i) Implicant

(ii) Prime Implicant

(iii) Essential prime Impliment

for those k-map which produces multiple type of answers.

1. Implicant :-

It represents number of minterms or no. of 1's present in the k-map

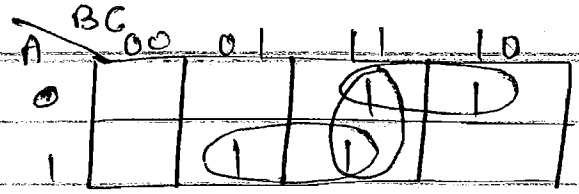
2. Prime Implicant :-

It is a product term formed by maximum possible grouping without failing priority.
And also include retundent group.

3. Essential prime Impliment :-

It is the part of prime implicant but excluded retundent group or if a single k-map produce multiple type of answers then the final ans is compare, the no. of common terms present in the final answer represent Essential prime implicant.

Qus Find Implicant, Prime Implicant and Essential prime Implicant for a given k-map.

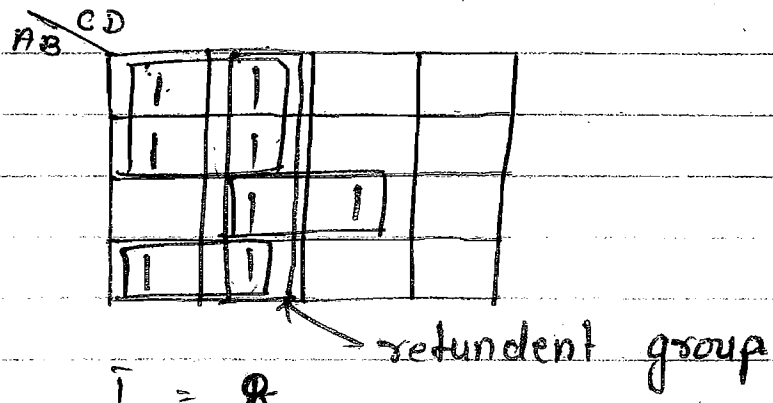


I = 4

P.I = 3

E.P.I = 2

(iii)



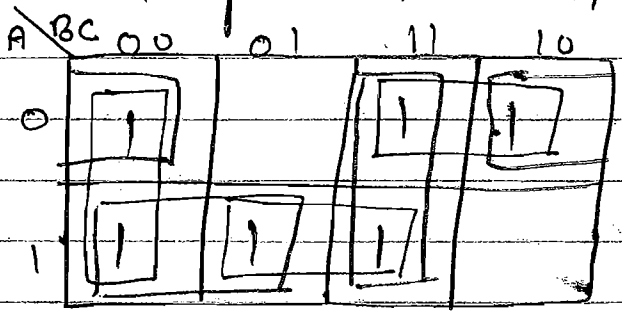
I = 8

P.I = 4

E.P.I = 3

Ques Find out the parameters I, PI, EPI.

Sol^n



I = 6

P.I = 6

E.P.I = 0

$y_1 = \bar{B}\bar{C} + AC + \bar{A}B$

$y_2 = BC + \bar{A}\bar{C} + A\bar{B}$

{ ∵ Here no common term in final ans.

Ques Find the parameters I, PI, EPI.

1	1	1
	1	1

$I = 5$

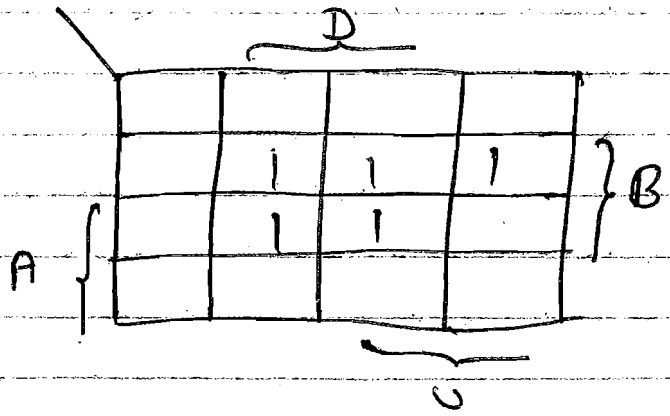
$PI = 2$

$EPI = 2$

Ques For the given function $f(A,B,C) = \pi M(2,4,6,7)$
find the k-map $= \Sigma m(0,1,3,5)$

Ques $f(A,B,C,D) = \pi M(2,3,6,7,10,11,12,14)$
$= \Sigma m(0,1,4,5,8,9,13,15)$

Ques For the given k-map

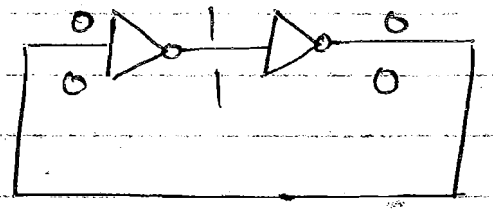


Sequential Circuit

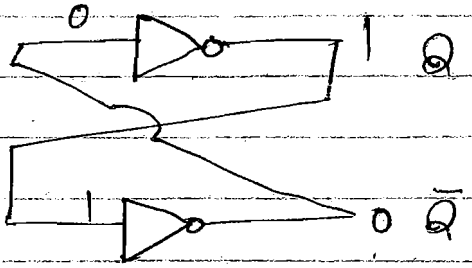
Flip-Flop :-

This is the basic memory element in the digital system. The basic flip-flop is also called Bistable multivibrator It is a single bit storage device. i.e it can store either 1 or 0.

A Flip-Flop can store indefinitely unless and untill the input conditions are changed.



Every Flip-Flop will have two output both will be compliment of each other.



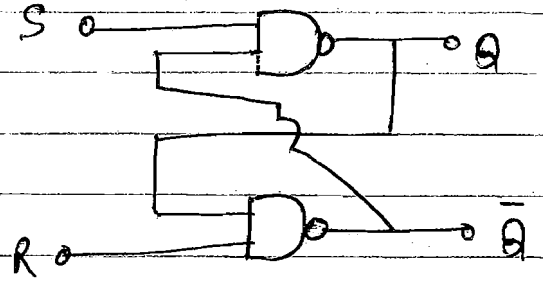
Every Flip-Flop will have cross-coupling in between input and output.

Types of Flip-Flop

1. Latch
2. S.R Flip-Flop
3. JK Flip-Flop
4. D-Flip-Flop
5. T-Flip-Flop

* Difference between Latch and Flip-Flop :-

* Replace every not gat by using NAND gate.



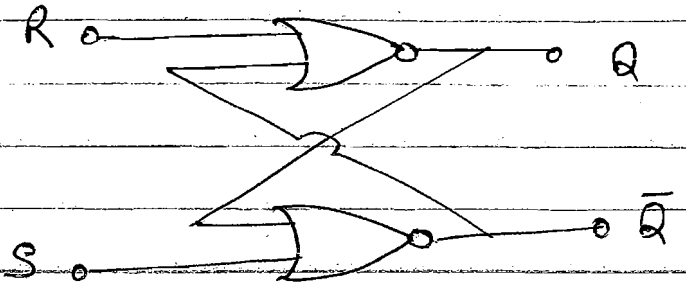
S-R Latch

Truth Table:-

S	R	Q
0	0	Invalid o/p
0	1	1
1	0	0
1	1	previous o/p.

Complementary S-R Latch :-

Replace every NAND gate by NOR gate and interchange either the position of S-R or Q & $\bar{Q}$

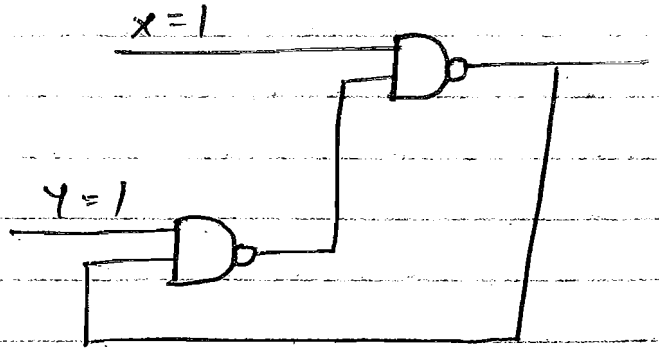


Truth Table :-

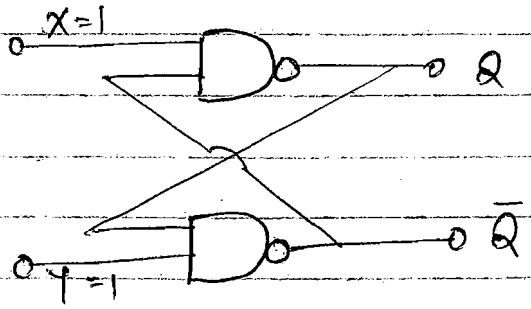
S	R	Q
0	0	Previous Output
0	1	0
1	0	1
1	1	invalid

S-R Flip-Flop :-

Ques Find the output Q for the given circuit.

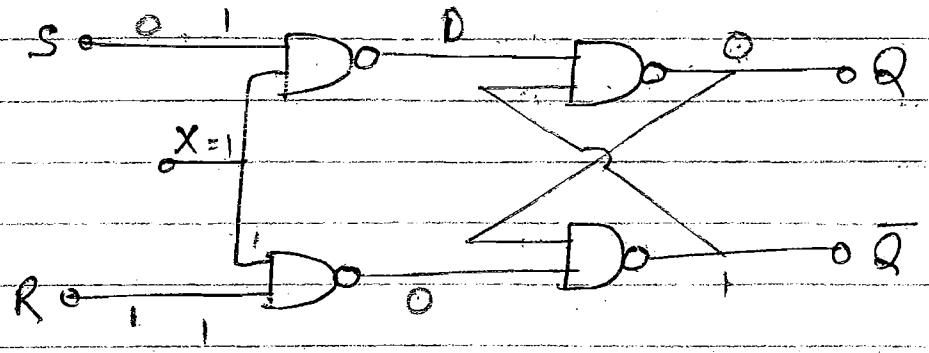


Soln :-



Previous o/p.

* S-R Flip-Flop :-



Truth Table :-

X	S	R	Q
0	X	X	Previous state
1	0	0	Previous state
1	0	1	0
1	1	0	1
1	1	1	Invalid

The disadvantage of SR-Flip Flop is when S=R=1 produces invalid output can't be use for practical applications.

Flip - Flop

- Characteristic Table (o/p Table)
- Charateristic Equation (o/p eqn)
- Exitation Table (i/p Table)

Characteristic Table :-

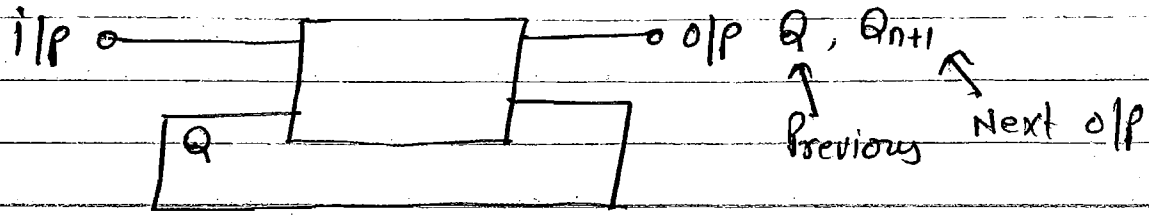
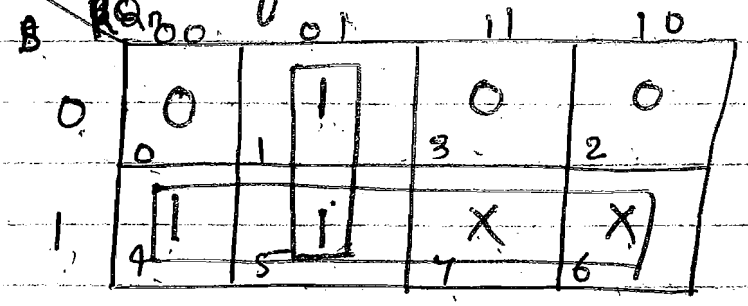


Table { Truth Table } :-

S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	X	0
0	1	X	0
1	0	X	1
1	0	X	1
1	1	0	X
1	1	1	X

* Characteristic Equation :-

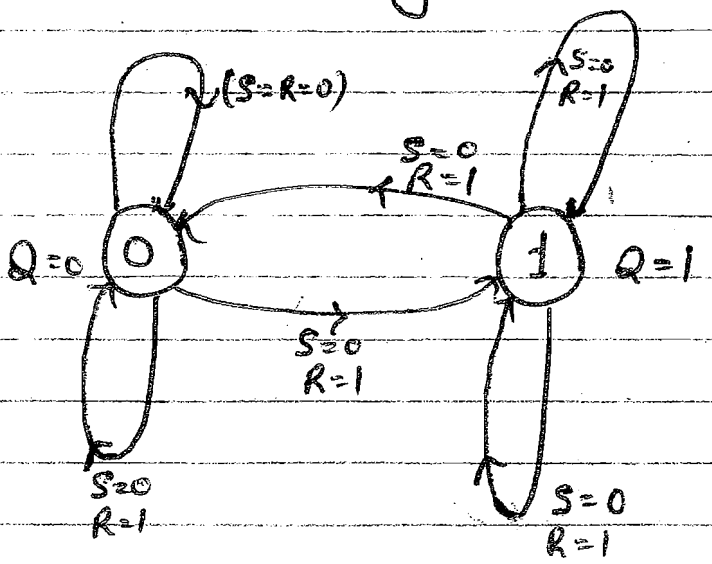


$$Q_{n+1} = S + \bar{R} Q_n \quad \text{---} \circledast \quad \{\text{remember}\}$$

* Exitation Table :-

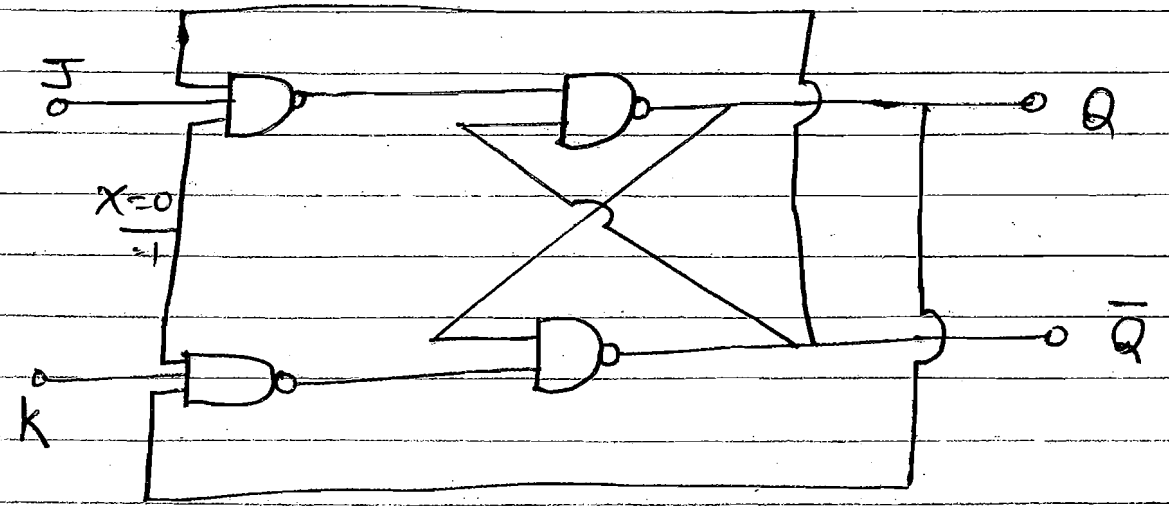
Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

* State Transition Diagrams :-



* The Disadvantage of S-R flip-flop is when S=R=1 produces invalid o/p hence replaced by J-K Flip-Flop.

* JK-Flip Flop :-



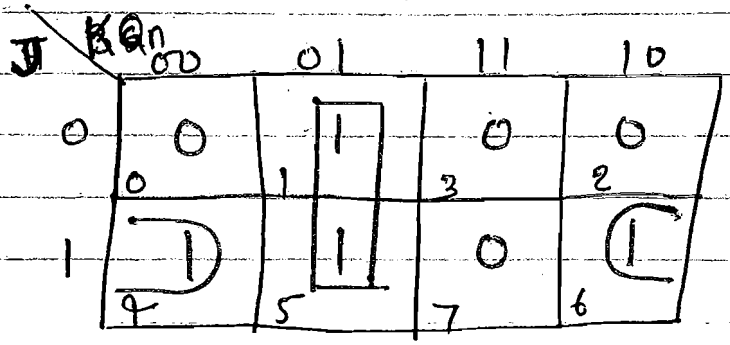
* Truth Table :-

X	J	K	Q
0	X	X	Prev.
1	0	0	Prev.
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}$

* Characteristic Table :-

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	X	0
0	1	X	0
1	0	X	1
1	0	X	1
1	1	0	1
1	1	1	0

* Characteristic Equation :-



$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

{Remember this}

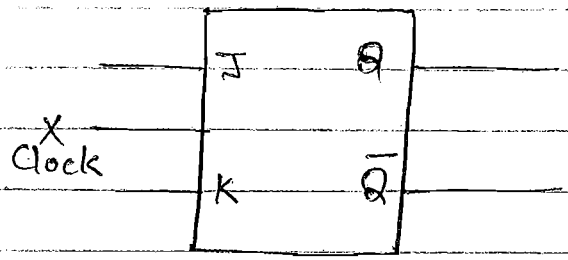
Ques | Draw the exitation table of Jk-Flip-Flop.

Soln

Q_n	Q_{n+1}	J	k
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

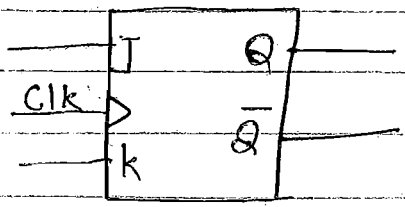
Note :- Jk-Flip-Flop is also called as universal Flip-Flop.

Rectangular box of J-K flip-Flop :-

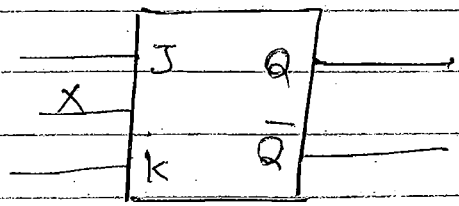


X → Clk works when X = 1
→ does not work X = 0

Meaning of X :- Clock which carry on the J.K Flip-Flop.



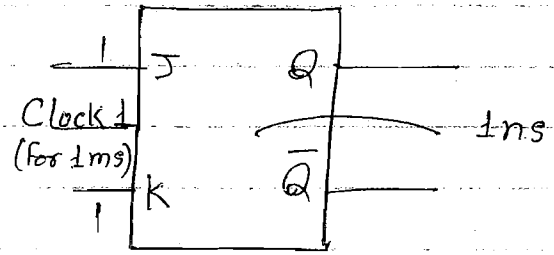
edge triggered Clock pulse

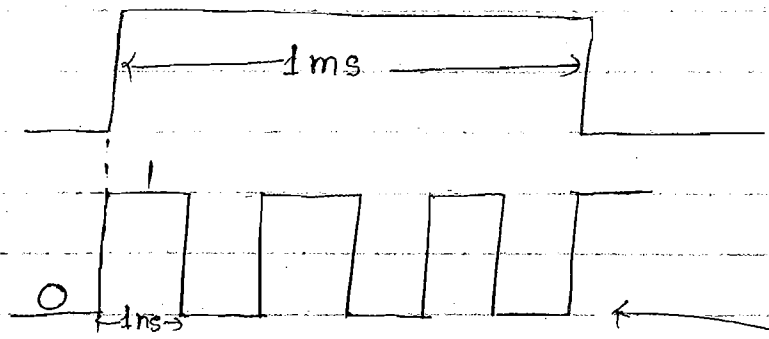


level triggered Clock pulse.

Output changes continuously under the clock pulse as input changes.

In the edge trigger clock pulse output will change either raising edge or falling edge. not both.

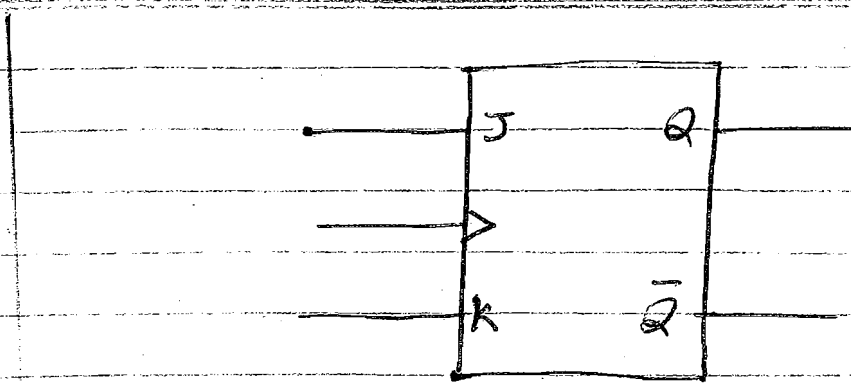


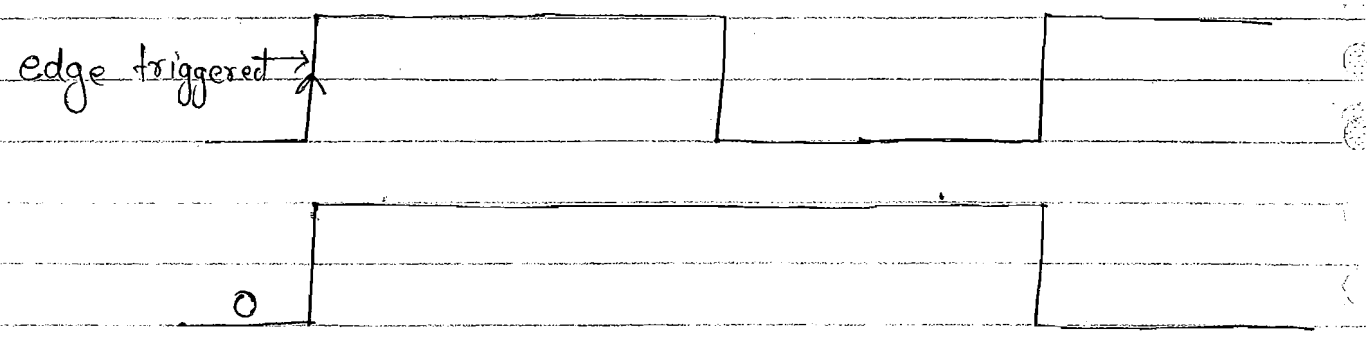


In the level triggered JK-flip-flop output changes many times under a single clock pulse for JK = 1 is called as **Race Arround Condition.**

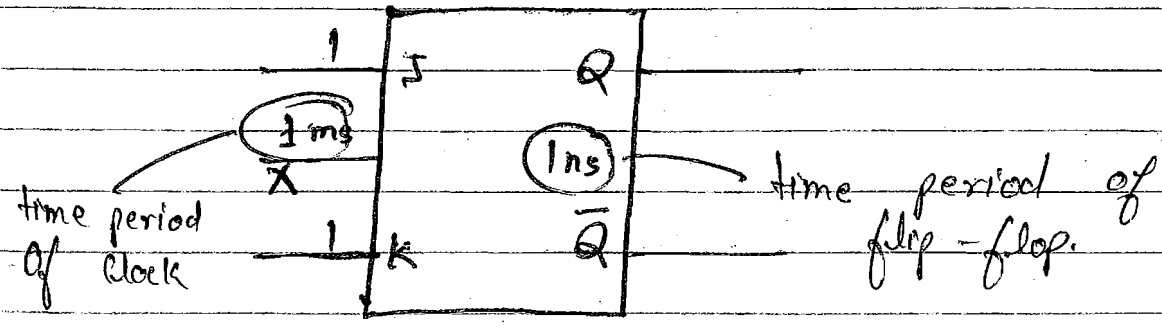
Race arround condition is the disadvantage of JK-flip flop.

* **Removal of Race Arround Condition:-**





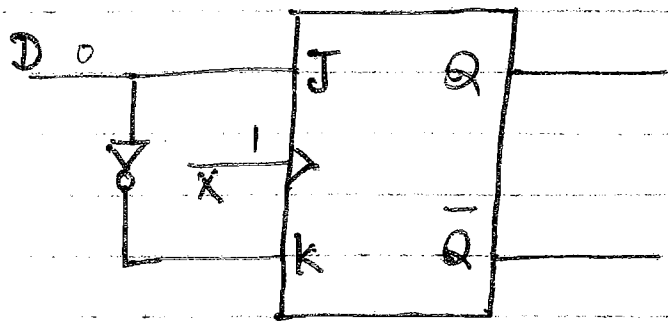
Race arround condition can be removed by using edge triggered clock pulse in place of level triggered clock pulse.



Race arround condition can be removed by reversing the condition $t_{pd\ clk} > t_{pd\ ff}$ to $t_{pd\ clk} < t_{pd\ ff}$.

To increase the time period of flip-flop cascading of flip-flop is performed for example Master slave flip flop is also useful for Race arround condition.

* D - Flip Flop :-



Truth table :-

X	D	Q
0	X	Previous
1	0	0
1	1	1

Characteristic Table :-

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Characteristic Equation :-

$$Q_{n+1} = D$$

D - flip-flop acts as a buffer.

⇒ D - flip-flop is useful for implimentation of registers.

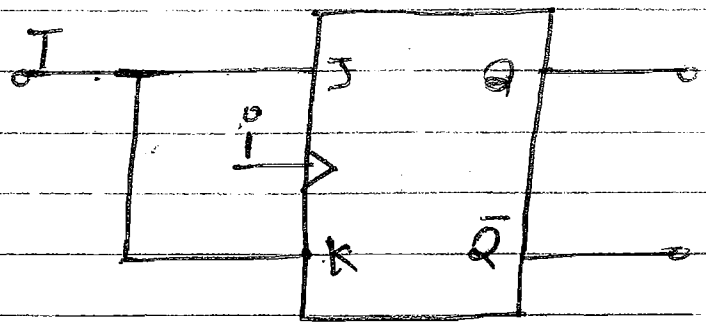
$= J\bar{Q}_n + \bar{K}Q_n$

$= D$

Excitation Table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

* T - Flip - Flop



Truth Table :-

X	T	Q
0	X	Previous State
1	0	Previous State
1	1	$\bar{Q}$

Characteristic Table :-

T	Q_n	Q_{n+1}
0	0	Previous (0)
0	1	1
1	0	1
1	1	0

Characteristic Equation :-

$$Q_{n+1} = T \oplus Q_n$$

Exitation Table :-

Q	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T-Flip Flop perform ex-OR operation.

* Point To be Remember :-

Characteristic Eqn :-

① SR $Q_{n+1} = S + \bar{R} Q_n$

② JK $Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$

③ D $Q_{n+1} = D$

④ T $Q_{n+1} = T \oplus Q_n$

* Exitation Table :-

Q_n	Q_{n+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

For X = 1

J	K	Q
0	0	Previous
0	1	0
1	0	1
1	1	$\bar{Q}$

For X = 1

S	R	Q
0	0	Previous
0	1	0
1	0	1
1	1	X

* Registors :-

Mainly implimented by D flip-flop.

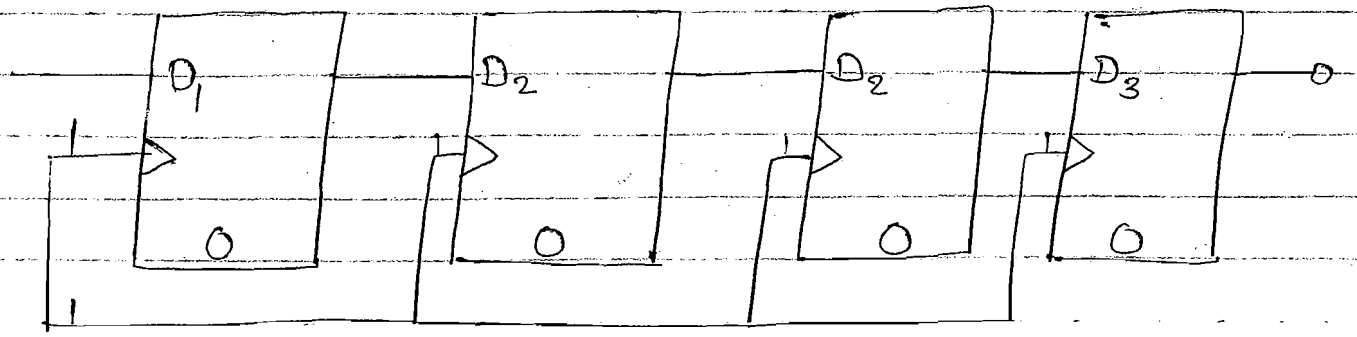
To store n number of bit, n flip-flops are require { because one flip-flop stores only 1 bit either 0 or 1 }.

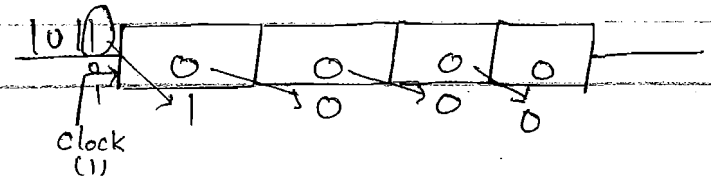
Based on input and Output Registors are Classified as -

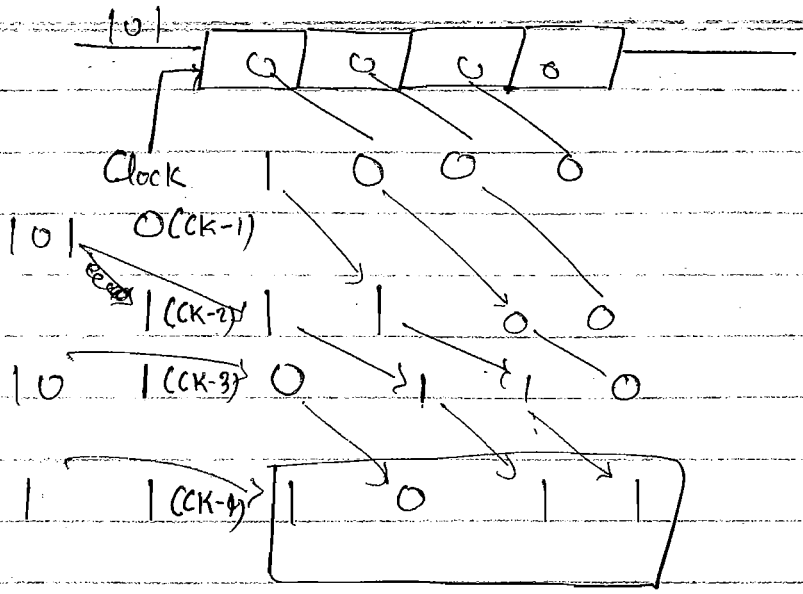
1. Serial input Serial Output Register [SISO]
2. Serial input Parallel Output Register [SIPO]
3. Parallel input Parallel Output Register [PIPO]
4. Parallel input Serial Output Regrster. [PISO]

1. Serial input Serial Output Registor [SISO] :-

{ 4-bit SISO } :-

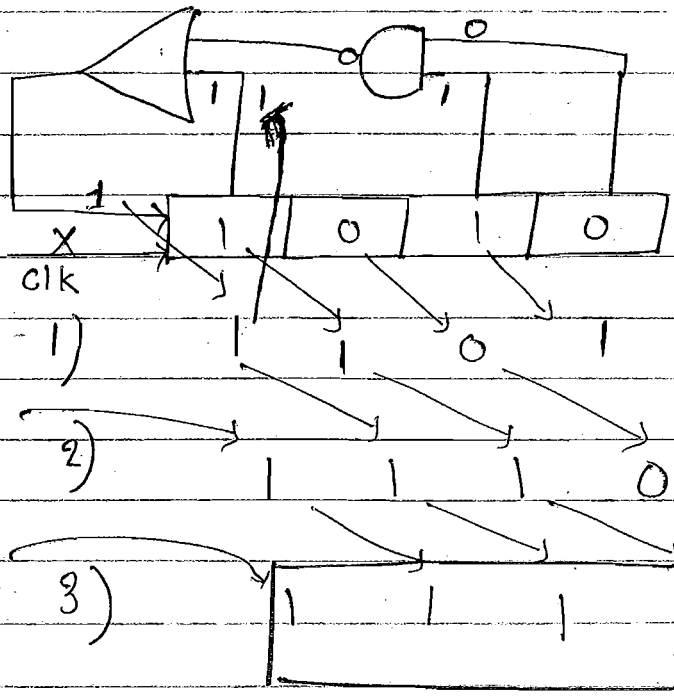






for n bit serial register for input storage n - clock pulse are required.

Ques For the given circuit diagram identify the content after three clock pulse.

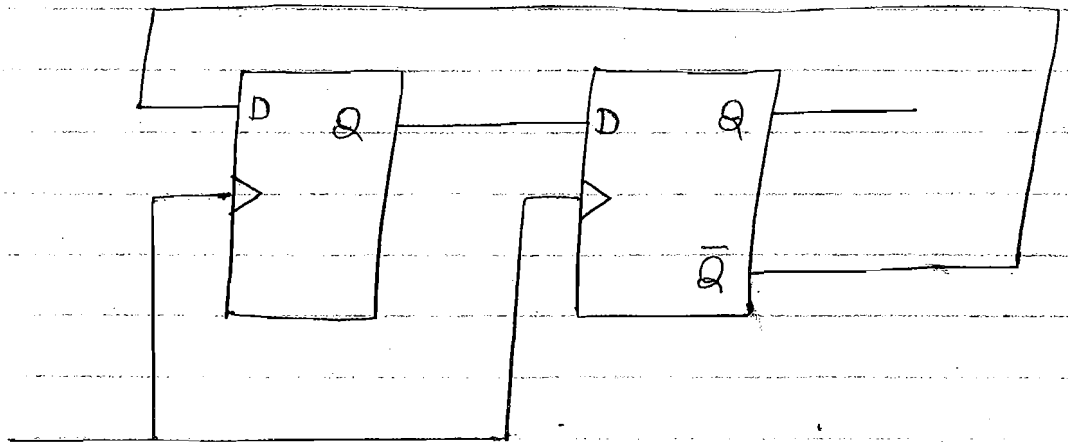


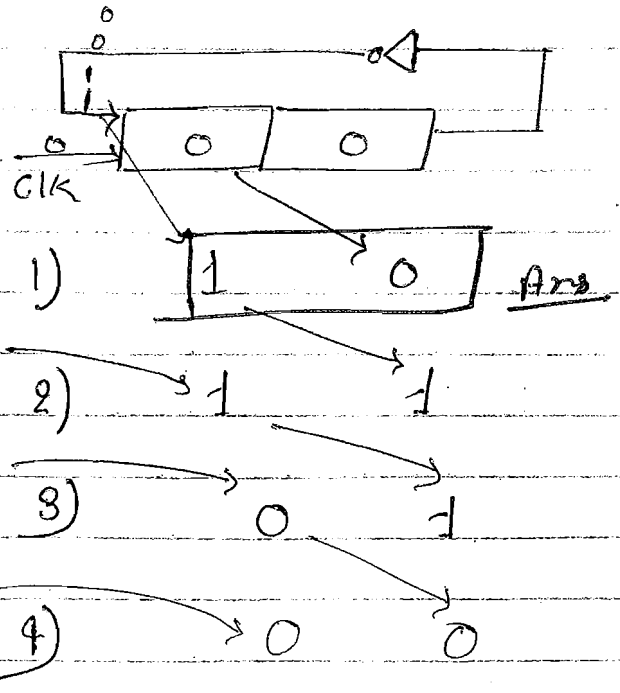
Soln

This the content after three clk pulses.

Ques for the given circuit diagram find the content after 333 clock pulse.

Sol^{n}





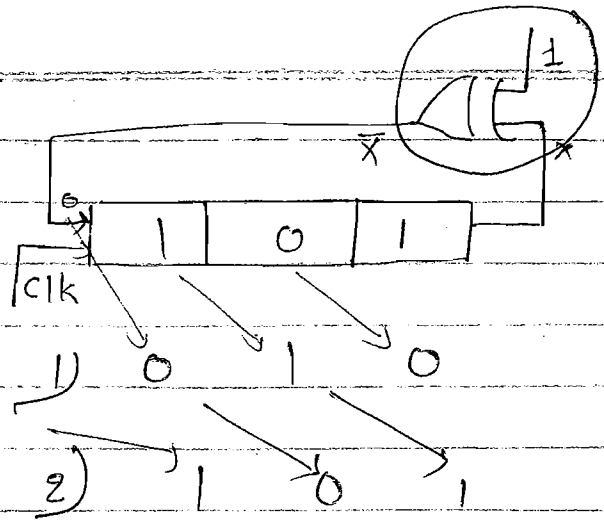
$$\begin{array}{r} 83 \\ 4\overline{)333} \\ 32 \\ \hline 13 \\ 12 \\ \hline 1 \end{array}$$

So after 83 clk we find 0 0 there for it mean previous state

So after 333 clk pulse we find 10 as fist o/p.

2. for the given circuit find the content after 332 clk pulse.

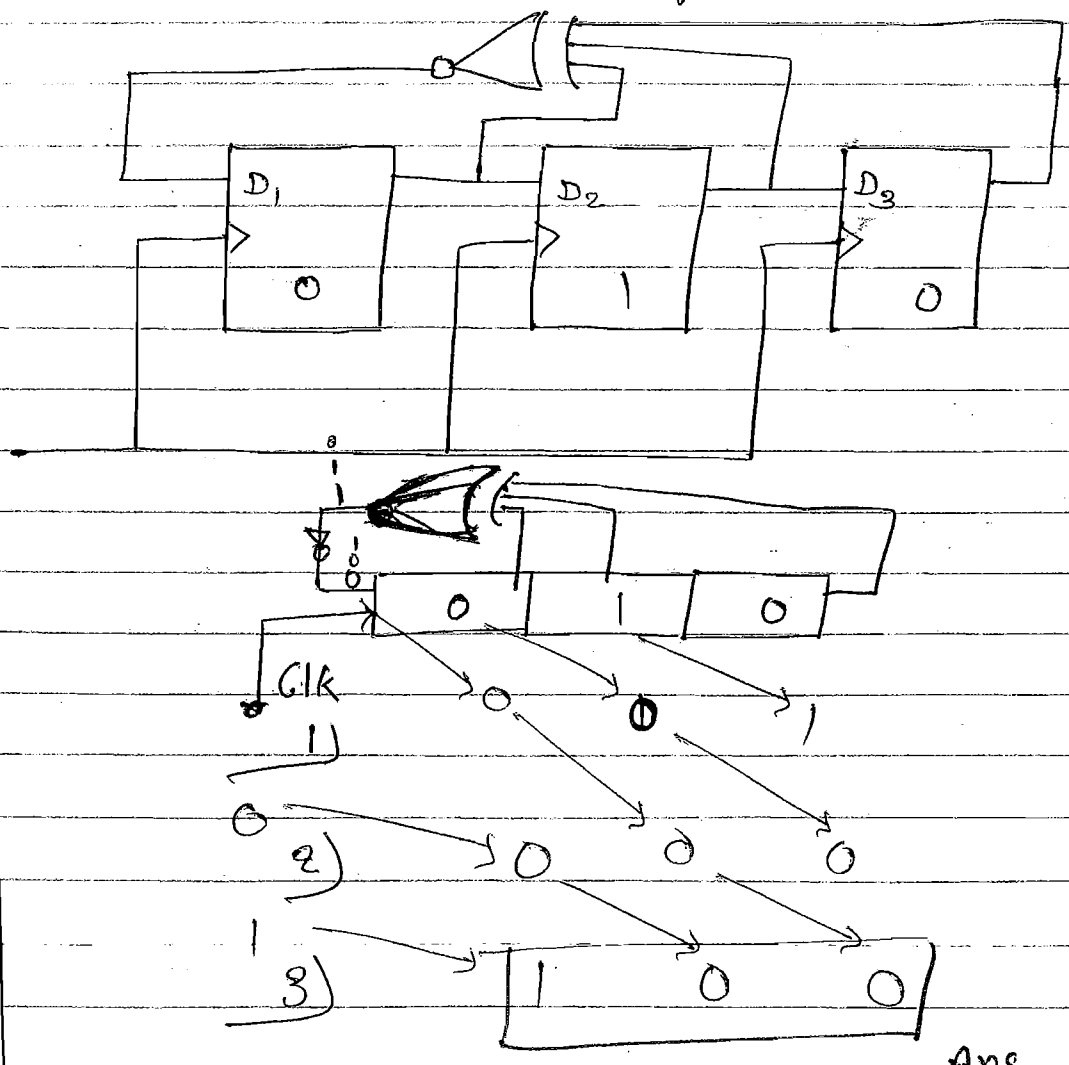
It is like a not gate.



So after two step we reach previous state so after 332 clk we get 101.

Q. Find the content after 3 clock pulse.

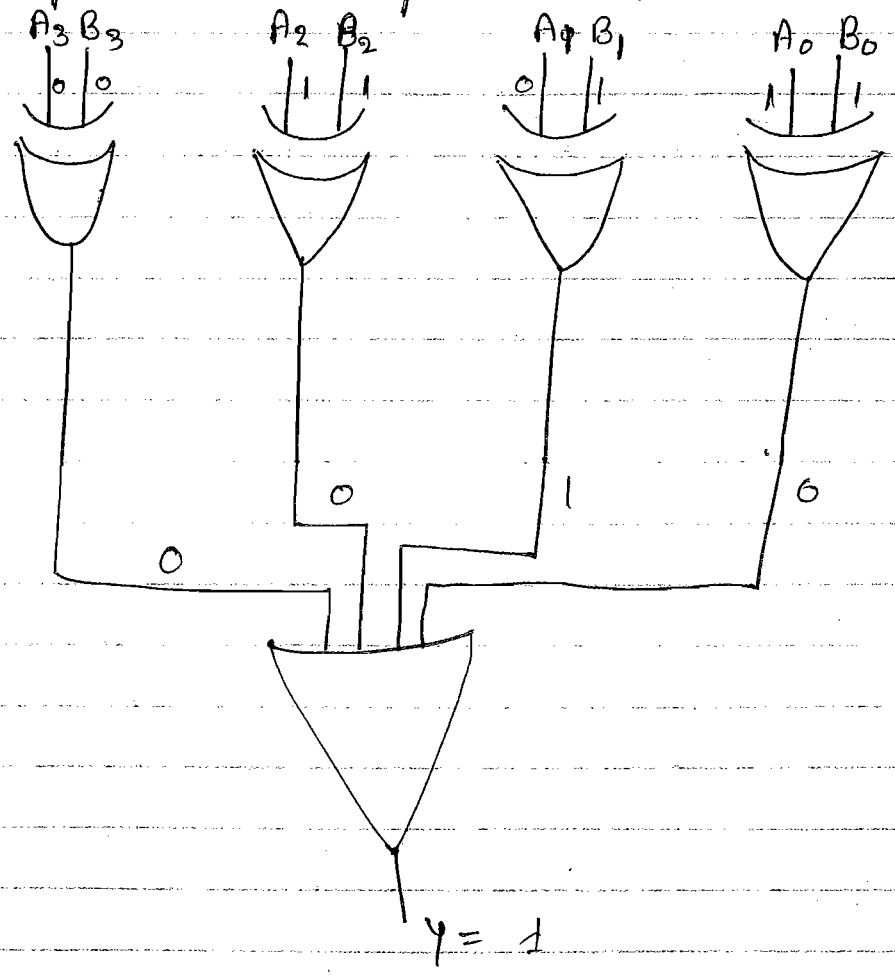
Soln



Ans

Qus for the given circuit diagram identify for which of the following combination of i/p produces high output.

Soln



	A_3 A_2 A_1 A_0	B_3 B_2 B_1 B_0
(a)	1 0 1 0	1 0 1 0
(b)	0 1 0 1	0 1 0 1
(c)	0 0 1 1	0 0 1 1
(d)	0 1 0 1	0 1 1 1 [✓]

Q. For the given circuit diagram determine the content after 3 clock pulse.

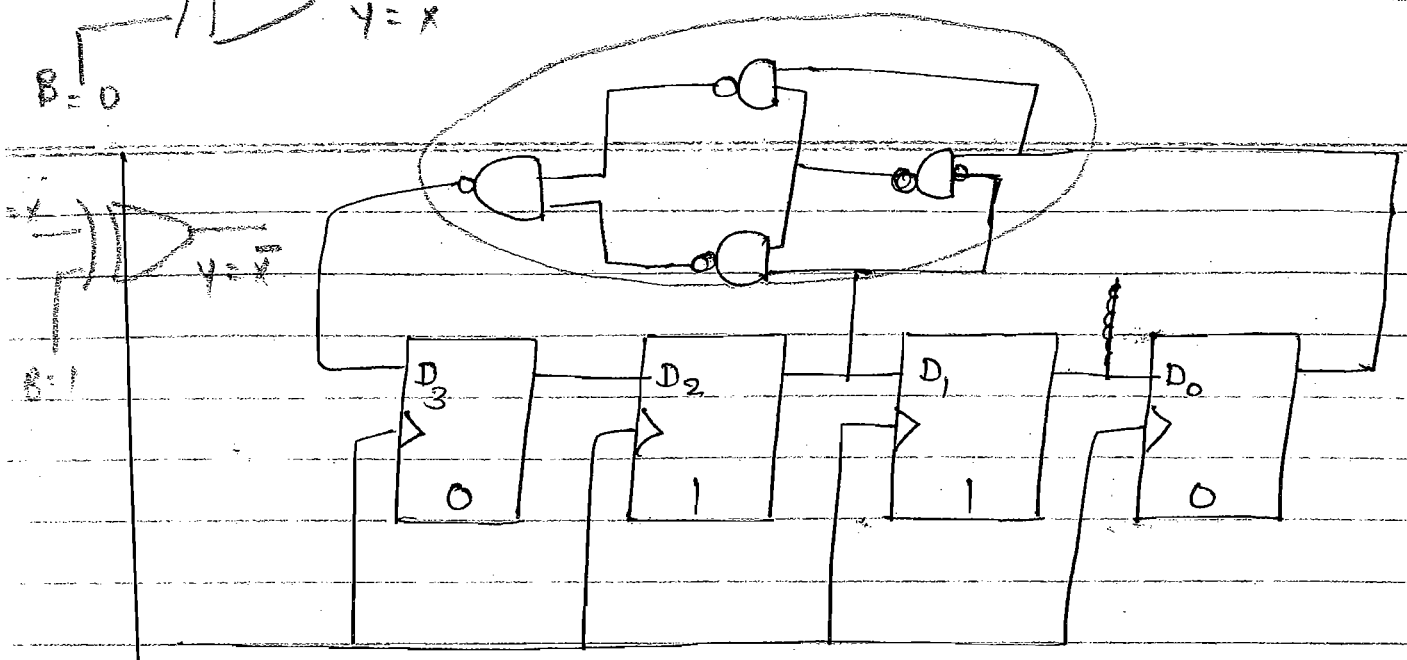
Soln

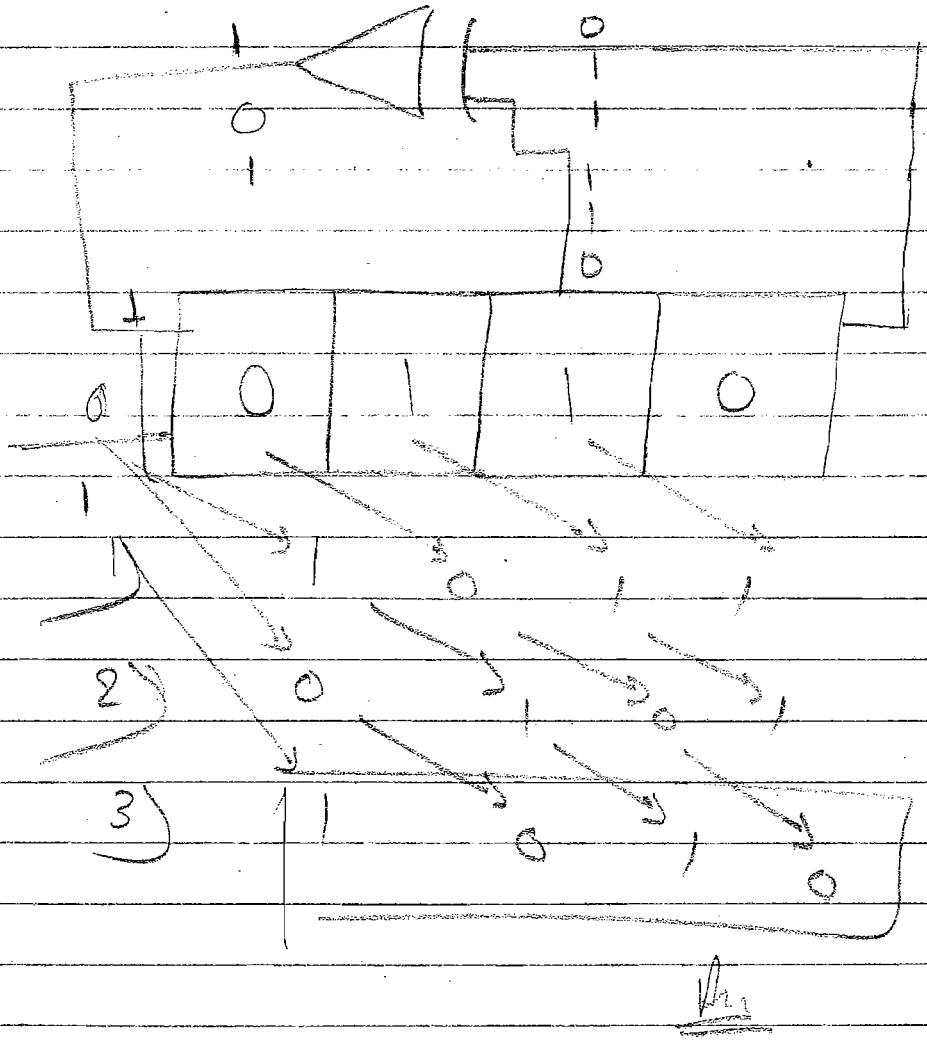
A = X

B = 0

Y = X

X – ОК – чипе = $A\bar{B} + \bar{A}B = A \oplus B$





* **Counters :-**

These are used to count the number of clock pulses.

- These are used to measure the width (time period) of the clock pulse.
- These are used to measure the freqeuncy of clock pulse.
- These are used biomedical applicatim (ECG)
- These are used in the radar applicatim.
- These are used in the timer ll circuit.

Counters are basically classified as-

1. Assynchronous Counter [Slow]
2. Synchronous Counter [Fast]

* **Classification between Assynchronous and Synchroneus Counter :-**

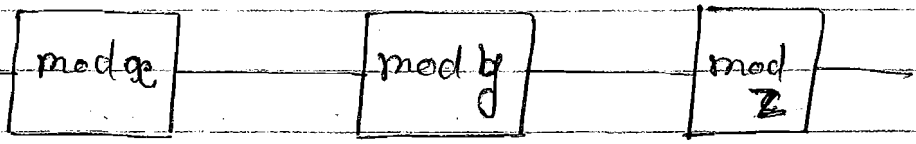
	Assynchroneus	Synchronous.
•	In the assynchroneus counter only one flip-flop is applied by external clock pulse. Rest, every flip-flop having clock pulse applied by previous F.F.	All the flip-flops are applied by same clock pulse.
•	Delay is present (slow)	• Delay is not present (Fast.

• Decoding error present.	• No decoding error
• Only up (increasing ↑) or down (decreasing ↓) Count is possible	• Any count sequence is possible.
• It is also called as Ripple Counter.	• Ex - Ring / Johnson Counter.
• Only JK or T Flip-Flop is used.	• Any Flip-Flop is used

* ~~Asynchronous Counter~~

* **Modulus of a Counter :-**

Mod of a counter represents number of state counted by counter.

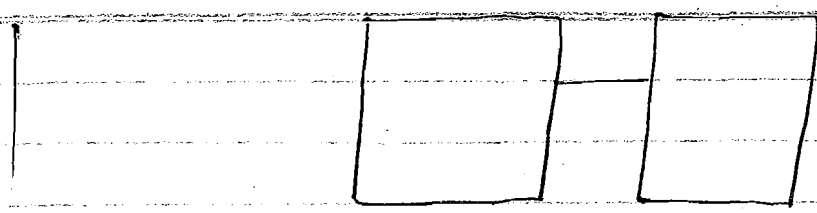


over all mod = xyz

If the counters having mod x, mod y, mod z are cascated, then overall mod is xyz.

Qus A mod 78 counter can be implimented by -

(a) 6 number of mod 6 counter
(b) 13 number of mod 6 counter
(c) A mod 13 & a mod 6 counter [✓]
(d) 13 mod of mod 13 counter.



0 0
0 1
1 0
1 1

mod (4) → 2^{2} ← no. of flip-flo

mod 8 :- $2^{(3)}$ ← No. of flip-flop

mod 16 :- $2^{(4)}$ ← No. of flip-flops.

no of mod → $N = 2^{(n)}$ → no. of flip-flops.

$\Rightarrow N = 2^n$

$\log N = \log 2^n$

$\log_2 N = n \log_2 2$

$\boxed{n = \log_2 N}$ $\{ \because \log_2 2 = 1 \}$

OR

$\boxed{n \geq \log_2 N}$

mod 8 = 3 flip flop

mod 7 = ? 3 flip-flo

2 = 4 (too less)

3 = 8

Counters

9/Aug/2014

1. These are used to count the number of clock pulses.
2. These are used to measure the width (time period).
3. These are used to measure the frequency of clock pulse.
4. These are used in biomedical

* Asynchronous Counter :-

In the asynchronous counter only one flip-flop will be applied by external clock, that flip-flop will be haves as Least Significant Bit (L.S.B). The adjacent flip-flop will behaves as - M.S.B.

clk ← Q
↓
down Counter

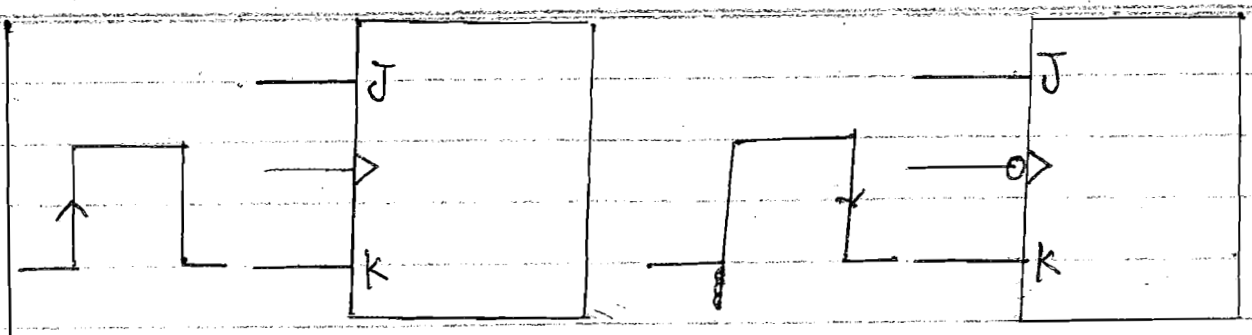
clk ← $\bar{Q}$
↓
Up Counter

for e.g. :- MOD 4

0 0
0 1
1 0
1 1

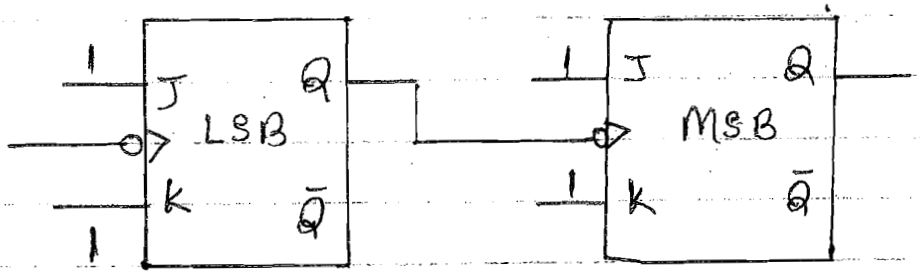
For the asynchronous counter design J-K or T flip-flop are used with applied input is equal to 1.

Mod-4 Up-Counter :-



Mod-4 Up Counter by using J-K Flip-Flop:-

Mod 4 = 2^2 ⇒ No. of FF required = 2.



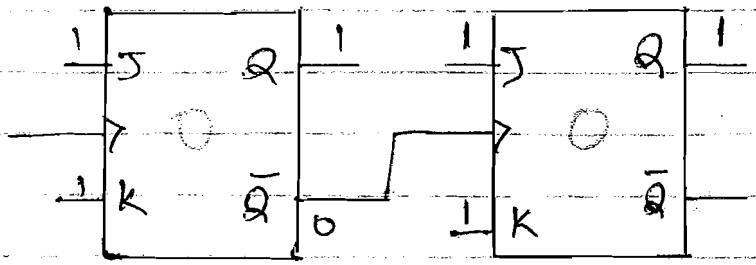
Clk			
	(X)	0	0
	(1)	1	0
	(2)	0	1
	(3)	1	1
	(4)	0	0

When J=1, K=1 then $Q = \bar{Q}$

⇒ Initial state will be equal to final state if no. of mod equal to no. of clock pulse.

Ques Design a Mod-4 up counter by using +ve edge triggered flip-flop.

Sol^n

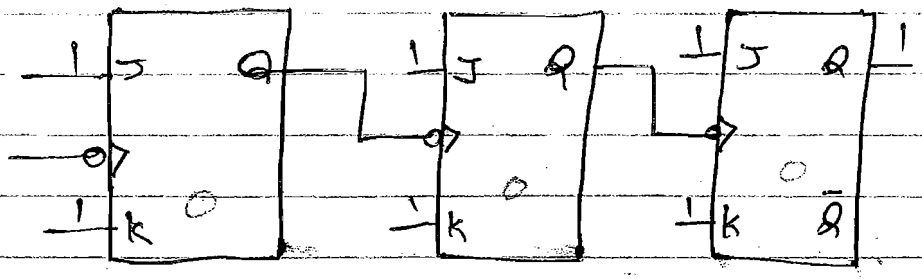


Clock (x) 0 ↓ 0 ↓
(1) 1 ↓ 0 ↓
(2) 0 . 1

Ques Design a Mod-8 up counter by using negative edge triggered J.K f.f.

Sol^n

Mod 8 = 2^3 { req. ff = 3 }

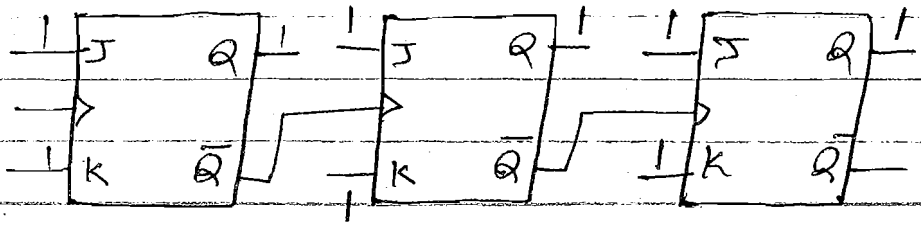


CLK

(X) 0 ↓ $\xrightarrow{\bar{Q}}$ 0 ↓P 0 ↓P
(1) 1 ↓ 0 ↓P 0 ↓P
(2) 0 ↓ 1 0 ↓
(3) 1 ↓ 1 0
(4)

Q. Mod-8 up counter by using +ve edge trigger using J-K FF.

Sol^n

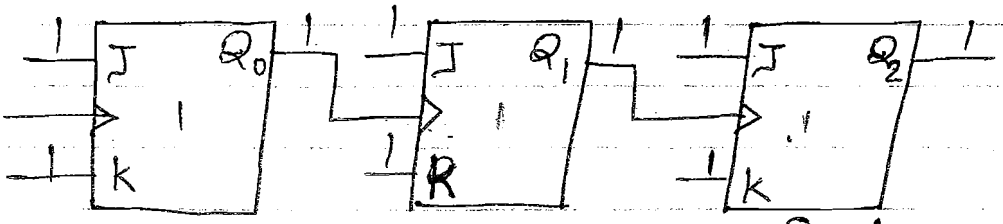


Clk	Q_2	Q_1	Q_0
(X)	0	0	0
(1)	1	0	0
(2)	0	1	0
(3)	1	1	0

Read Right to left.

Ques Design a Mod-8 down counter by using positive edge triggered?

Soln



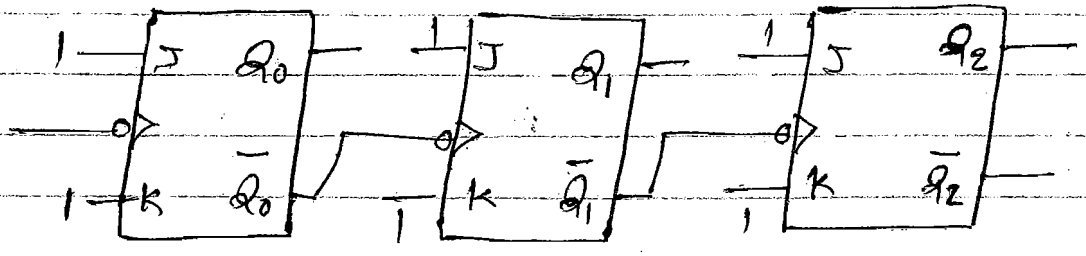
Clk	Q_2	Q_1	Q_0
(X)	1	1	1
(1)	0	1	1
(2)	1	0	1
(3)	0	0	1
(4)	1	1	0
(5)	0	1	0
(6)	1	0	0

See from

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Ques Design a Mod-8 down counter by using negative edge triggered J-K ff?

Soln



Clk	Q_2	Q_1	Q_0
(X)	1	1	1
(1)	0	1	1
(2)	1	0	1
(3)	0	0	1
(4)	1	0	0

down Counting.

Ques A Mod-8 and a Mod-4 counters are cascaded identify the number of flip-flop required?

(a) 4 (b) 5 ✓ (c) 6 (d) 7

Soln Total Mod = 8 × 4

= 32

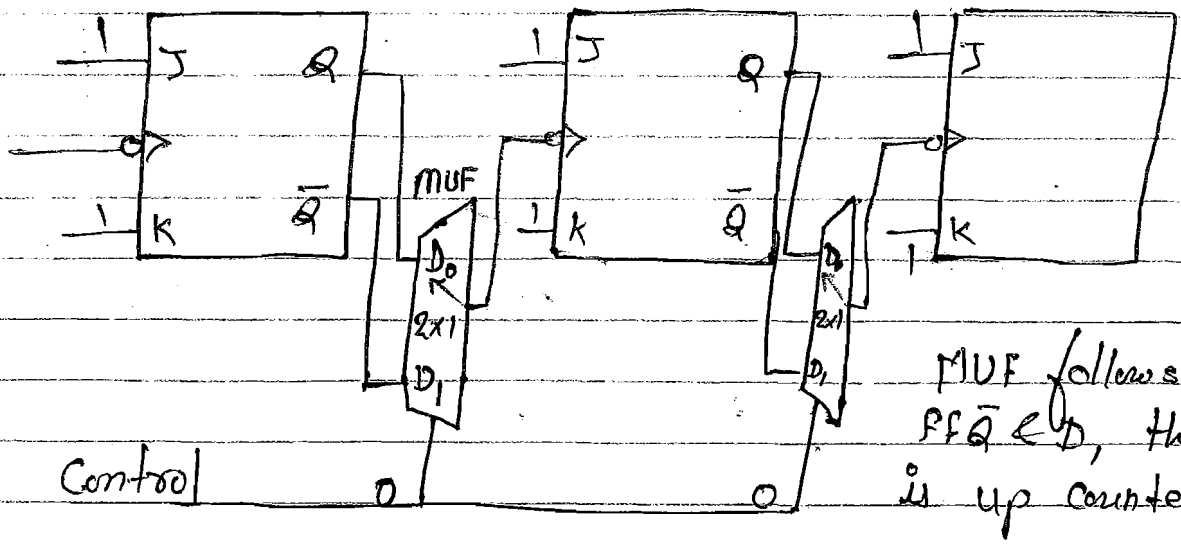
So $32 = 2^5$, Thus no. of flip-flop required = 5.

Ques Identify the Mod of counter for the given circuit diagram?

(a) Mod 32 Counter (b) Mod 16 Counter

(c) Mod 8 down Counter (d) Mod 8 up Counter ✓

Soln



* Reduction of State:-

To reduce the no. of count sequence from the actual sequence by using same no. of F.F. is called as reduction of state.

To reduce the no. of state preset & clear are used.

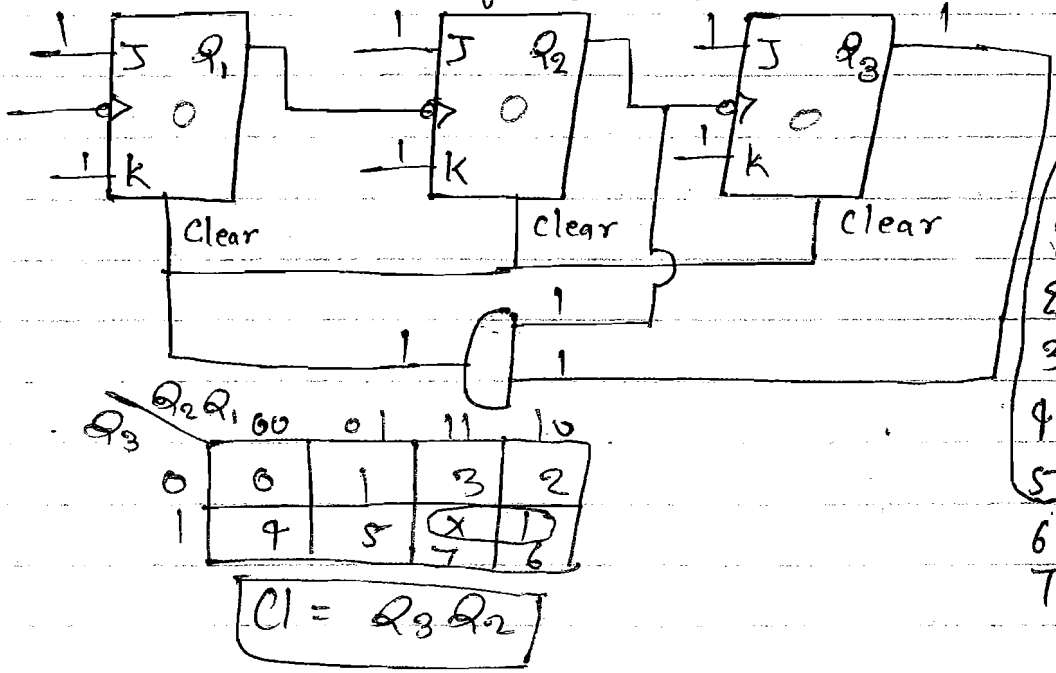
Preset:- It is used to display output 1.

Clear:- It is used to display output 0.

Both will operate at high input.

Ques Design a Mod-6 up counter by using negative edge triggered J-K flip-flop.

Sol^n For Mod-6, no. of flip-flops = 3.

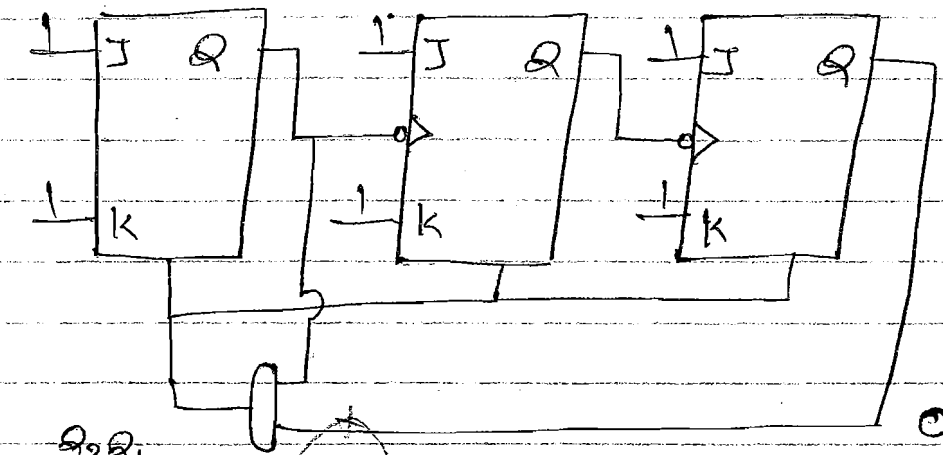


	Q_3	Q_2	Q_1	Clr
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
7	1	1	1	x/1

Q_3 \ Q_2Q_1	00	01	11	10
0	0	1	3	2
1	4	5	X 7	1 6

$Cl = Q_3 Q_2$

Q. Design a Mod-5 up Counter:



	Q_3	Q_2	Q_1	Clr
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
6	1	1	0	1/x
7	1	1	1	1/x

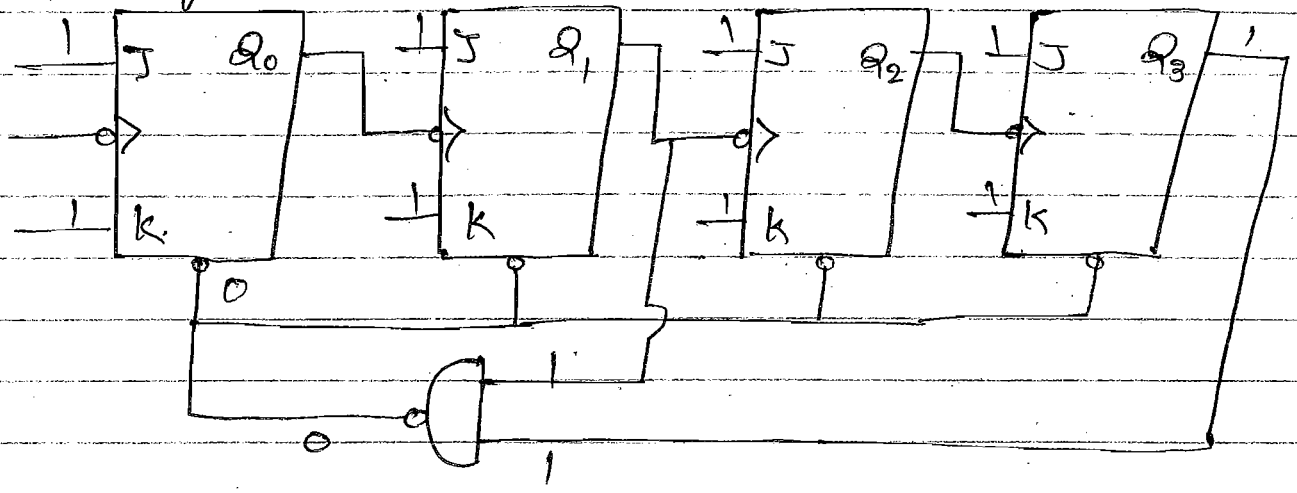
1 or don't Care

Q_3 \ Q_2Q_1	00	01	11	10
0	0	1	3	2
1	4	5	X 7	X 6

$Cl = Q_3 Q_1$

Ques for the given circuit diagram find the Mod of the counter?

Sol^n



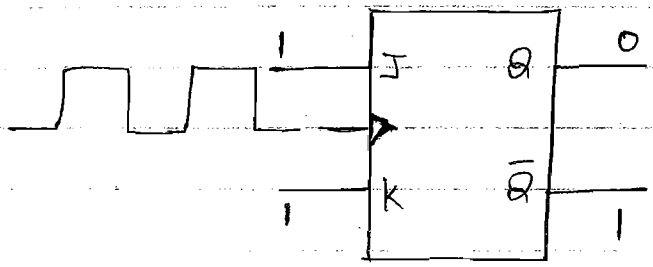
Ans:- Mod - 10 up counter.

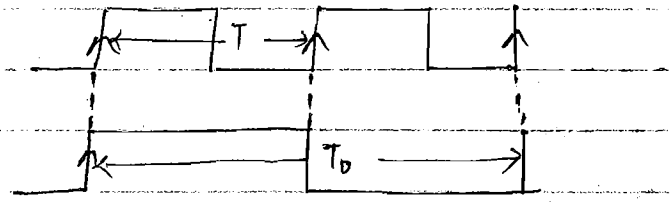
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

12/Aug/2019

Synchronous Counter:

Any ~~cant~~ count sequence is possible. Any flip-flop count be used for the design purpose. Operation is faster as compared to Assynchronous Counter.





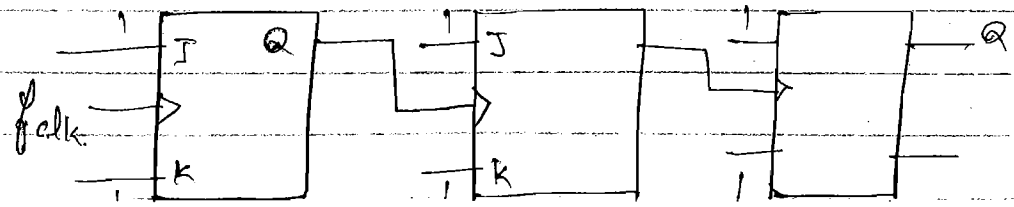
$T_0 = 2\,T_{clk}$

$f_0 = \frac{1}{2}\frac{1}{T_{clk}} = \frac{f_{clk}}{2}$

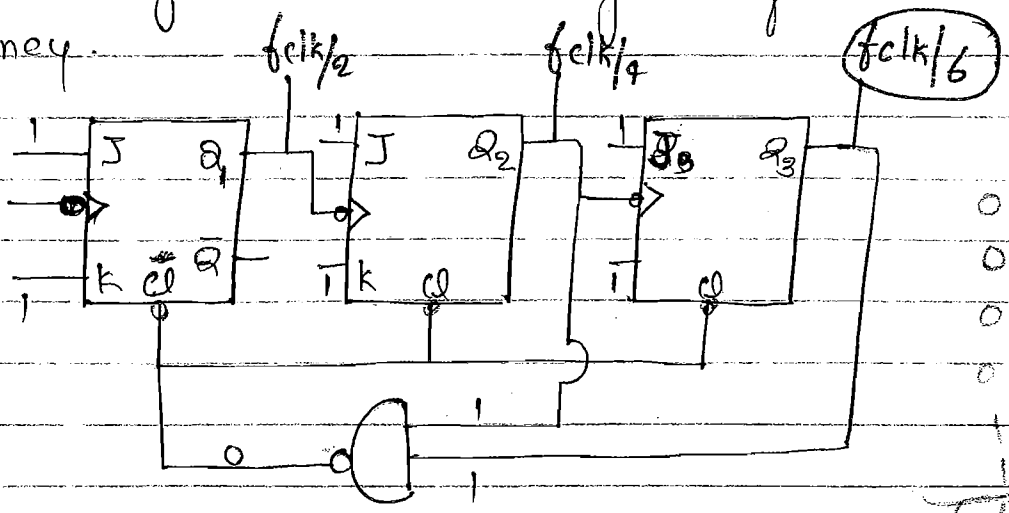
Output frequency of any flip-flop in the Asynchronous conter of is given by -

$$f_{clk} = \frac{f_{in}}{MOD}$$

Qus For the given circuit diagram find the output frequency of each flip-flop.

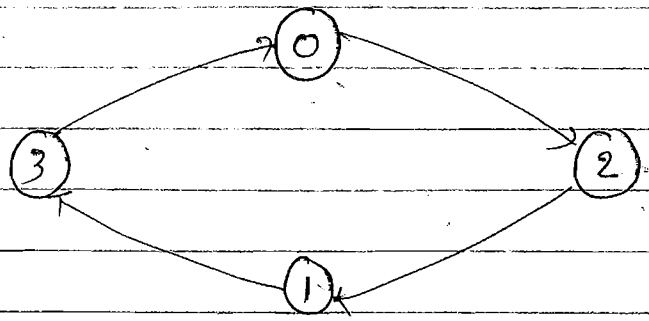


Ques For the given circuit diagram find the output frequency.



0	0	0		0
0	0	1		0
0	1	0		0
0	1	1		0
1	0	0		0
1	0	1		0
1	1	0		1

Ques Design a synchronous counter show that it counts

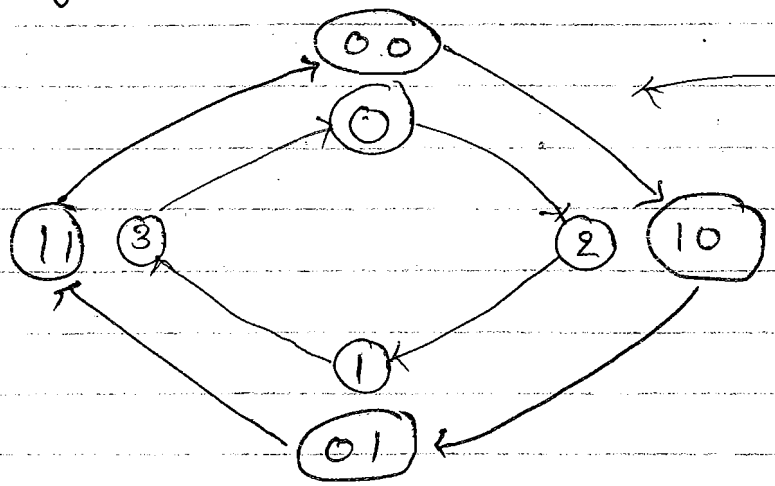


by using D-flip-flop.

Soln Steps for Counter Design :-

(i) Determine the count sequence
(ii) Draw the state table
(iii) Draw the excitation table
Implement characteristic table for the given flip-flop.
Minimise the logic circuit by using K-map.

(i) No. of flip-flop = 2 { largest no. is 3 = 11, so we need 2-f/f.

(ii) 

← State Table

(iii) Exitation Table :-

Q_n		Q_{n+1}			
Q_2	Q_1	Q_{2+1}	Q_{1+1}	D_2	D_1 { $\because Q_{n+1} = D$
0	0	1	0	1	0
1	0	0	1	0	1
0	1	1	1	1	1
1	1	0	0	0	0

Flip-Flops ⇒ D_1 and D_2

$D_2 \Rightarrow$

Q_2 \ Q_1	0	1
0	0 1	1 1
1	2 0	3 0

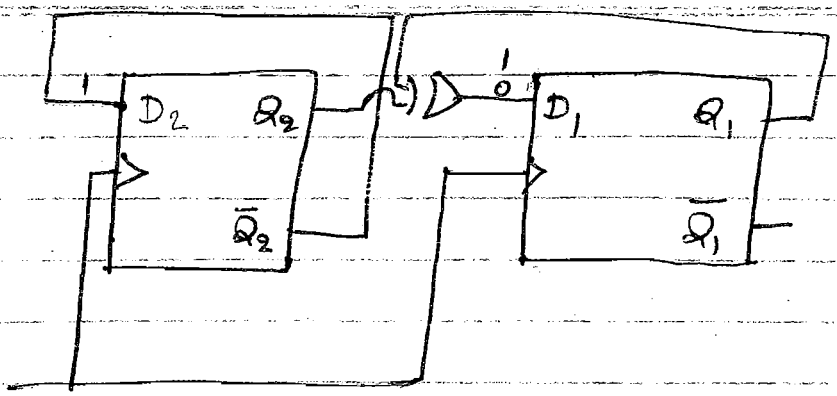
$$\boxed{D_2 = \overline{Q_2}}$$

$D_1 \Rightarrow$

Q_2 \ Q_1	0	1
0	0 0	1 (1)
1	2 (1)	3 0

$$D_1 = \overline{Q_2} Q_1 + \overline{Q_1} Q_2$$

$$\boxed{D_1 = Q_1 \oplus Q_2}$$



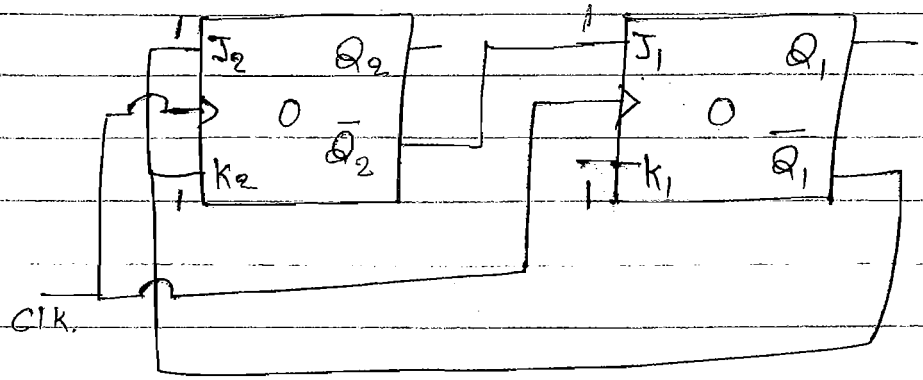
Ques For the given circuit diagram identify the count sequence if initial state are (0,0).

$D_2 = \bar{Q}_2$

$D_1 = Q_1 \oplus Q_2$

	D_2	D_1	Q_2	Q_1
X	1	0	0	0
			1	0
1)	0	1		
			0	1
2)	1	1		
			1	1
3)	0	0		

Ques For the given circuit diagram find the circuit sequence Q_2, Q_1.



(a) 00, 01, 10, 00, 01, 10

(b) 00, 01, 11, 00, 01, 11

(c) 00 10, 01, 00, 10, 01

(d) 00, 01, 10, 11, 00, 01, 10, 11

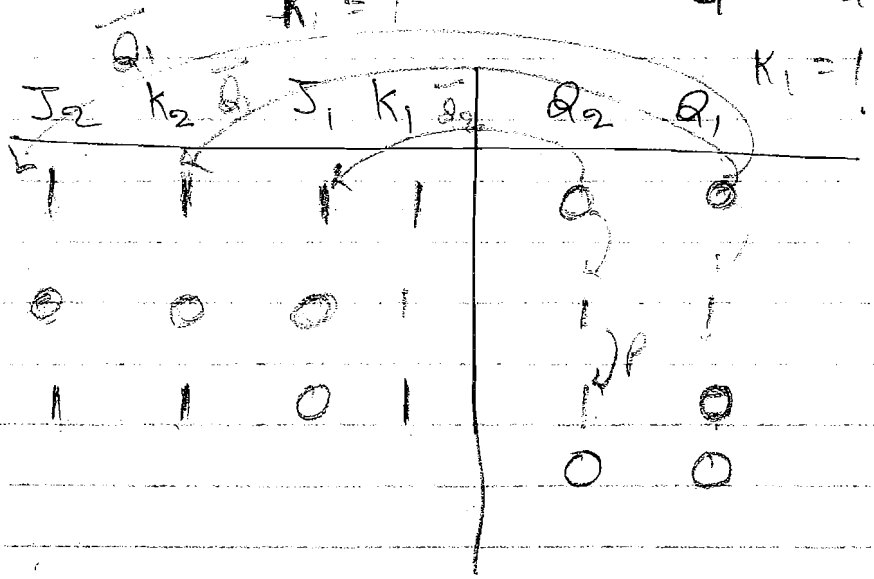
(e) 00, 11, 01

(f) 00 11 10

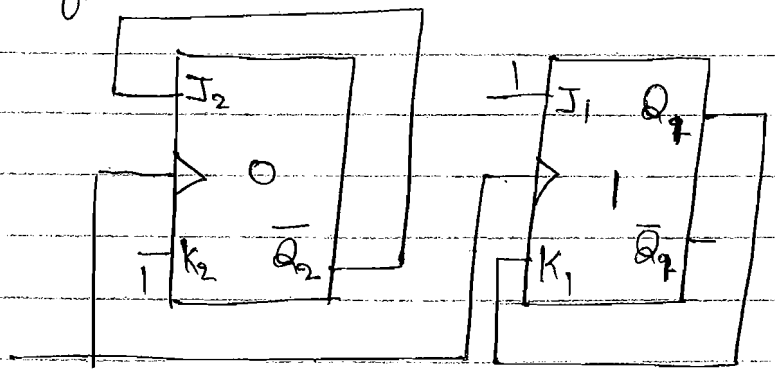
$D_2 = \overline{Q_2}$ $\quad J_2 = \overline{Q_1} = K_2$

$K_1 = 1$ $\quad J_1 = \overline{Q_2}$

$K_1 = 1$



Q. For the given circuit diagram find the count sequence.



$K_2 = 1, \quad J_1 = 1$

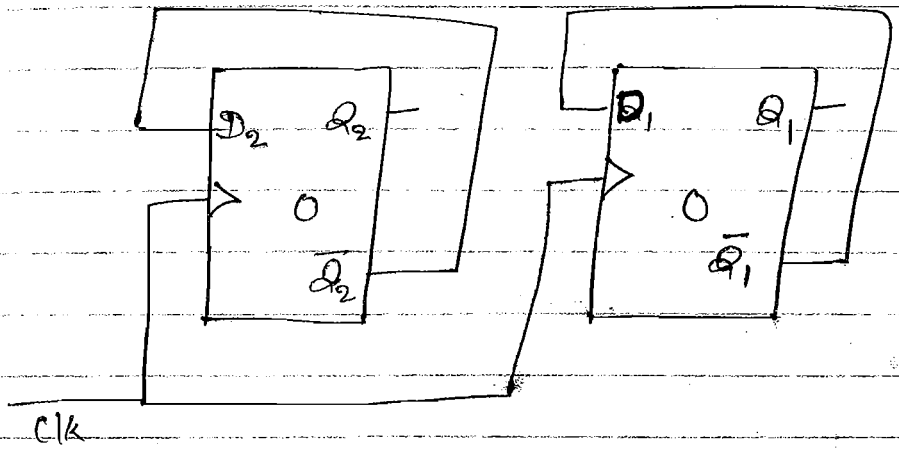
$J_2 = \overline{Q_2}, \quad K_1 = Q_1$

	J_2	K_2	J_1	K_1	Q_2	Q_1
X	1	1	1	1	0	1
1)	0	1	1	0	1	0
2)	1	1	1	1	0	1
3)	0	1	1	1	1	0

Sequence :-

01, 01, 01

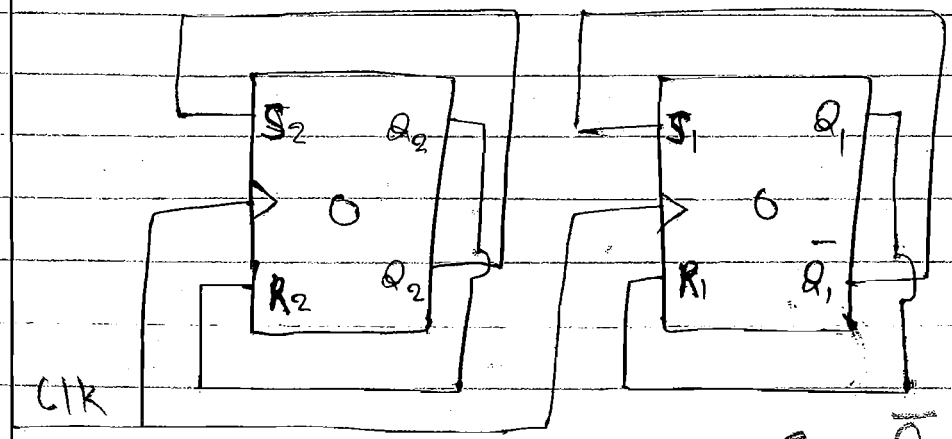
Ques Find the count sequence for the given circuit.



$D_2 = \bar{Q}_2$, $D_1 = \bar{Q}_1$

	D_2	D_1	Q_2	Q_1
X	1	1	0	0
1)	0	0	1	1
2)	1	1	0	0

Ques Find the count sequence for the given circuit.



$R_2 = Q_2$

$S_1 = \bar{Q}_1$ $\quad R_1 = Q_1$

$S_2 = \bar{Q}_2$

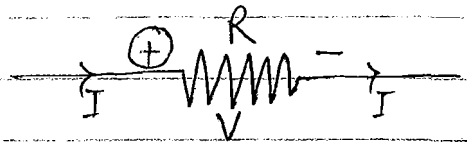
	S_2	R_2	S_1	R_1	Q_2	Q_1
X)	1	0	1	0	0	0
1)	0	1	0	1	1	1
2)	1	0	1	0	0	0

Final Sequence : 00, 11, 00, 11 (etc.)

DAC / ADC ⟶ Op-Amp.

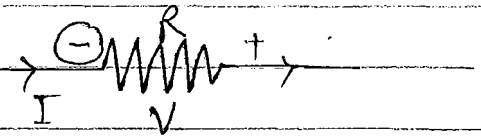
Logic Families ⟶ Transistors.

* Network Theory :-



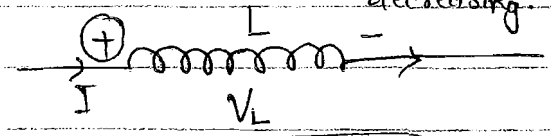
$$\therefore V = IR$$

↳ Voltage Drop { bcoz +ve to −ve voltage decreasing. }

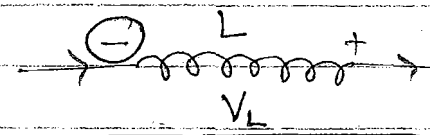


$$\therefore V = -IR$$

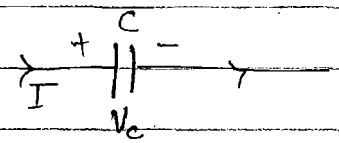
↳ Voltage Rise { bcoz −ve to +ve voltage increasing. }



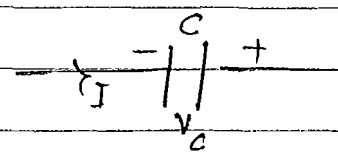
$$V_L = L\frac{dI}{dt}$$



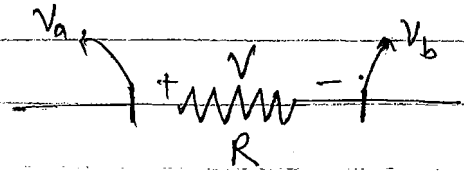
$$V_L = -L\frac{dI}{dt}$$



$$I = C\frac{dV_c}{dt}$$

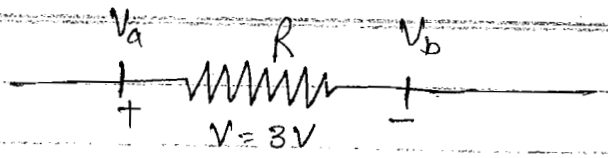


$$I = -C\frac{dV_c}{dt}$$



$$V = V_a - V_b$$

Ex-



$$V = V_a - V_b$$

$$3V = V_a - V_b$$

$$V_a - V_b = 3V$$

$3 - 0$ ← ground

$0 - (-3)$

$5 - 2$

$2 - (-1)$

⋮

So infinite no. are possible.

It is not possible to calculate potential at any point whether it is possible to calculate potential difference b/w two points.

$$V = IR$$

$$I = \frac{V}{R} = \frac{V_a - V_b}{R}$$

$\frac{V_a - V_b}{R}$ — always used.

$\frac{V}{R}$ — not used

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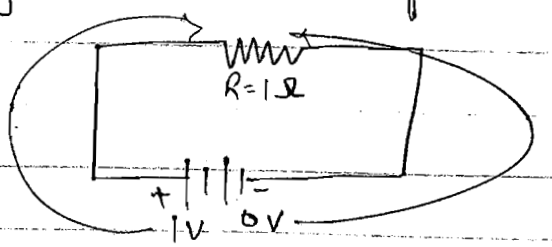
Q. for the given network find current I



$P = V^2/R$ OR $P = VI$

$P = I^2R$

Soln :- $I = \frac{V_a - V_b}{R} = \frac{1-0}{1\Omega}$

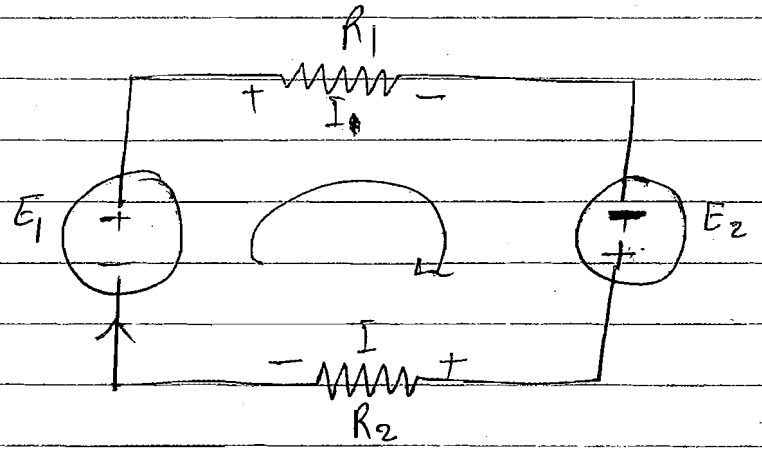
$I = 1$ Amp. Ans

Ques

$P = VI$ $P = -VI$

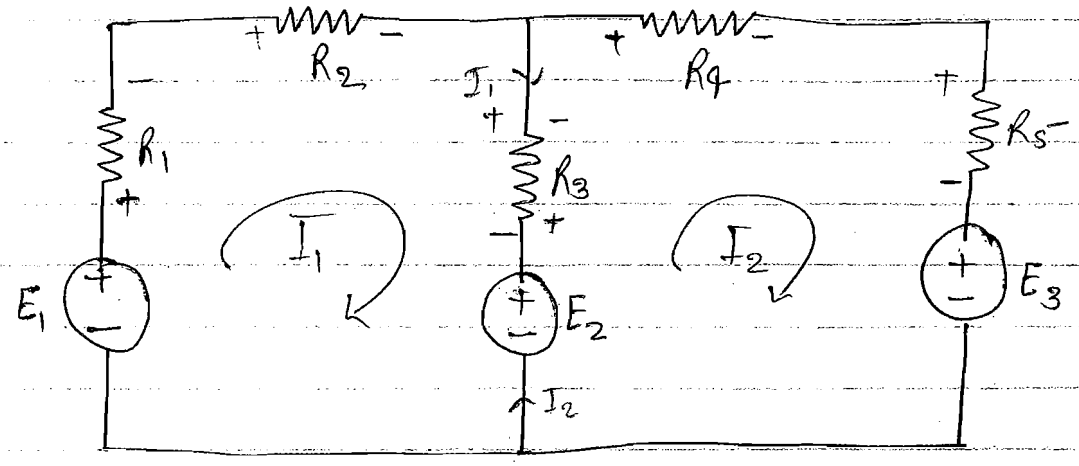
* K.V.L. :-

Algebraic sum of all voltage in a closed loop is always equal to zero.



$-E_1 + IR_1 - E_2 + IR_2 = 0$

Ques for the given circuit diagram write the loop equation.



loop I :- $$-E_1 + I_1R_1 + I_1R_2 + (I_1 - I_2)R_3 + E_2 = 0$$

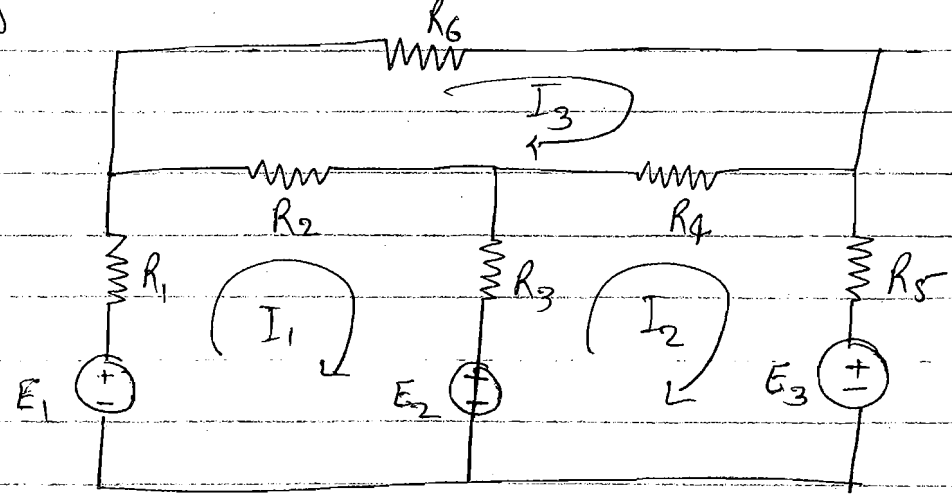
loop II :- $$I_2R_4 + I_2R_5 + E_3 - E_2 - (I_1 - I_2)R_3 = 0$$

OR

$$I_2R_4 + I_2R_5 + E_3 - E_2 + (I_2 - I_1)R_3 = 0$$

↳ (Sign of $R_3(+,-)$ are considered)

Ques Write the loop equation for the given circuit diagram.

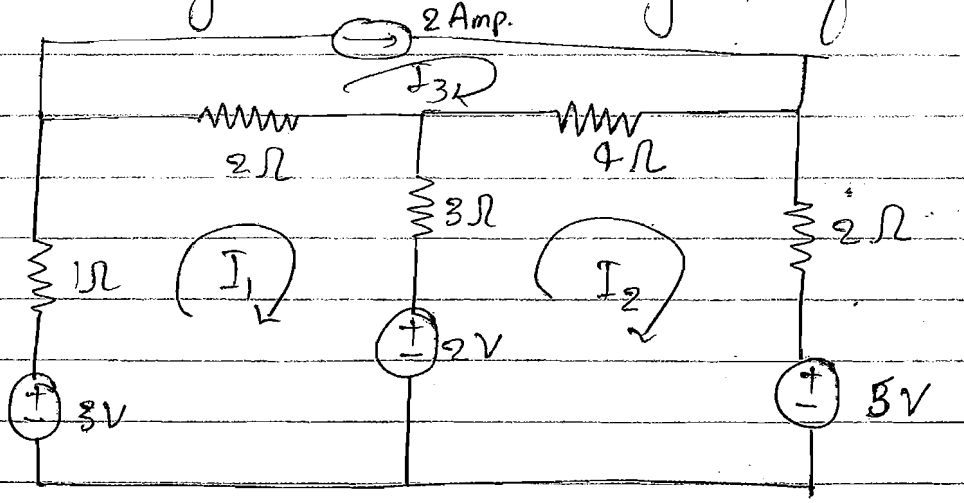


Loop I :-

Loop II :- $(I_2 - I_3) R_4 + I_2 R_5 + E_3 - E_2 + (I_2 - I_1) R_3 = 0$

Loop III :- $I_3 R_6 + (I_3 - I_2) R_4 + (I_3 - I_1) R_2 = 0$

Ques For the given circuit diagram find I_1, I_2, I_3 ?



Loop I :-

$\Rightarrow -3 + I_1 \cdot 1 + (I_1 - I_3) 2 + (I_1 - I_2) 3 + 2 = 0$ — (I)

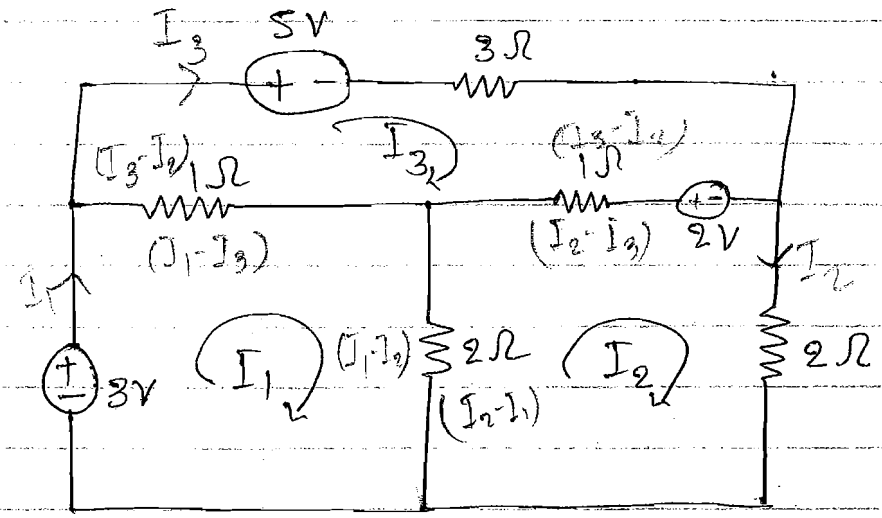
$\Rightarrow$ Loop II :-

$I_2 2 + 5 - 2 + (I_2 - I_1) 3 + (I_2 - I_3) 4 = 0$ — (II)

$\Rightarrow$ Loop III :-

$I_3 = 2$ Amp.

Qus For the given circuit diagram find the currents I_1, I_2, I_3 ?



loop I :-

$$(I_1-I_3)1 + (I_1-I_2)2 - 3 = 0$$

$$\Rightarrow 3I_1 - 2I_2 - I_3 = 3 \quad \text{---} \quad (I)$$

loop II :-

$$I_2 \cdot 2 + (I_2-I_1)2 + (I_2-I_3)\cdot 1 + 2 = 0$$

$$\Rightarrow 2I_1 - 5I_2 + I_3 = 2 \quad \text{---} \quad (II)$$

loop III :-

$$5 + 3 \times I_3 - 2 + (I_3-I_2)\cdot 1 + (I_3-I_1)\cdot 1 = 0$$

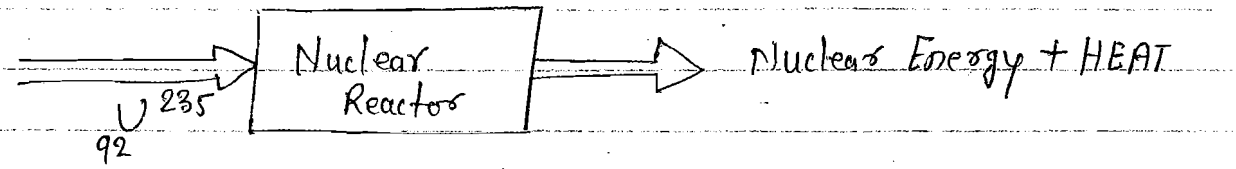
$$\Rightarrow -I_1 - I_2 + 4I_3 = 2-5 = -3$$

$$\Rightarrow I_1 + I_2 - 4I_3 = 3 \quad \text{---} \quad (III)$$

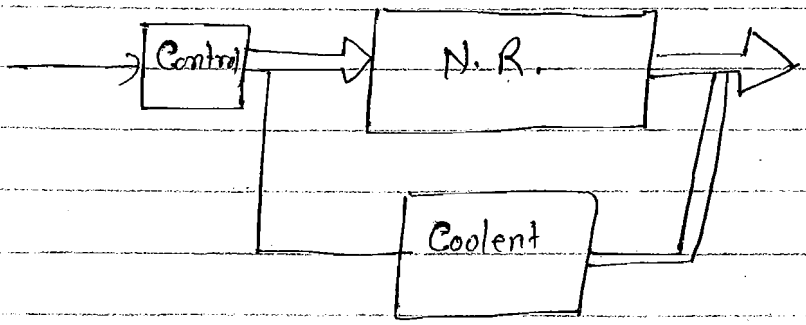
Op - Amp

Operational Amplifier

- Open Loop Op-Amp. (Comparator)
- Close Loop Op-Amp
  - Negative feedback (Amplifier)
  - Positive feedback (Wave form Generation)



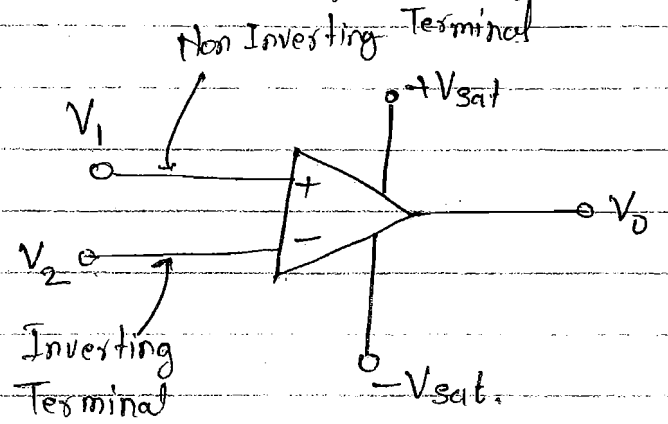
In the open loop connection there is no connection between output and input.



If there is a connection between output and input is called as feedback. If the ammount of i/p reduced from the actual ammount is.

called Negative feedback. If the ammount of input is increased from the actual ammount is called Positive feedback.

Open Loop Op-Amp :-



Entering Input :-

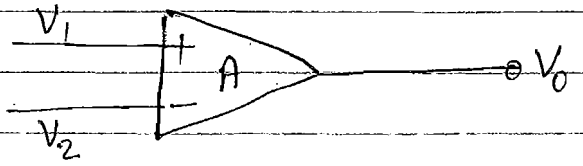
$V_1 + (-V_2) = V_0$

$$V_1 - V_2 = V_0$$

The Basic operation of op-Amp to amplify the difference of input.

Characteristic Properties of Open loop Op-Amp:-

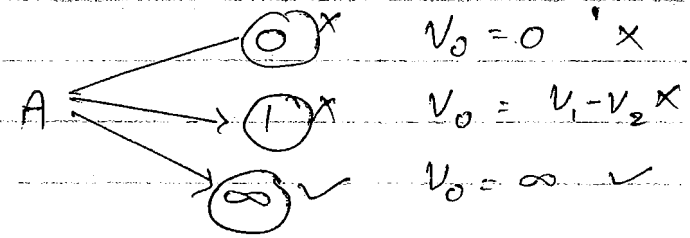
1 Open Loop Gain :-



$$A = \frac{V_0}{V_{in}}$$

$$V_0 = A \cdot V_{in}$$

$$V_0 = A(V_1 - V_2)$$



So ideal value of gain is must be infinity.

Case I :

$$V_0 = A(V_1 - V_2)$$

$$V_0 = \infty (V_1 - V_2)$$

Say $V_1 = 5$, $V_2 = 3$ $\therefore V_1 > V_2$

So $\therefore$ $\boxed{V_0 = +\infty}$ $= \boxed{+V_{sat}}$

Case II :

$$V_0 = A(V_1 - V_2)$$

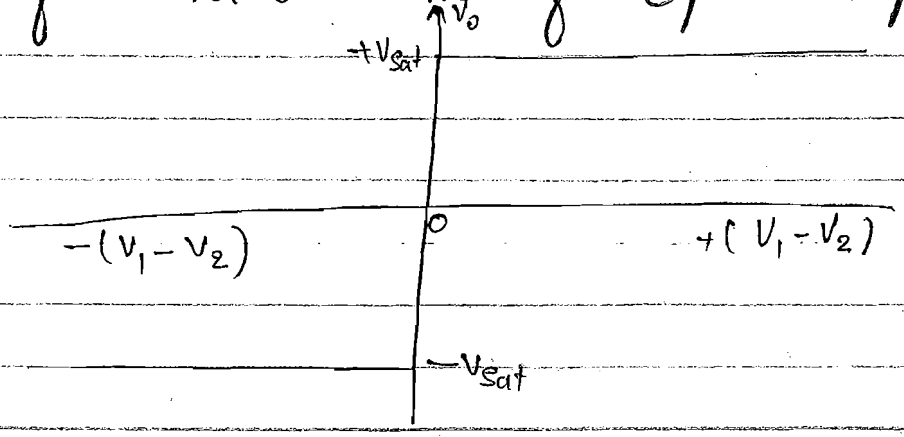
$$V_0 = \infty (V_1 - V_2)$$

Say $V_1 = 3$, $V_2 = 5$ $\boxed{V_2 > V_1}$

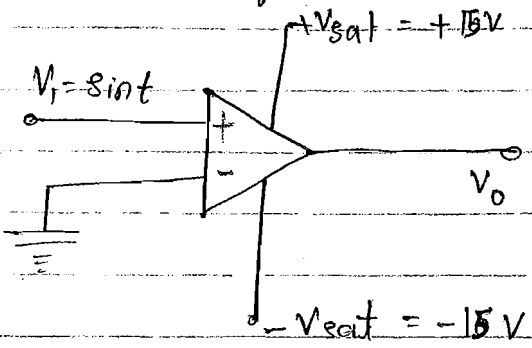
$$V_0 = \infty (-ve)$$

$\therefore$ $\boxed{V_0 = -\infty = -V_{sat}}$

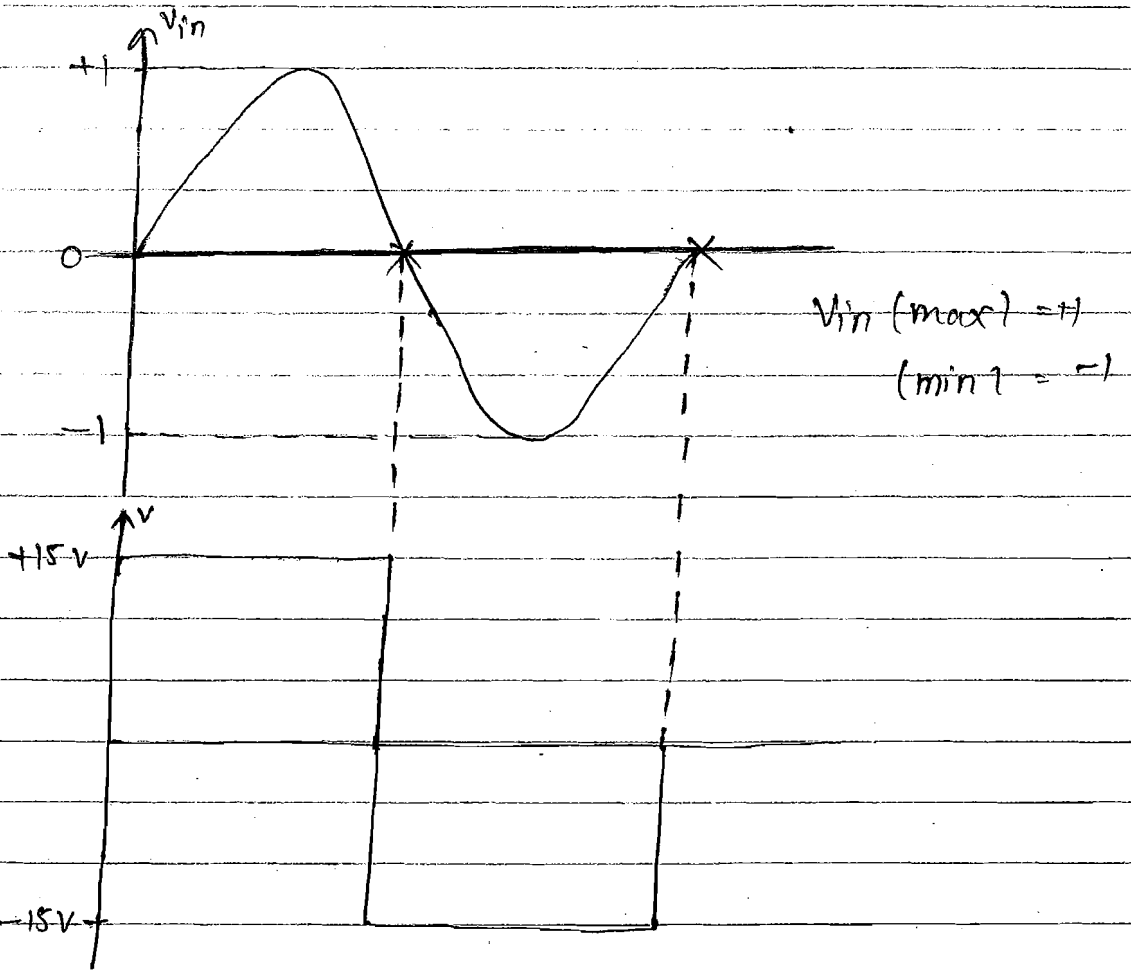
* Transfer characteristic of Open Loop Op-Amp :



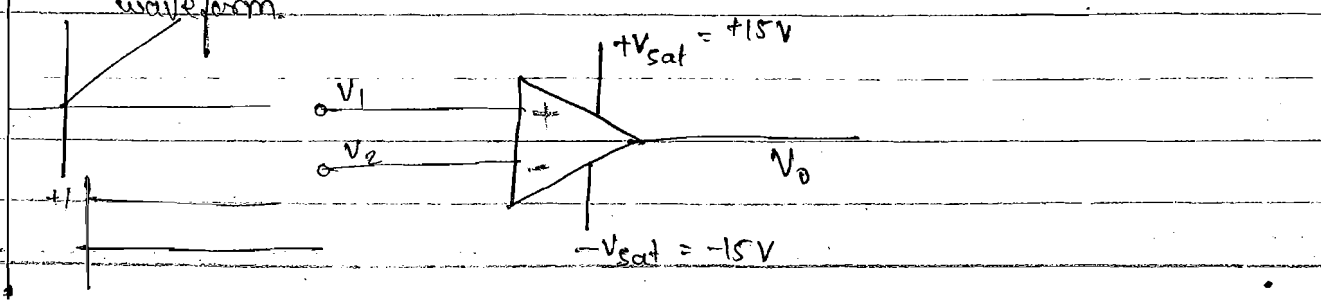
Ques for the given op-Amp Network draw the output waveform.



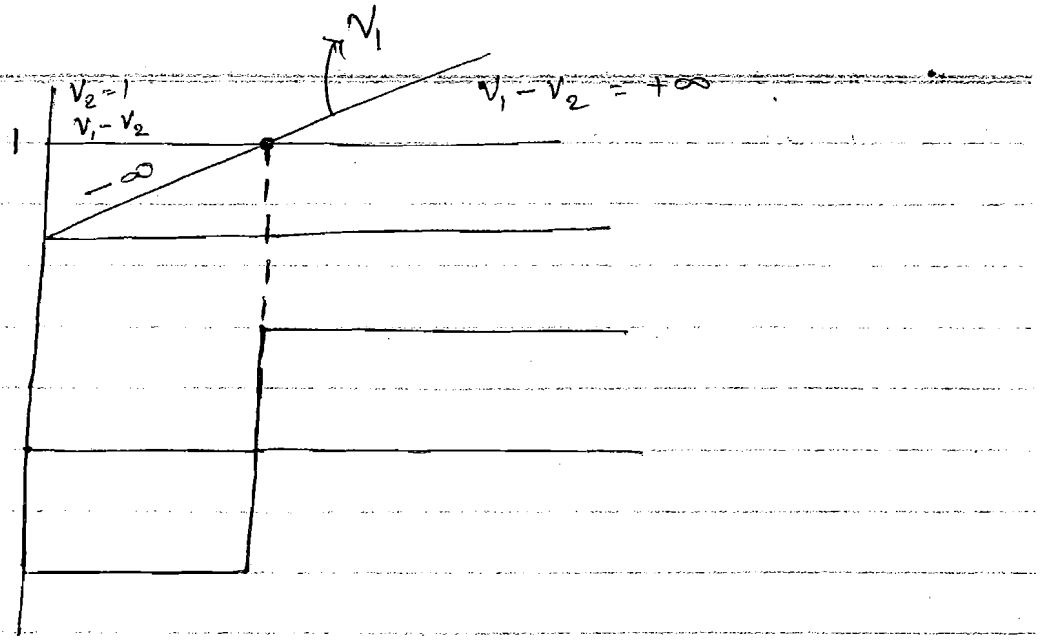
Soln :-



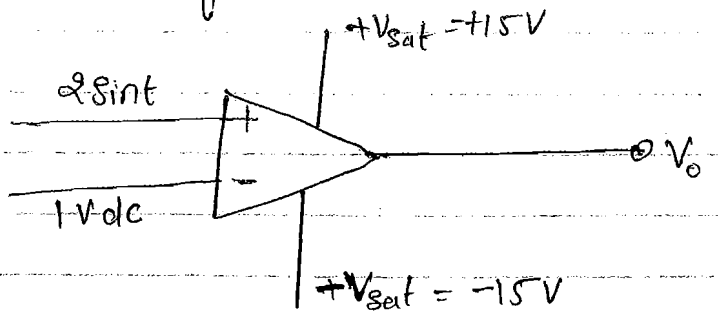
Ques for the given circuit diagram draw the output waveform.



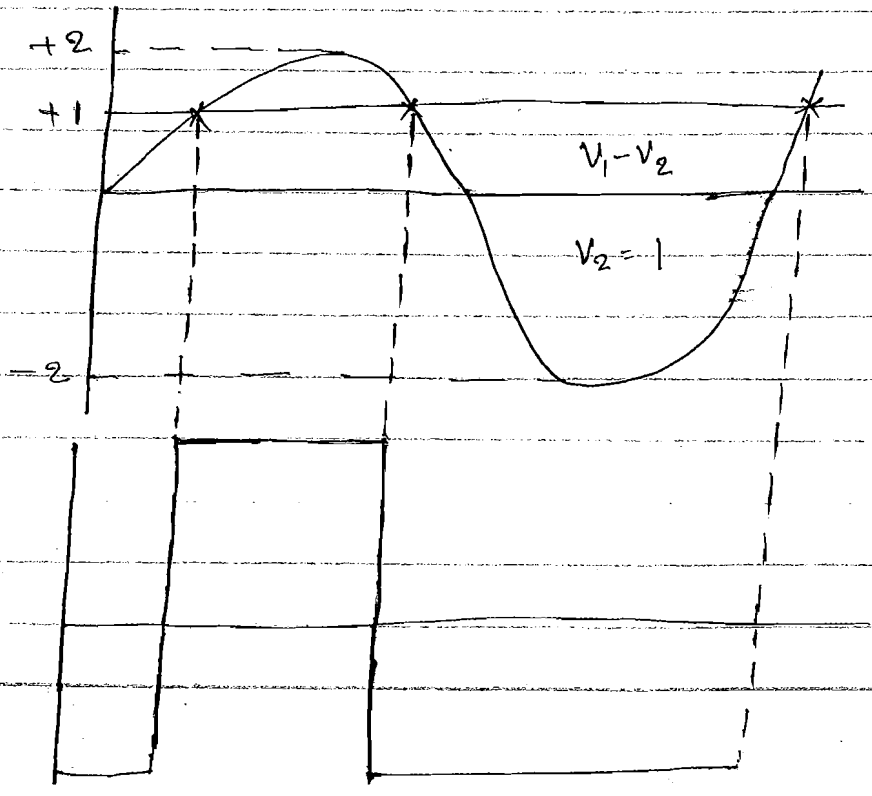
Soln :-



Ques For the given circuit diagram draw the output waveform.



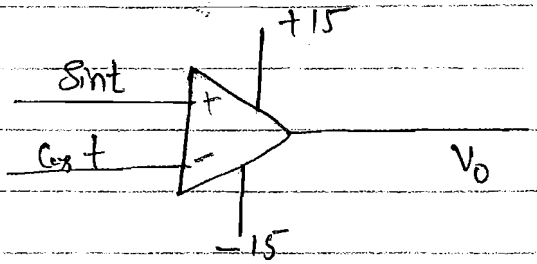
Soln



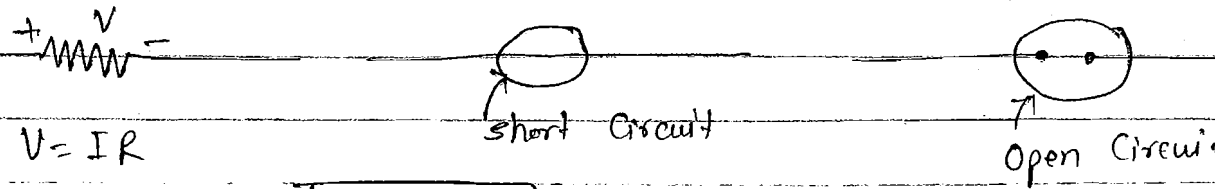
The output of open loop Op-Amp will be a rectangular wave.

H.W.

Ques Find the output waveform.



* Basic :-



$I = I_{max}$

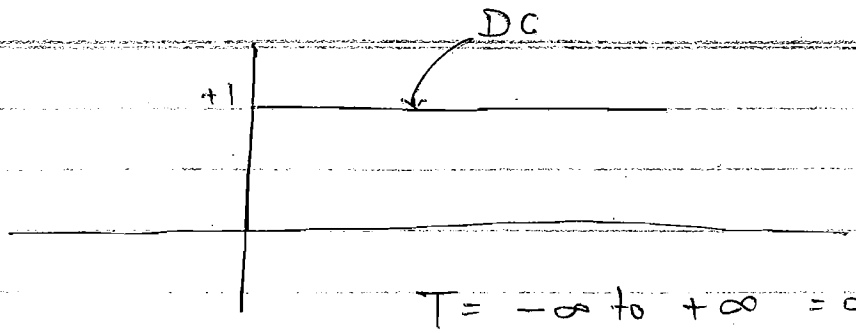
$V = IR$

$V = I \times 0 = 0$

$V = 0$

$I = 0$

$V = V_{max}$



$T = -\infty$ to $+\infty = \infty$

$\boxed{T = \infty}$

$f = \frac{1}{T} = \frac{1}{\infty} = 0$

$\boxed{f = 0}$

$X_L = \omega L = 2\pi f_L$

$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f_C}$

for D.C. $f_L = 0$

$\Rightarrow \boxed{X_L = 0}$

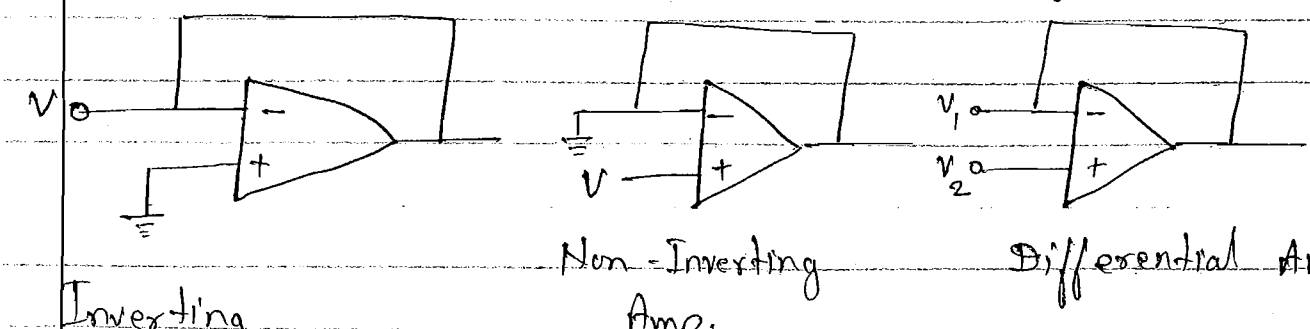
for D.C. $\boxed{f_C = 0}$

$\boxed{X_C = \infty}$

Note:- for a D.C source inductor will be replaced by a wire and capaciter is replaced by broken wire.

Amp.

* Close Loop Op-Amp. { Negative feedback } :-



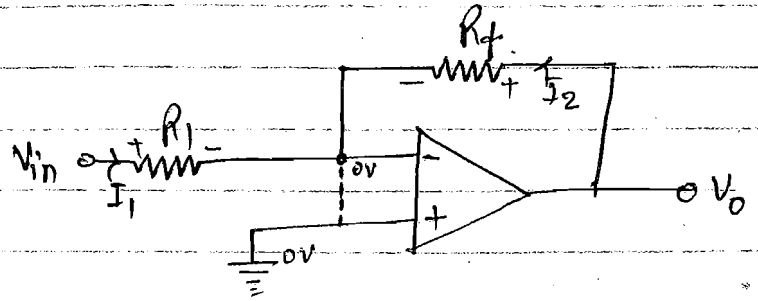
Inverting Amp

Non-Inverting Amp.

Differential Amp.

(iv) To solve negative feedback connection assume inverting and non-Inverting terminals are connected (Virtual short).

* Inverting Amplifier :-



$$\Rightarrow I_1 + I_2 = 0 \quad \{ \text{by K.C.L.} \}$$

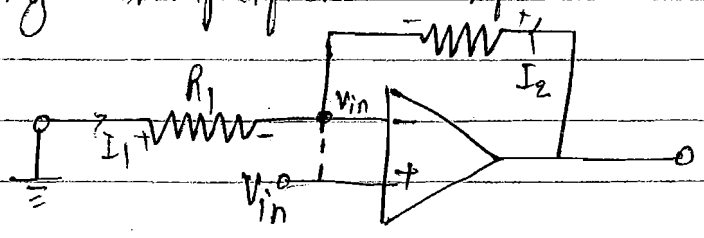
$$\Rightarrow \frac{V_{in} - 0}{R_1} + \frac{V_o - 0}{R_f} = 0$$

$$\Rightarrow \frac{V_{in}}{R_1} + \frac{V_o}{R_f} = 0$$

$$\Rightarrow \frac{V_o}{R_f} = \frac{-V_{in}}{R_1}$$

$$\Rightarrow \boxed{\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}} = \text{gain of Inverting Amplifier.}$$

* Non-Inverting Amplifier :-



$$I_1 + I_2 = 0$$

$$\frac{0 - V_{in}}{R_1} + \frac{V_o - V_{in}}{R_f} = 0$$

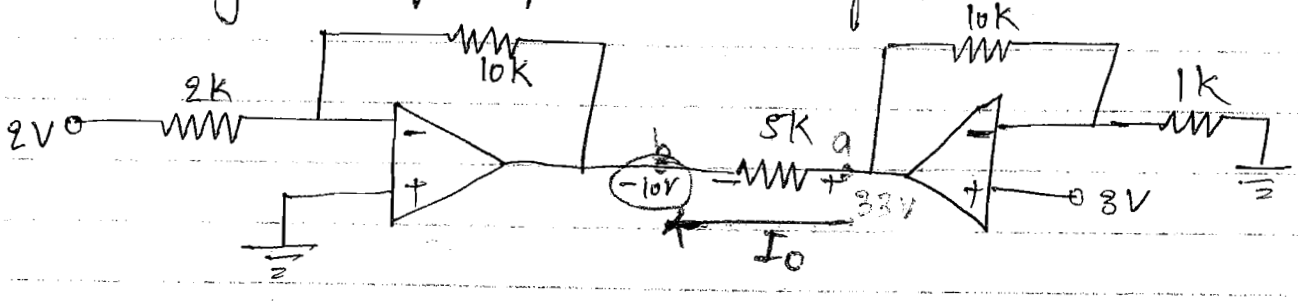
$$\frac{V_o - V_{in}}{R_f} = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{R_f} = V_{in}\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\frac{V_o}{V_{in}} = R_f\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\boxed{\frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right)} = \text{Gain of Non-Inverting Amplifier.}$$

Ques For the given Op-Amp network find the current I_o



Soln

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1} = \frac{-10k}{2k} = -5\,k$$

$$V_o = V_{in} \times -5 = 2 \times -5$$

$$\boxed{V_o = -10\ V}$$

$$\frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_1}\right) = \left(1 + \frac{10}{1}\right) = 11$$

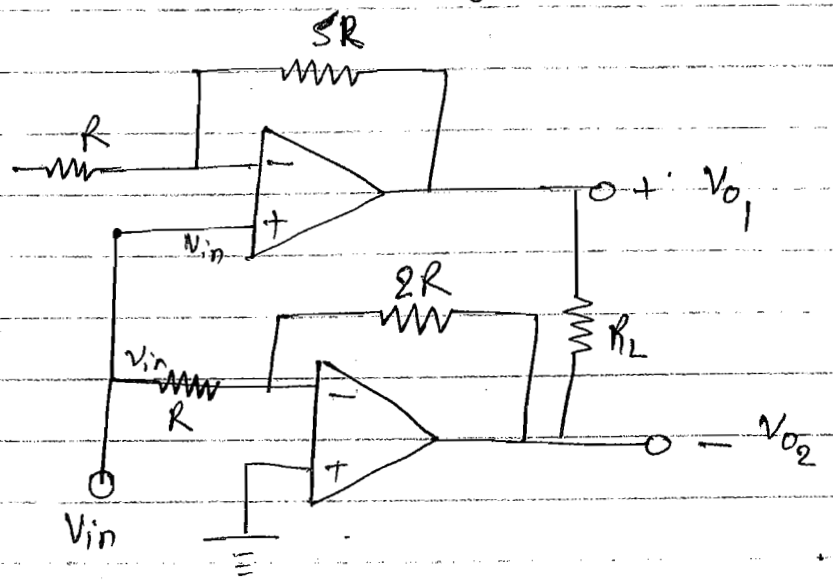
$$V_o = 3 \times 11 = 33V$$

$$\boxed{V_o = 33V}$$

$$\therefore I_o = \frac{V_a - V_b}{R} \Rightarrow I_o = \frac{3.3 - (-10)}{5k} = \frac{43}{5k} = 8.6\ m.A.$$

Ans

Qus | for the given circuit diagram find output voltage V_o.



Soln I/ $\frac{V_{o_1}}{V_{in}} = 1 + \frac{R_f}{R_1} = 1 + \frac{5R}{R} = 6$

$$\boxed{V_{o_1} = 6V_{in}}$$

II nd $\frac{V_{o_2}}{V_{in}} = \frac{-R_f}{R_1} = \frac{-2R}{R}$

$$\frac{V_{o_2}}{V_{in}} = -2$$

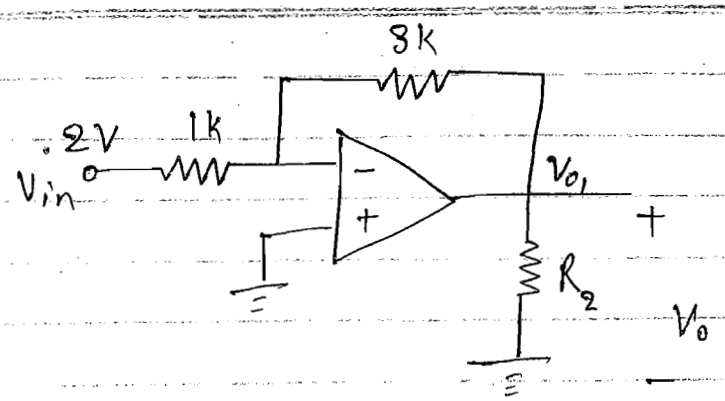
$$\Rightarrow \boxed{V_{o_2} = -2V_{in}}$$

$$V_o = V_{o_1} - V_{o_2} = 6V_{in} - (-2V_{in}) = 8V_{in}$$

$$\boxed{\frac{V_o}{V_{in}} = 8}$$ Ans

H.W.

Ques



Sol^n

$$\frac{V_{o_1}}{V_{in}} = \frac{-R_f}{R_1} = \frac{-3K}{1K}$$

$$\frac{V_{o_1}}{V_{in}} = -3$$

$$V_{o_1} = -3 \times V_{in} = -3 \times 2$$

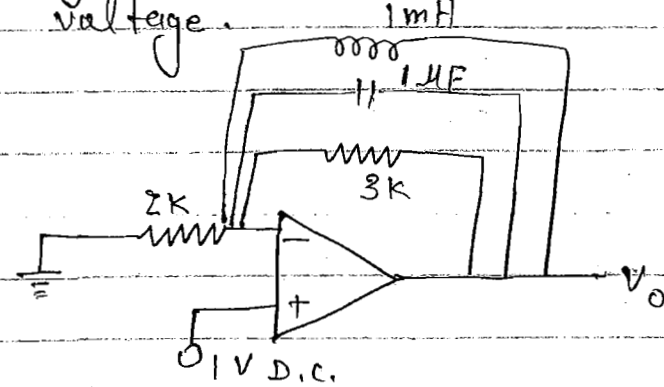
$$\boxed{V_{o_1} = -6}$$

$$V_o = V_{o_1} - 0$$

$$= -6 - 0$$

$$\boxed{V_o = -6}$$ Ans

Ques For the given Op-Amp network determine output voltage.



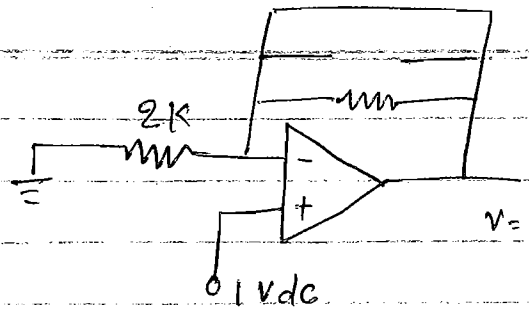
Sol^n

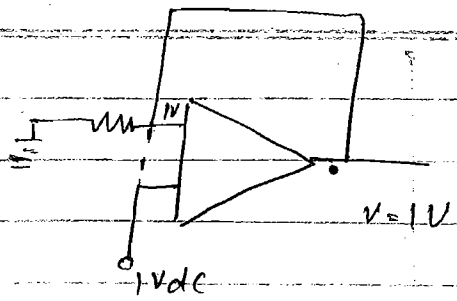
(a) 10 V

(b) −10 V

(c) 1 V

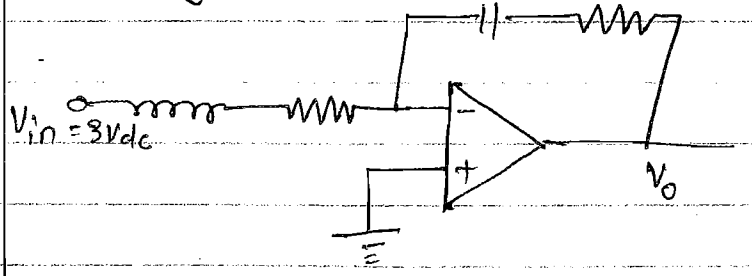
(d) −1 V



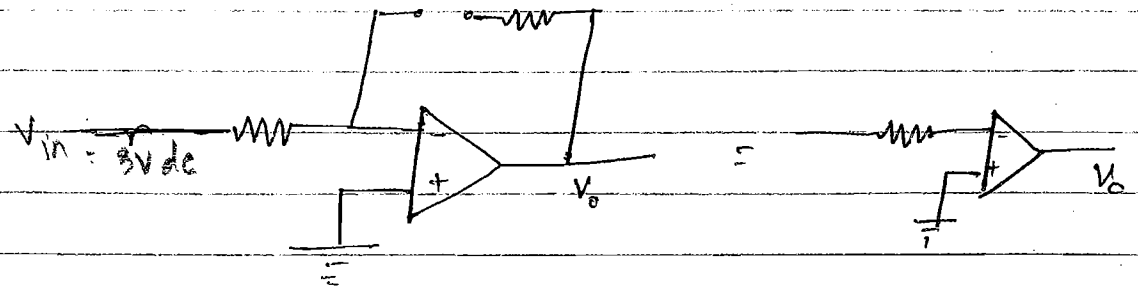


$V = 1\ V_{volt}$ Ans

Ques For the given circuit diagram find the output voltage.

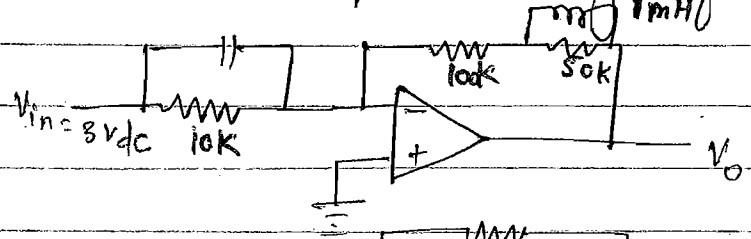


(a) 3 V
(b) −3 V
(c) Saturation Voltage
(d) −10 V

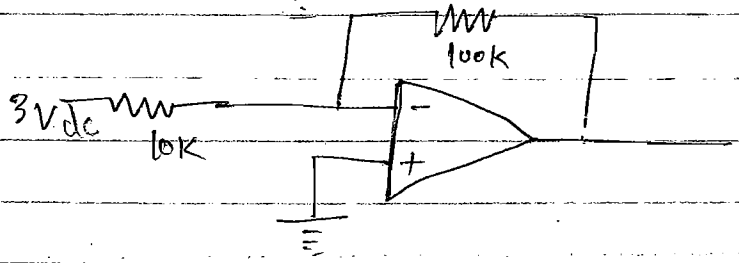


Since it is open loop so the o/p = saturation.

Ques Find the output voltage for given circuit.



Sol^n

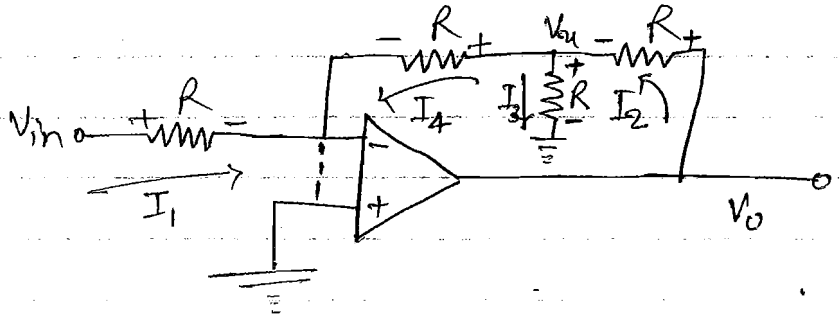


$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1} = \frac{-100\,k}{10k}$$

$$\frac{V_o}{V_{in}} = -10$$

$$\Rightarrow V_o = -10 \times V_{in} = -10 \times 3 = -30\,V \quad \text{Ans}$$

Ques For the given network calculate the voltage gain.



Soln

$$I_2 = I_3 + I_4$$

$$\frac{V_o - V_{a1}}{R} = \frac{V_{a1} - 0}{R} + \frac{V_{a1} - 0}{R}$$

$$V_o = 3V_{a1}$$

$$\boxed{V_{a1} = \frac{V_o}{3}}$$

$$I_1 + I_f = 0$$

$$\frac{V_{in} - 0}{R} + \frac{V_{a1} - 0}{R} = 0$$

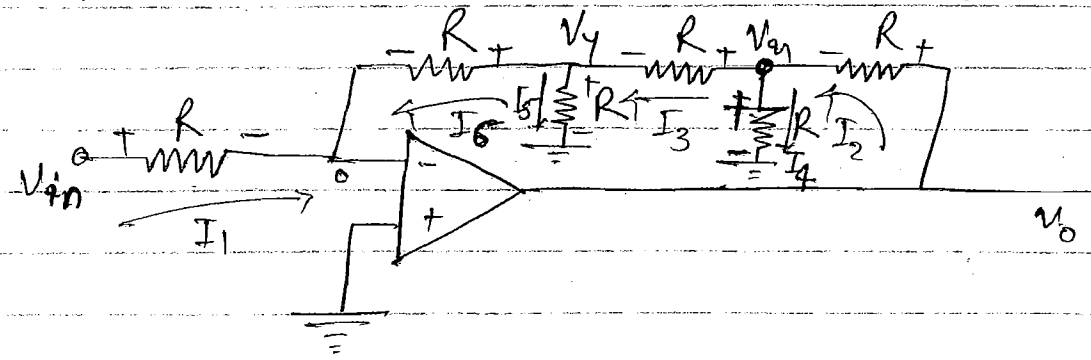
$$V_{in} = -V_{a1}$$

$$V_{in} = -\frac{V_o}{3}$$

$$\boxed{\frac{V_o}{V_{in}} = -3}$$

Ans

Qus: For the given network find the voltage gain.



(a) -5^- (b) -8 (c) -10 (d) -11

Soln:

$$I_2 = I_3 + I_4$$

$$\frac{V_o - V_2}{R} = \frac{V_2 - V_1}{R} + \frac{V_2}{R}$$

$$\boxed{V_o = 3V_2 - V_1} \quad \text{---(i)}$$

Now $I_3 = I_5 + I_6$

$$\frac{V_2 - V_1}{R} = \frac{V_1 - 0}{R} + \frac{V_1 - 0}{R}$$

$$\boxed{V_2 = 3V_1} \quad \text{---(ii)}$$

from (ii) & (i)

$$V_o = 3 \times 3V_1 - V_1$$

$$= 9V_1 - V_1$$

$$\boxed{V_o = 8V_1}$$

OR $\boxed{V_1 = \frac{V_o}{8}}$

$$I_1 + I_6 = 0$$

$$\frac{V_{in} - 0}{R} + \frac{V_y}{R} = 0$$

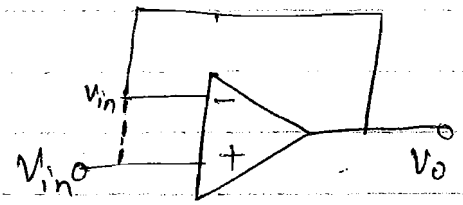
$$V_{in} = -V_y$$

$$V_{in} = \frac{-V_o}{8}$$

$$\boxed{\frac{V_o}{V_{in}} = -8}$$

Qus for the given circuit diagram determine o/p voltage.

Soln



$$\boxed{V_o = V_{in}}$$

- This circuit is called voltage follower (o/p voltage always follow i/p voltage).

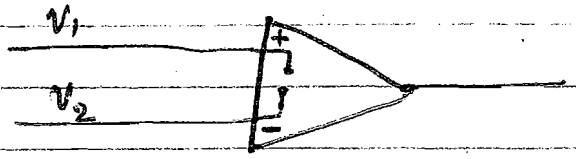
$$\boxed{\frac{V_o}{V_{in}} = 1}$$

- It is also called as Unity gain Amp.
- Voltage follower is used to convert high impidence source to low impidance source.

Properties of Op-Amp.

* Input Current :-

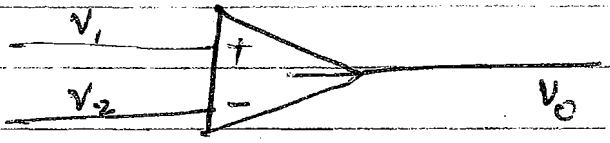
The input resistance of the op-Amp will be infinity (represented by input circuit) hence input current will be zero. Voltage will be maximum.



i/p Resistance will be ∞.

* Output Resistance :-

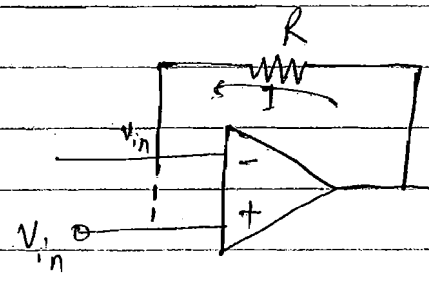
The output resistance of op-Amp will be ideally zero.



O/p Resistance $\simeq 0$

Ans for the given circuit diagram find output voltage.

Soln



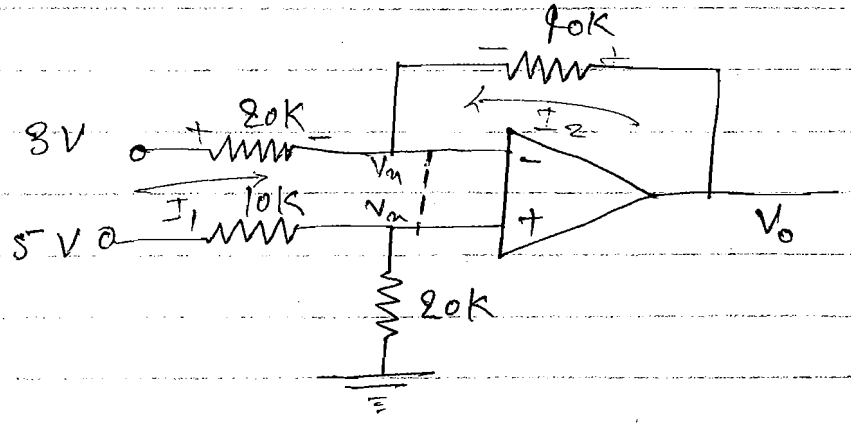
$$I = 0$$

$$\frac{V_o - V_{in}}{R} = 0$$

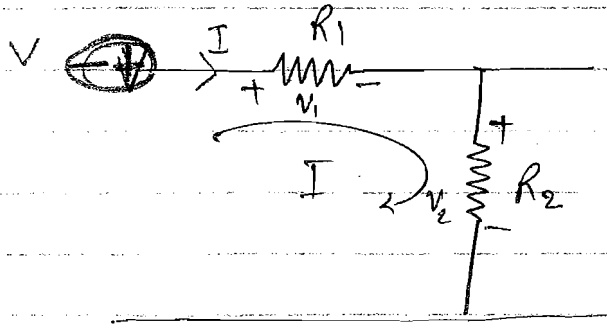
$$\boxed{V_o = V_{in}}$$

Still voltage follower :

Qus For the given Op-Amp determine the op voltage.



Soln



$$-V + IR_1 + IR_2 = 0$$

$$I(R_1 + R_2) = V$$

$$\boxed{I = \frac{V}{R_1 + R_2}}$$

$$V_1 = IR_1$$

$$\boxed{V_1 = \frac{VR_1}{R_1 + R_2}} \quad \text{(memorize)}$$

$$V_2 = IR_2$$

$$\boxed{V_2 = \frac{VR_2}{R_1 + R_2}} \quad \text{(memorize)}$$

So $V_a = \frac{5 \times 20}{3 \times} = \frac{10}{3}$ Volt

$\Rightarrow I_1 + I_2 = 0$

$$\frac{3 - V_x}{20k} + \frac{V_o - V_x}{10k\,2} = 0$$

$$3 - V_x + \frac{V_o - V_x}{2} = 0$$

$$3 - V_x + \frac{V_o}{2} - \frac{V_x}{2} = 0$$

$$\frac{V_o}{2} = \frac{3V_x}{2} - 3$$

$$\frac{V_o}{2} = \frac{3 \times 10 \times 5}{2 \times 3} - 3$$

$$\frac{V_o}{2} = 5 - 3 = 2$$

$$V_o = 2 \times 2 = 4$$

$$\boxed{V_o = 4}$$

Trick :-

When $\frac{R_f}{R_1} = \frac{R_3}{R_2}$ { in Differential Amp.

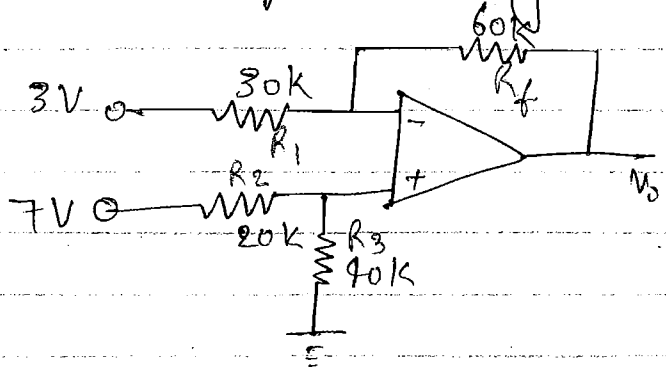
then $\boxed{V_o = (V_+ - V_-)\left(\frac{R_f}{R_1}\right)}$ (Memorise)

$$V_o = (5 - 3)(2)$$

$$= 2 \times 2$$

$$\boxed{V_o = 4\,V}$$ Ans

Qus Find the output voltage



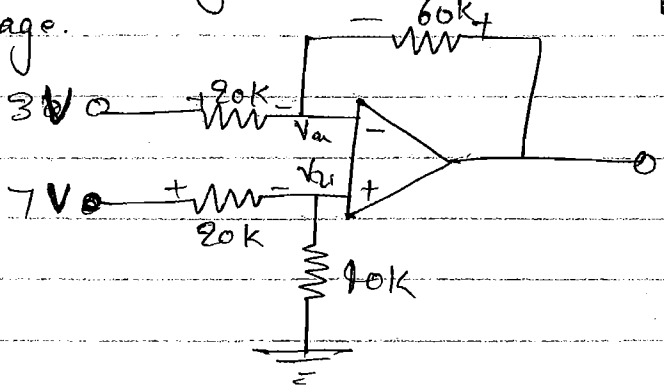
Sol^n

$$\frac{R_f}{R_1} = \frac{R_3}{R_2} = 2$$

So $V_o = (7-3) \times 2 = 4 \times 2$

$$\boxed{V_o = 8}$$

Qus For the given circuit diagram determine o/p voltage.



Sol^n

$$V_a = \frac{40 \times 7}{20+40} = \frac{280}{60} = \frac{28}{6}\ V$$

by K.C.L :-

$$I_1 + I_2 = 0$$

$$\frac{V_a - 3}{20} + \frac{V_o - V_a}{60} = 0$$

$$\frac{\frac{28}{6} - 3}{20} + \frac{V_o - \frac{28}{6}}{60} = 0$$

$$\frac{28-18}{120} + \frac{28-19}{6 \times 60} = \frac{-V_o}{60}$$

$$\frac{10}{120} + \frac{9}{180} = \frac{-V_o}{60}$$

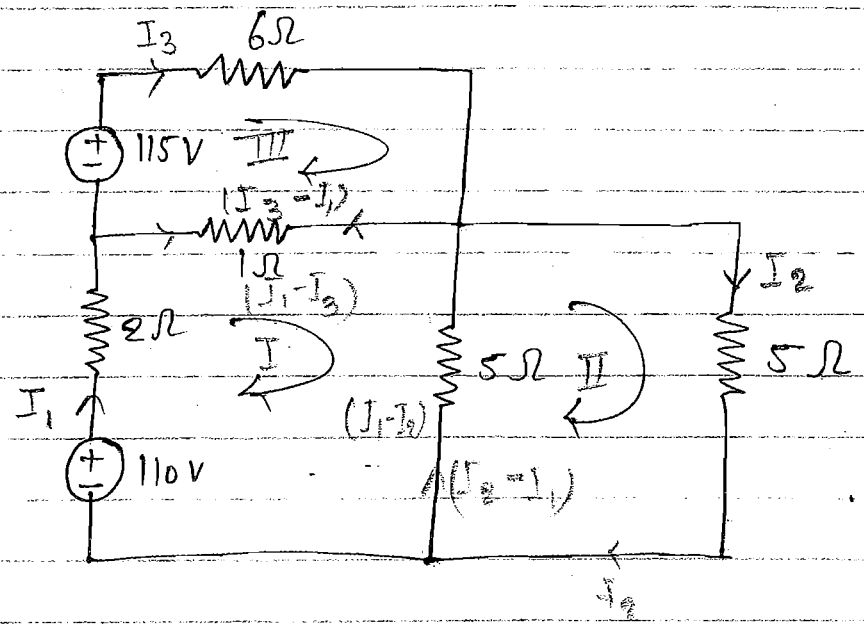
$$-V_o = \frac{60}{12} + \frac{19 \times 60}{180}$$

$$-V_o = 5 - \frac{19}{3} = \frac{+15-19}{3}$$

$$-V_o = \frac{+4}{3}$$

$$\boxed{V_o = 1.33\ V}$$

Qus For the given circuit diagram, Determine the all loop currents.



loop I :-

$$-110V + I_1 \times 2\Omega + (I_1-I_3)\,1\Omega + (I_1-I_2)\,5\Omega = 0$$

$$2I_1 + I_1 - I_3 + 5I_1 - 5I_2 = 110$$

$$8I_1 - 6I_2 = 110 \quad \text{---(I)}$$

loop III :-

$$-115 + I_3 6\Omega + (I_3-I_1)1\Omega = 0$$

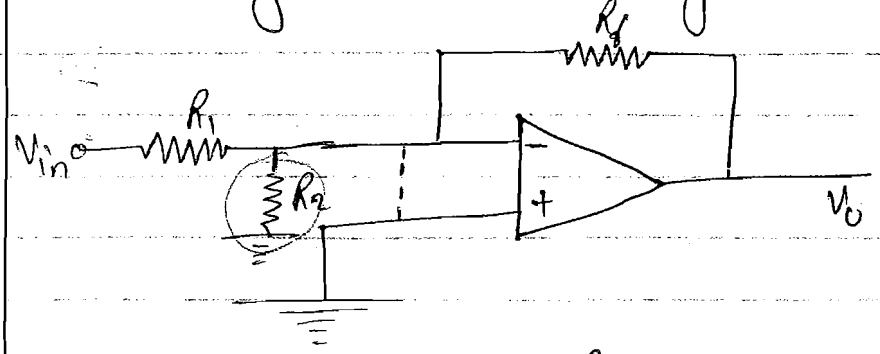
$$7I_3 - I_1 = 115 \quad \text{---(II)}$$

loop II :-

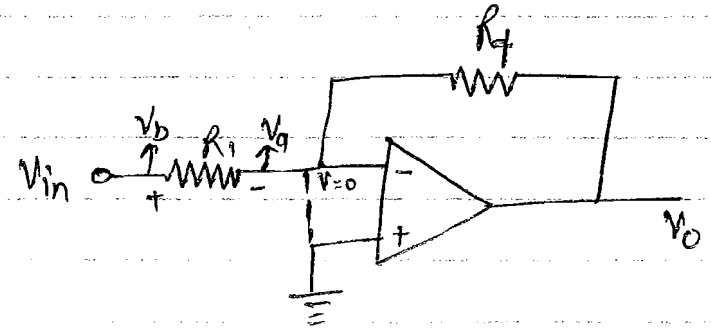
$$I_2 \times 5\Omega + (I_2-I_1)5\Omega = 0$$

$$10I_2 - 5I_1 = 0 \quad \text{---(III)}$$

Qwy For the given circuit diagram calculate voltage gain.

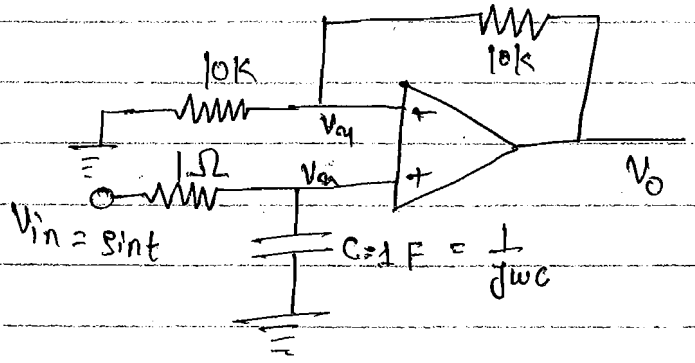


Sol^n:-



$$\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$$

Qwy For the given circuit diagram calculate V_o



(a) $\sqrt{2}\sin(t+45^\circ)$

(b) $\sqrt{2}\sin(t+45^\circ)$

(c) $\frac{1}{\sqrt{2}}\sin(t-45^\circ)$

(d) $\frac{1}{\sqrt{2}}\sin(t+45^\circ)$

Soln

$\because V_{in} = \sin \omega t = \sin t$

~~but~~ $\boxed{\omega = 1}$

$\because C = \frac{1}{j\omega C} = \frac{1}{j(1)(1)}$

$$\boxed{C = \frac{1}{j}}$$

$$V_{ab} = \frac{\sin t \times \frac{1}{j}}{1 + \frac{1}{j}} \qquad \left(V_x = \frac{V \times R_2}{R_1 + R_2}\right)$$

$$V_{ab} = \frac{\sin t \times \frac{1}{j}}{\frac{j+1}{j}} = \frac{\sin t}{1+j}$$

by K.C.L. :-

$$I_1 + I_2 = 0$$

$$\frac{0 - V_{ab}}{10k} + \frac{V_0 - V_{ab}}{10k} = 0$$

$$V_0 - 2V_{ab} = 0$$

$$\boxed{V_0 = 2V_{ab}}$$

$$V_0 = \frac{2 \sin t}{1+j} \quad \text{①}$$

$a+ib = \sqrt{a^2+b^2} = \text{mag.}$

phase $\angle = \tan^{-1}\left(\frac{b}{a}\right)$

$\frac{1}{a+jb} = \frac{1}{\sqrt{a^2+b^2}}$

phase $\angle = -\tan^{-1}\left(\frac{b}{a}\right)$

$\text{mag.} = |1+j.1| = \sqrt{1^2+1^2} = \sqrt{2}$

Phase Angle $= -\tan^{-1}\left(\frac{1}{1}\right)$

$= -\tan^{-1} 1 = -\tan^{-1}(\tan 45)$

$= -45^\circ$

So from ① $V_0 = \frac{2 \sin t \angle -45^\circ}{\sqrt{2}}$

$V_o = \sqrt{2}\sin t \angle -45^\circ$

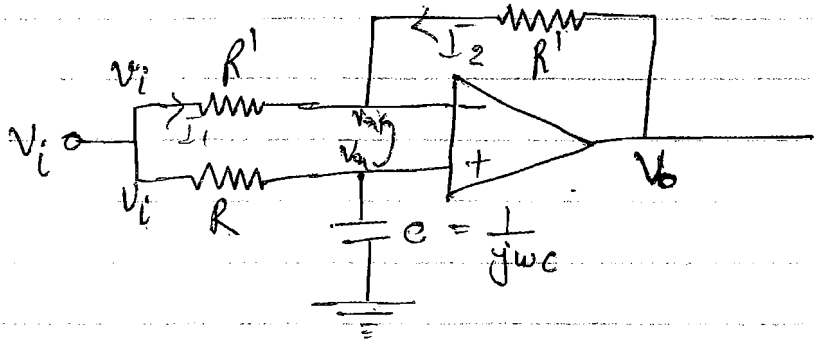
$\boxed{V_o = \sqrt{2}\sin(t-45^\circ)}$ Ans

$\sin\theta\angle -\phi$

$\sin(\theta+\phi)$ $\{\because \phi$

$-\sin(\theta-\phi)$ $\{\because$

Qus For the given circuit diagram find the ~~output~~ maximum phase difference b/w o/p and i/p.



$$V_{a2} = \frac{V_i \times \frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{V_i / j\omega C}{\frac{1 + j\omega RC}{j\omega C}}$$

$$\boxed{V_{a2} = \frac{V_i}{1 + j\omega RC}}$$

By KCL :-

$$I_1 + I_2 = 0$$

$$\frac{V_i - V_{a2}}{R} + \frac{V_o - V_{a2}}{R} = 0$$

$$\boxed{V_o = 2V_{a2} - V_i}$$

$$V_o = \frac{2V_i}{1 + j\omega RC} - V_i$$

$$V_o = V_i\left(\frac{2}{1 + j\omega RC} - 1\right)$$

* Phase Angle Problems on Properties of Logarithms

$$V_o = V_i \left[\frac{2 - (1 + j\omega RC)}{1 + j\omega RC}\right]$$

$$= V_i \left[\frac{2 - 1 - j\omega RC}{1 + j\omega RC}\right]$$

$$V_o = V_i \left[\frac{1 - j\omega RC}{1 + j\omega RC}\right]$$

$$\frac{V_o}{V_i} = \left[\frac{1 - j\omega RC}{1 + j\omega RC}\right]$$

$$\text{Phase Difference} = \left[\frac{1 + j(-\omega RC)}{1 + j(\omega RC)}\right]$$

$$= \tan^{-1}\left(\frac{-\omega RC}{1}\right) - \tan^{-1}(\omega RC)$$

$$= -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)$$

$$= -2\tan^{-1}(\omega RC)$$

∴ Maximum Phase Difference -

$$= -2\tan^{-1}(\infty)$$

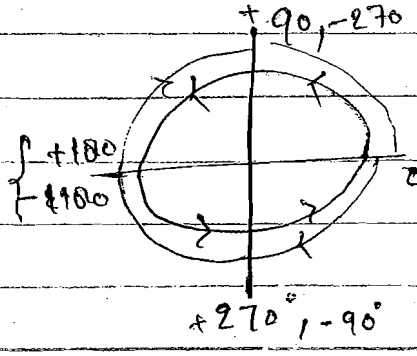
{because tan is maximum at 90°}

$$= -2 \times 90^\circ$$

$$= -180^\circ$$

$$= +180^\circ$$

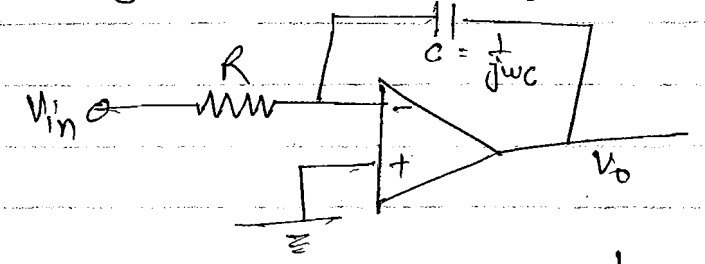
} Ans



$V_1 - V_2 = 0$ A ∞ $\boxed{V_1 = V_2}$

Note :- The Virtual short concept is fails when gain is not infinity.

Qus For the given circuit diagram calculate the voltage gain.

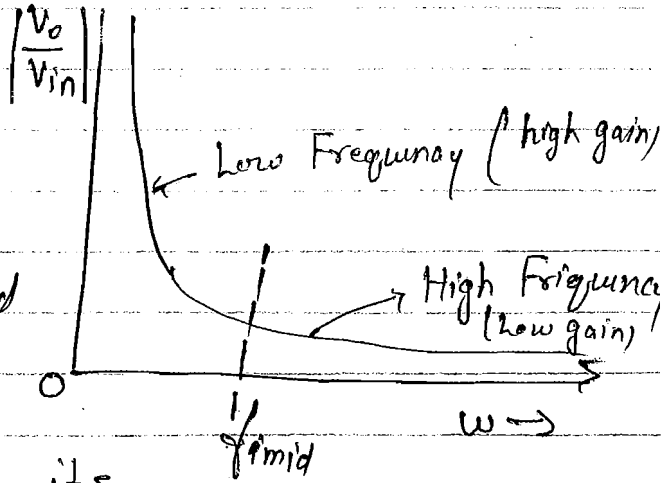


Sol^n

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1} = \frac{-\frac{1}{j\omega C}}{R} = \frac{-1}{j\omega RC}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{1}{\sqrt{0 + (\omega C)^2}} = \frac{1}{\sqrt{\omega^2 C^2 R^2}}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{1}{\omega CR}$$

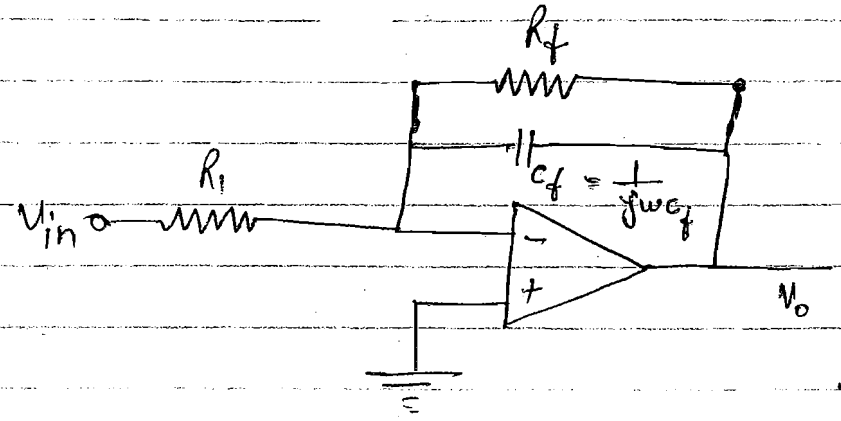


Note :- A Network which produces high gain in low freq. range is called as Low Pass Filter.

It is unstable filter becoz its gain reaches to infinity at $\omega = 0$

Filter

* Practical Low Pass Filter :-



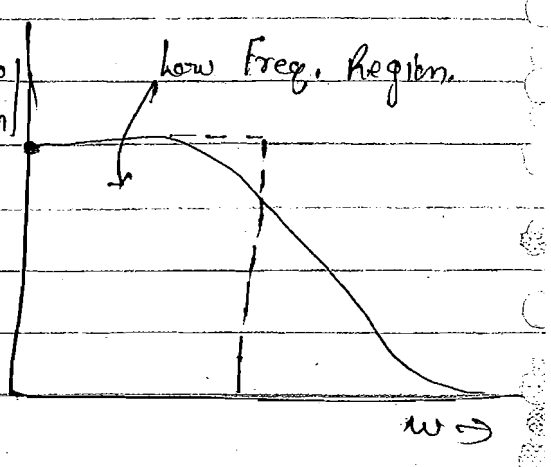
$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

$$R_{11del} = \frac{R_f \times \frac{1}{j\omega C_f}}{R_f + \frac{1}{j\omega C_f}} = \frac{R_f}{R_f j\omega C_f + 1}$$

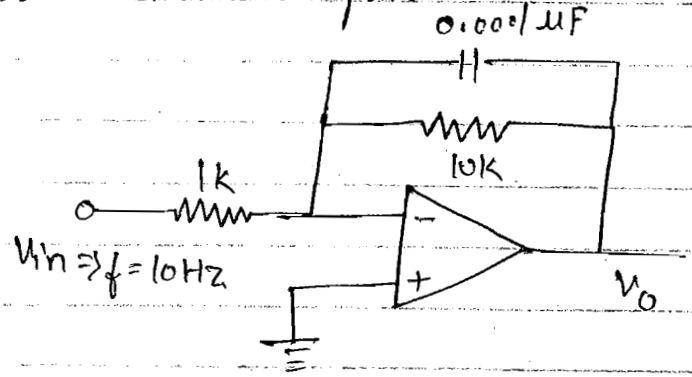
$$R_{11del} = \frac{R_f}{1 + R_f j\omega C_f}$$

$$\text{So} \quad \frac{V_o}{V_{in}} = \frac{-R_f}{1 + R_f j\omega C_f} = \frac{-R_f}{R_1(1 + j\omega C_f R_f)}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1\sqrt{1 + \omega^2 C_f^2 R_f^2}}$$



Qus For the given circuit diagram calculate magnitude of voltage gain and phase difference b/w output and input.



(a) $10, \frac{\pi}{2}$

(b) $10, \pi$ ✓

(c) $-10, \pi$

(d) $5\sqrt{2}, \frac{\pi}{2}$

Soln

$$\text{Voltage Gain } \left(\frac{V_o}{V_{in}}\right) = \frac{-R_f}{R_1\left(1+j\omega R_f C_f\right)}$$

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1\left(1+j2\pi f R_f C_f\right)}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1\sqrt{1+4\pi^2 f^2 C_f^2 R_f^2}}$$

$$= \frac{R_f}{R_1\sqrt{1+4(3.14)^2(10)^2(10)^2(0.0001\times10^{-6})^2}}$$

$$= \frac{10k}{1k\sqrt{1+4\times(3.14)^2\times10^{10-20}}}$$

$$= \frac{10}{1\sqrt{1+(3.14)^2\,4\times10^{-10}}}$$ → Very Small in Comparison of 1.

$$= \frac{10}{\sqrt{1+\text{Neglect}}}$$

$$\left|\frac{V_o}{V_{in}}\right| = 10$$ Ans

Positive Numbers — Phase Angle = 0

Negative " " " = 180

Phase Angle :-

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1(1+j\omega R_f C_f)}$$

$$= \frac{-10k}{1k\left[1+j\,2\pi\times10\times10\times10^{3}\times0.0001\times10^{-6}\right]}$$

$$= \frac{-10}{\left[1+j\,2\pi\times10^{-5}\times0.0001\times10^{-6}\right]}$$

$$= \frac{-10}{1+j\,6.25\times10^{-5}} = \frac{-10}{1+j0.0000628}$$

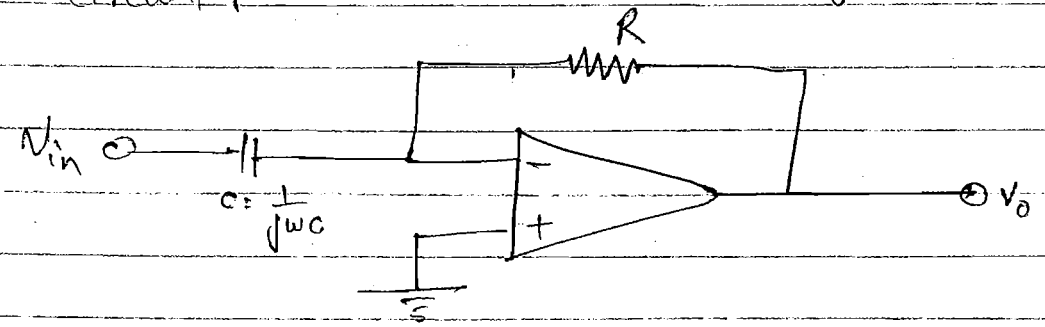
$$\angle\frac{V_o}{V_{in}} = 180 - \tan^{-1}\left(\frac{0.0000628}{1}\right)$$

$$= 180 - \tan^{-1}(0)$$

$$= 180 - 0$$

Phase diff. = 180°

Qus Find the voltage gain of the given circuit.

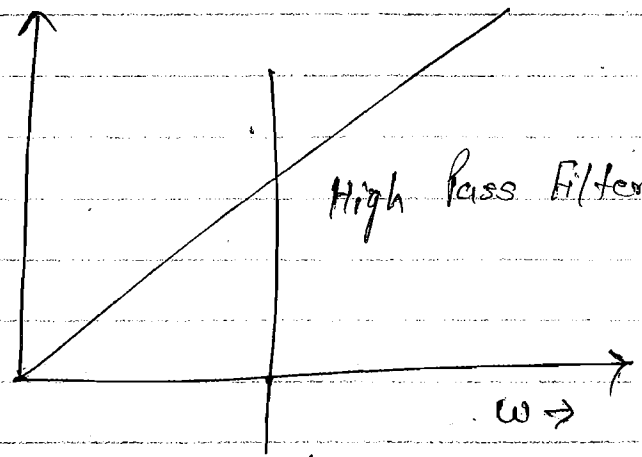


$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

$$= \frac{-R}{1/j\omega C}$$

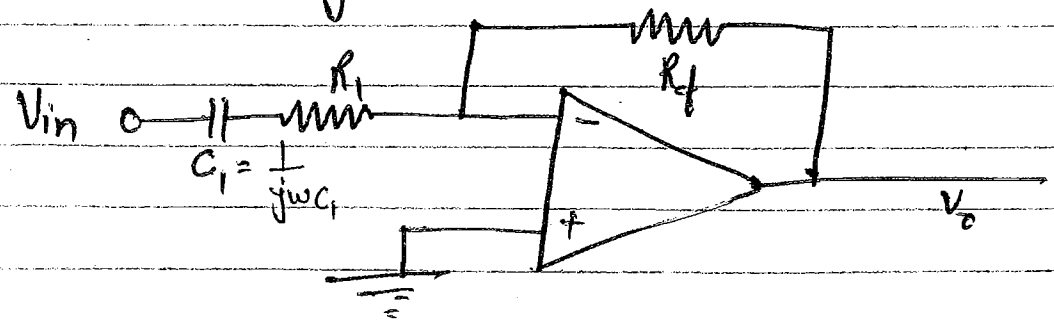
$$= -j\omega CR$$

$$\left|\frac{V_o}{V_{in}}\right| = \omega RC$$



Since gain reaches to infinity at $\omega = \infty$ so it become unstable (Impractical).

* Practical High Pass Filter :-



$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

$$= \frac{-R_f \times j\omega C_1}{1 + j\omega R_1 C_1}$$

$$R_{series} = R_1 + \frac{1}{j\omega C}$$

$$= \frac{j\omega R_1 C_1 + 1}{j\omega C}$$

$$= \frac{1 + j\omega R_1 C_1}{j\omega C}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f \omega C_1}{\sqrt{1^2 + \omega^2 R_1^2 C_1^2}}$$

$$= \frac{1}{\frac{\sqrt{1 + \omega^2 R_1^2 C_1^2}}{\omega R_f C_1}} = \frac{1}{\sqrt{\frac{1 + \omega^2 R_1^2 C_1^2}{\omega^2 R_f^2 C_1^2}}}$$

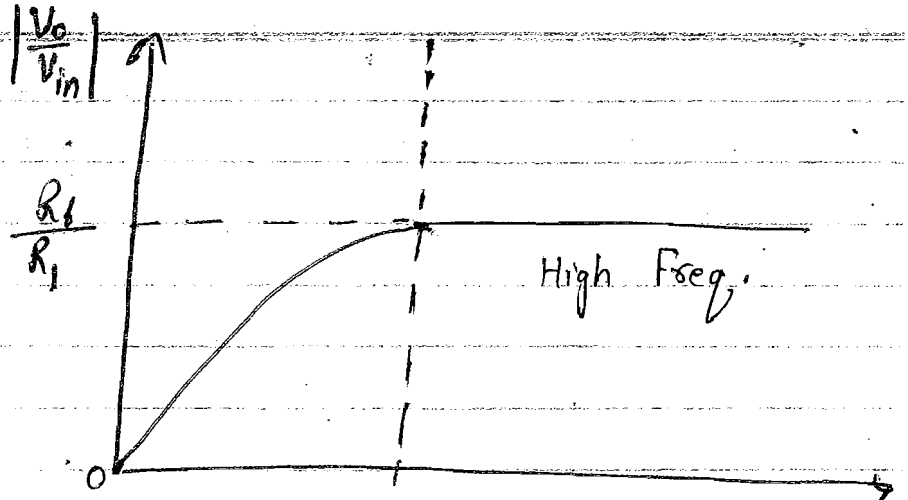
$$= \frac{1}{\sqrt{\frac{1}{(\omega R_f C_1)^2} + \frac{\omega^2 R_1^2 C_1^2}{\omega^2 R_f^2 C_1^2}}}$$

$$= \frac{1}{\sqrt{\frac{1}{(\omega R_f C_1)^2} + \frac{R_1^2}{R_f^2}}}$$

$$= \frac{1}{\sqrt{\left(\frac{R_1}{R_f}\right)^2 \left[1 + \frac{1}{(\omega R_f C_1)^2}\left(\frac{R_f}{R_1}\right)^2\right]}}$$

$$= \frac{1}{\frac{R_f}{R_1}\sqrt{1 + \frac{1}{(\omega R_1 C_1)^2}}}$$

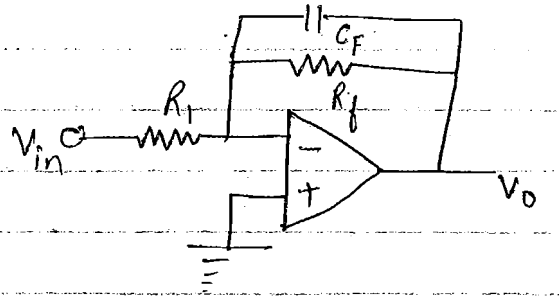
$$\boxed{\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1\sqrt{1 + \frac{1}{(\omega R_1 C_1)^2}}}}$$



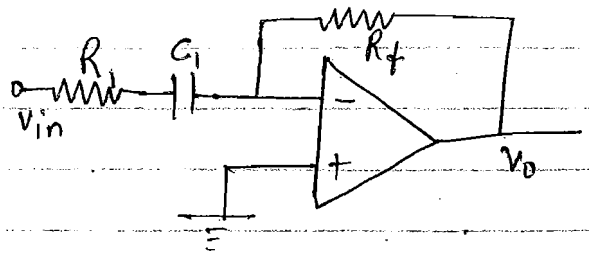
Practical High Pass Filter

* Short Trick :- {Practical} OR Stable Filter :-

L. P. F.



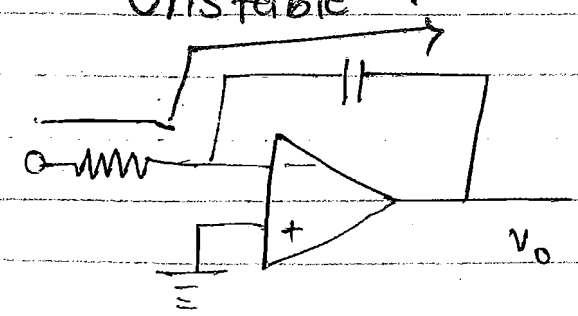
H. P. F.



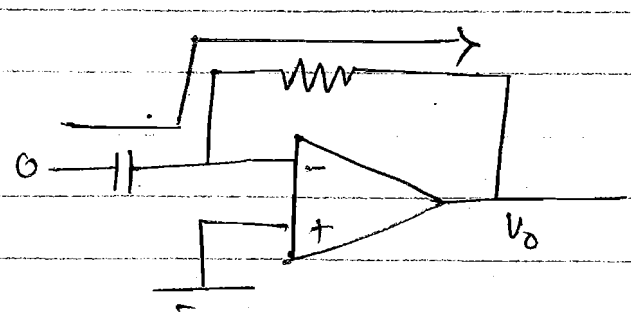
$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1\sqrt{1+(\omega R_f C_f)^2}}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1\left[\sqrt{1+\frac{1}{(\omega R_1 C_1)^2}}\right.}$$

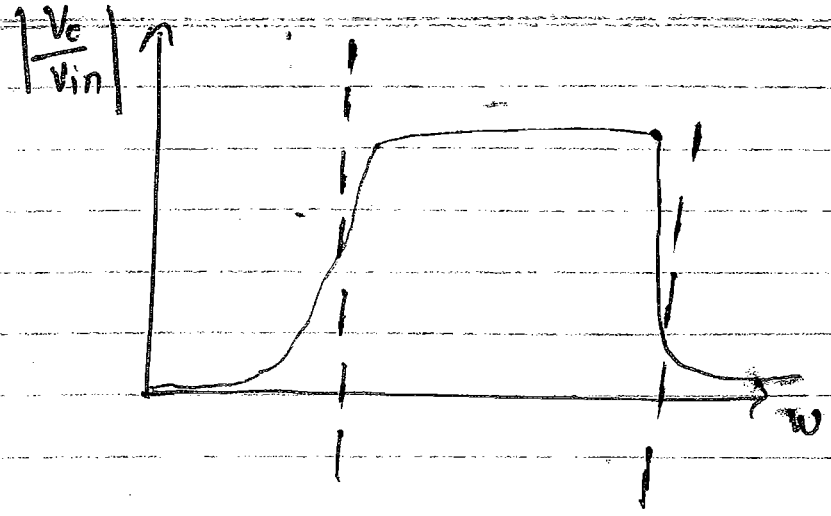
* Unstable :-



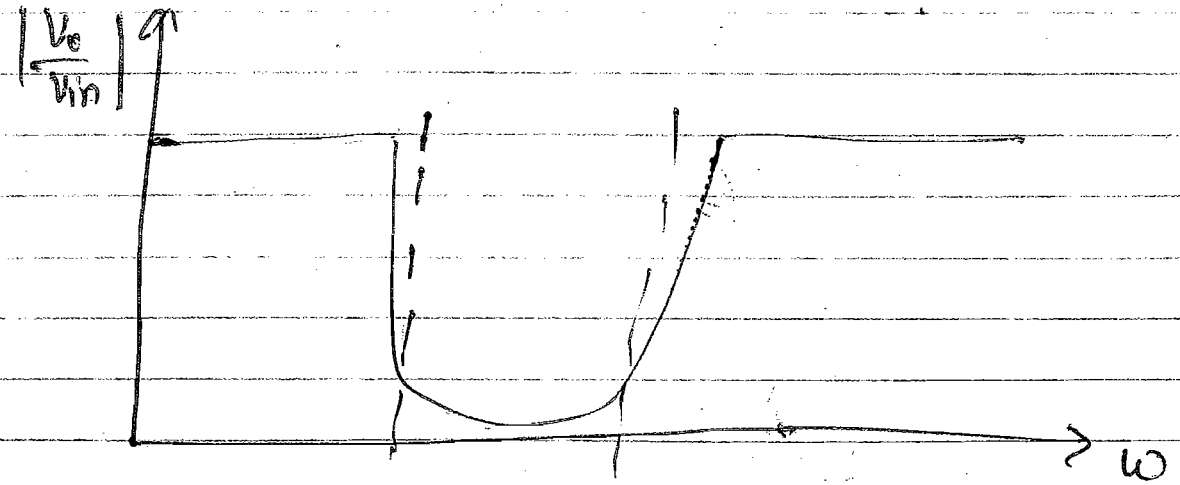
R → C → L.P.F.



C → R → H.P.F.



Band Pass Filter



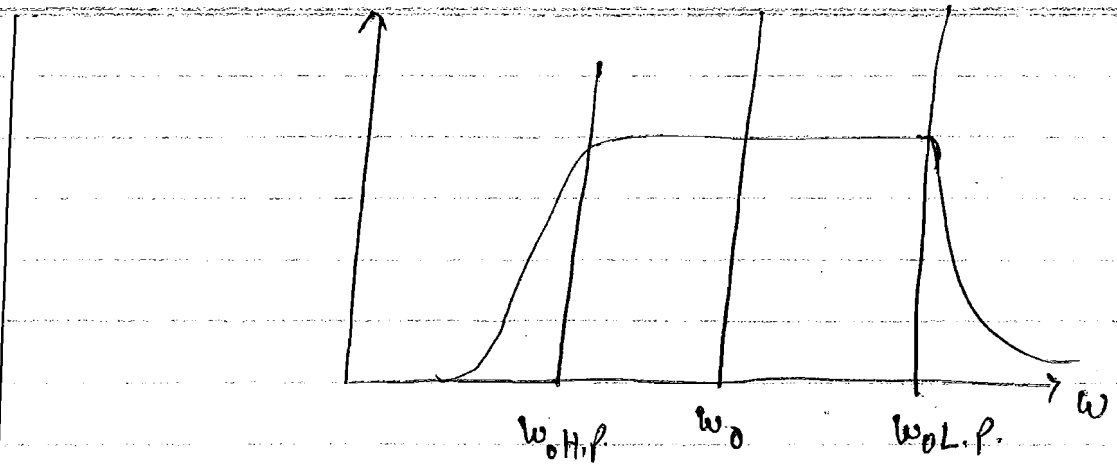
Band Reject Filter OR Band Stop Filter

2013 NET

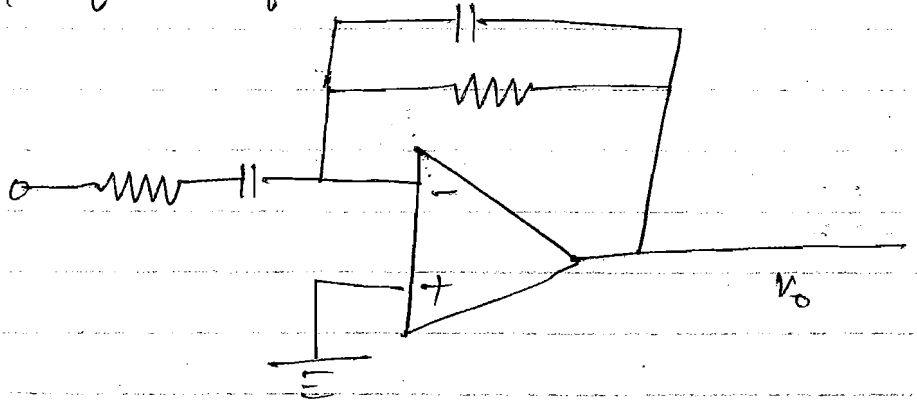
Ques A B.P.F is represented by its mid frequency ω_0 it is implemented by using H.P.F. and L.P.F. If the cut-off frequency of L.P.F. is ω_{0LP} and H.P.F is ω_{0HP} then which of the following will satisfy for Band Pass filter.

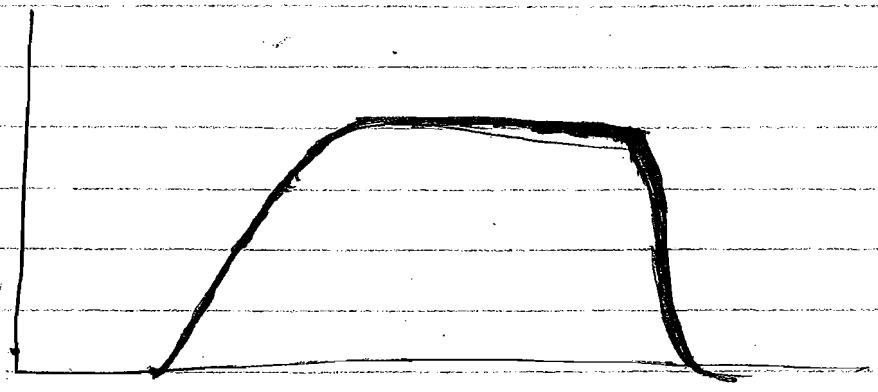
(a) $\omega_0 > \omega_{0LP} + \omega_0 > \omega_{0HP}$ (c) $\omega_0 < \omega_{0LP} + \omega_0 > \omega_{0HP}$

(b) $\omega_0 > \omega_{0LP} + \omega_0 < \omega_{0HP}$ (d) $\omega_0 < \omega_{0LP} + \omega_0 < \omega_{0HP}$



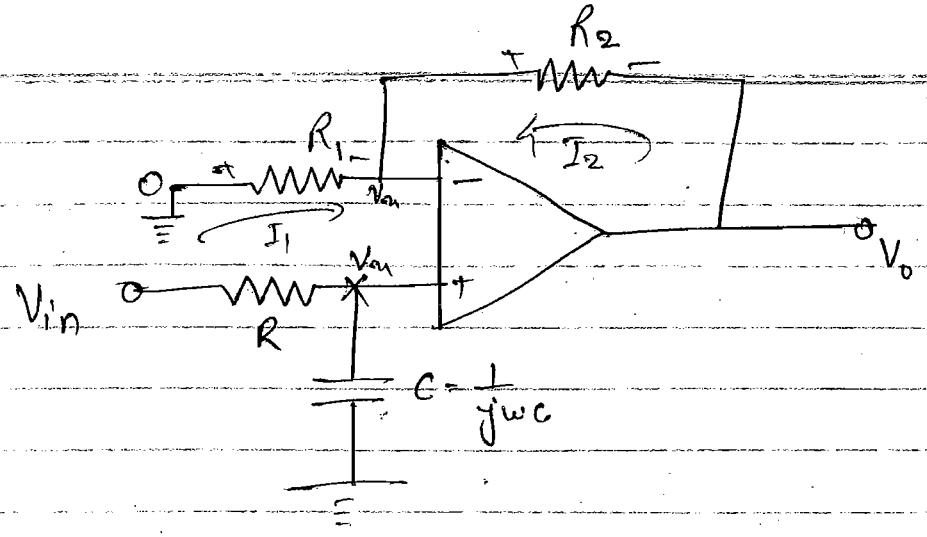
Qus for the given circuit diagram identify the type of filter.





Band Pass Filter.

Qus for the given circuit diagram identify the filter.



$$V_a = V_{in} \cdot \frac{\frac{1}{jwC}}{R + \frac{1}{jwC}} = \frac{V_{in}}{1 + RjwC}$$

$$V_a = \frac{V_{in}}{1 + RjwC}$$

By KCL :-

$$I_1 + I_2 = 0$$

$$\frac{0 - V_a}{R_1} + \frac{V_o - V_a}{R_2} = 0$$

$$\frac{V_o}{R_2} = \frac{V_a}{R_1} + \frac{V_a}{R_2}$$

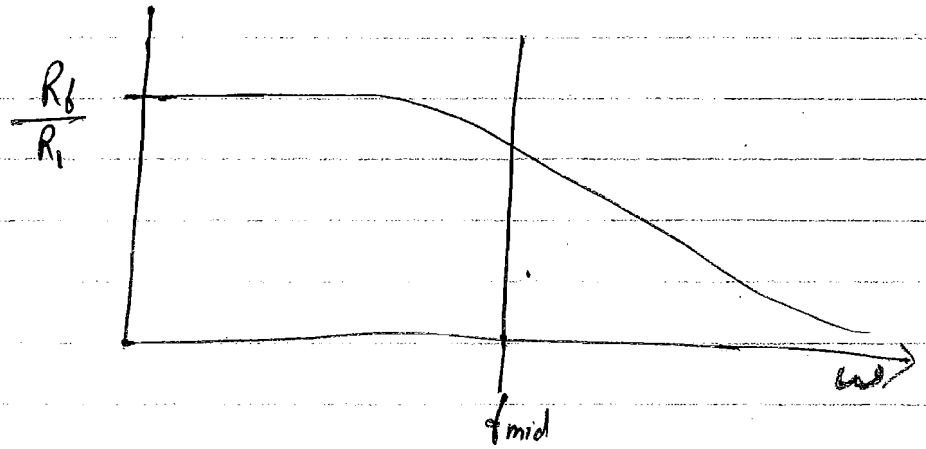
$$= V_a \left(\frac{1}{R_1} + \frac{1}{R_2} \right)$$

$$\frac{V_o}{R_2} = \frac{V_{in}}{1 + RjwC} \left(\frac{1}{R_1} + \frac{1}{R_2} \right)$$

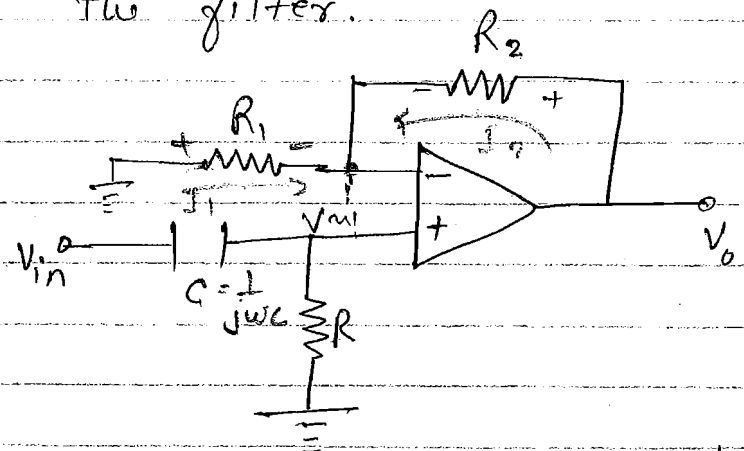
$$\frac{V_o}{V_{in}} = \frac{R_2}{1 + jwRC} \left(1 + \frac{R_2}{R_1} \right)$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{\left(1+\frac{R_2}{R_1}\right)}{\sqrt{1+w^2R^2C^2}}$$

when w increasing then $\left|\frac{V_o}{V_{in}}\right|$ decreasing So it is low Pass Filter.



Qus for the given circuit diagram identify the filter.



$$V_{a1} = \frac{V_{in}R}{R+\frac{1}{jwc}} = \frac{V_{in}(jwRC)}{1+jwRC} \quad \text{— (1)}$$

$$\frac{0 - V_{a1}}{R_1} = \frac{V_o - V_{a1}}{R_2}$$

$$\frac{-V_{a1}}{R_1} = \frac{V_0}{R_2} - \frac{V_{a1}}{R_2}$$

$$\frac{V_0}{R_2} = V_{a1}\left(\frac{1}{R_2} - \frac{1}{R_1}\right)$$

$$\frac{V_0}{R_2} = \frac{V_{in}\,R}{\left(R + \frac{1}{j\omega C}\right)}\left(\frac{1}{R_2} - \frac{1}{R_1}\right)$$

$$\frac{V_0}{V_{in}} = \frac{R_2 \cdot R}{\left(R + \frac{1}{j\omega C}\right)R_2}\left(1 - \frac{R_2}{R_1}\right)$$

$$= \frac{1}{\left(1 + \frac{1}{j\omega RC}\right)}\left(1 - \frac{R_2}{R_1}\right)$$

$$\left|\frac{V_0}{V_{in}}\right| = \frac{\left(1 + \frac{R_2}{R_1}\right)}{\left(1 - \frac{j}{\omega RC}\right)} = \frac{\left(1 + \frac{R_2}{R_1}\right)}{\sqrt{1^2 + \frac{1}{\omega^2 R^2 C^2}}}$$

$$\left|\frac{V_0}{V_{in}}\right| = \frac{\left(1 + \frac{R_2}{R_1}\right)}{\sqrt{1 + \left(\frac{1}{\omega RC}\right)^2}}$$

H. P. F

$\log \sqrt{2} = 0.15$

20|Aug|2014

* The frequency at which gain reduced by a factor of $\sqrt{2}$ that frequency is called as "Cut-off frequency" and it is given by -

$$\boxed{\omega_c = \frac{1}{R_f C_f}}$$

The factor $\sqrt{2}$ also represents 3db decrease which is given

$$\frac{1_0}{\sqrt{2}} \Rightarrow 20 \log\left(\frac{1_0}{\sqrt{2}}\right) \text{ db}$$

$$\Rightarrow 20\left[\log 1_0 - \log\sqrt{2}\right]$$

$$= 20\left[1 - 0.15\right]$$

$$= 20 - 3$$

$$= 17 \text{ d.B.}$$

$$\left(\frac{V_o}{V_{in}}\right) \Rightarrow \frac{R_f}{R_1\sqrt{1+\left(\frac{1}{\omega R_1 C_1}\right)^2}} = \frac{R_f}{R_1\sqrt{1-\frac{1}{\left(\frac{R_1 C_1}{\omega}\right)^2}}}$$

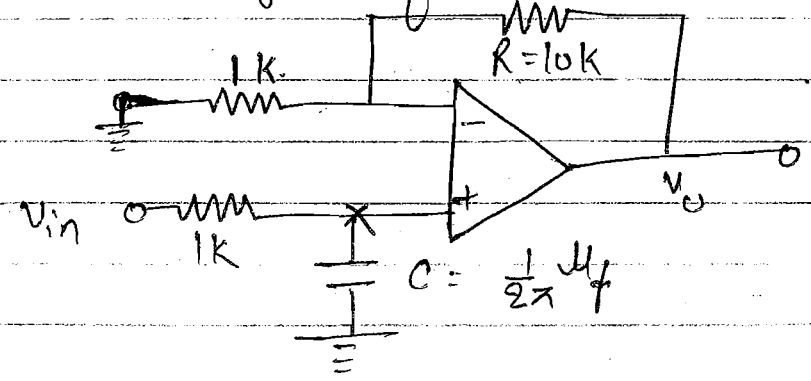
Unit of $R_1 C_1$ = Unit of ω

$$\omega_c = \frac{1}{R_1 C_1}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1\sqrt{1+\left(\frac{\omega_c}{\omega}\right)^2}}$$

The cut-off freq. defines the freq. after which gain decreases (L.P.F.) or gain increases (H.P.F.).

Ques For the given circuit diagram identify the type of filter ? and calculate the cut off frequency (Hz).



$$V_x = \frac{V_{in} \times \frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{V_{in} \times \frac{1}{j\omega C}}{\frac{Rj\omega C + 1}{j\omega C}}$$

$$\boxed{V_x = \frac{V_{in}}{1 + j\omega RC}}$$

By K.C.L –

$$I_1 + I_2 = 0$$

$$\frac{0 - V_a}{1K} + \frac{V_o - V_a}{10K} = 0$$

$$\frac{V_o}{10} = V_a + \frac{V_a}{10}$$

$$\frac{V_o}{10} = V_a \left(\frac{11}{10}\right)$$

$$V_o = \frac{11\, V_{in}}{1 + j\omega RC}$$

$$\frac{V_o}{V_{in}} = \frac{1}{1+j\omega RC}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{1}{\sqrt{1+\omega^2 R^2 C^2}}$$

Hence filter is L.P.F.

Cut of frequency $= \omega_c = \frac{1}{RC}$

$$\omega_c = \frac{1}{1 \times \frac{1}{2\pi}\mu F} \qquad (\omega_c = 2\pi f_c)$$

$$f_c = \frac{1 \times 2\pi}{2\pi \times 1 \times 1\mu F}$$

$$= \frac{10^6}{10^3}$$

$$= 10^3 \text{ Hz} \qquad \{ 1\text{Hz} = 10^0 \}$$

$$\boxed{f_c = 1 \text{ KHz}}$$ Ans

Ans ~~For the given circuit diagram iden~~

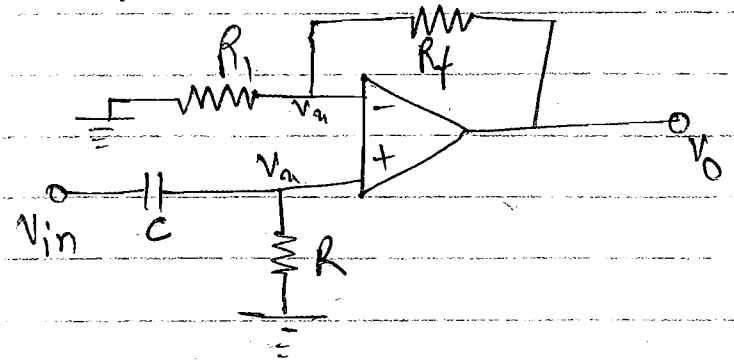
Calculate the D.C. gain :-

∴ D.C. gain for Non-Inverting Amp. $= \left(1 + \frac{R_f}{R_1}\right)$

So D.C. gain $= \left(1 + \frac{10K}{1K}\right)$

$$\boxed{\text{D.C. gain} = 11}$$

Qwy Identify the filter and find cut off freq.



Soln

$$V_a = \frac{V_{in} \times R}{1 + jwRC} \qquad V_a = \frac{V_{in} R}{\frac{1}{jwC} + R}$$

$$V_a = \frac{V_{in} R}{R}$$

$$V_a = \frac{V_{in} R^2}{1 + jwRC}$$

$$\boxed{V_a = \frac{V_{in} R\, jwC}{1 + jwRC}}$$

By K.C.L :-

$$I_1 + I_2 = 0$$

$$\frac{0 - V_a}{R_1} + \frac{V_o - V_a}{R_f} = 0$$

$$\frac{V_o}{R_f} = V_a \left(\frac{1}{R_f} + \frac{1}{R_1} \right)$$

$$V_o = V_a \left(1 + \frac{R_f}{R_1} \right)$$

$$V_o = \frac{V_{in} R\, jwC}{1 + jwRC} \left(1 + \frac{R_f}{R_1} \right)$$

$$\frac{V_o}{V_{in}} = \frac{R\, jwC}{1 + jwRC} \left(1 + \frac{R_f}{R_1} \right)$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{\omega RC}{\sqrt{1+(\omega RC)^2}}\left(1+\frac{R_f}{R_1}\right)$$

$$= \frac{1}{\sqrt{\left(\frac{1}{\omega RC}\right)^2+1}}\left(1+\frac{R_f}{R_1}\right)$$

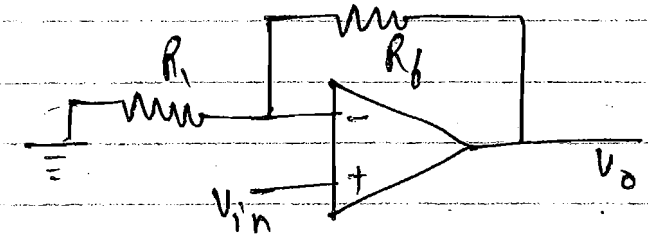
H.P.F.

$$\boxed{\omega_c = \frac{1}{RC}}$$

for D.C. gain :-

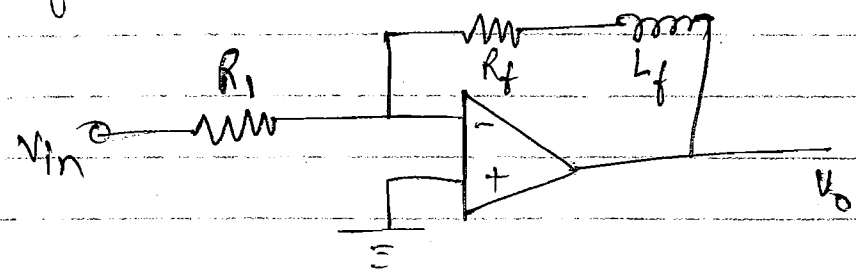
Capacitor change into breaked wire. In break wire current is zero but voltage is maximum so resistance have zero voltage.

So +ve terminal have V_{in}.



D.C. gain for non-inverting amplifier is $\left(1+\frac{R_f}{R_1}\right)$ and for inverting amplifier is $\left(\frac{-R_f}{R_1}\right)$

Qus: For the given circuit diagram identify the filter?



Sol^n

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1} = \frac{-R_s}{R_1} \quad \left(R_s = R_f + j\omega L\right)$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{\sqrt{R_f^2 + (\omega L_f)^2}}{R_1}$$

$$= \sqrt{\left(\frac{R_f}{R_1}\right)^2 + \left(\frac{\omega L_f}{R_1}\right)^2} = \sqrt{\left(\frac{R_f}{R_1}\right)^2\left[1 + \left(\frac{\omega L_f}{R_1}\right)^2 \times \left(\frac{R_1}{R_f}\right)^2\right]}$$

$$= \frac{R_f}{R_1}\sqrt{1 + \left(\frac{\omega L_f}{R_F}\right)^2}$$

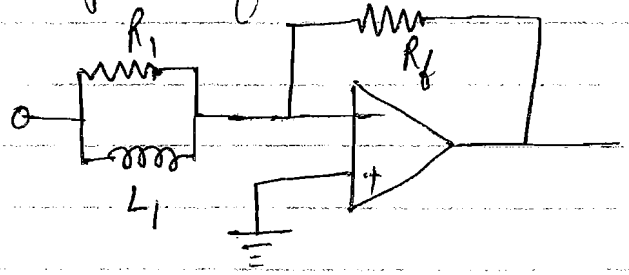
$$= \frac{R_f}{R_1}\sqrt{1 + \left(\frac{\omega}{\frac{R_f}{L_f}}\right)^2}$$

$$\omega = \frac{R_f}{L_f}$$

$$\boxed{f_c = \frac{1}{2\pi}\frac{R_f}{L_f}}$$

* Inductor ... of capacitor.

Ques For the given circuit diagram identify the type of filter.



L.P.F

Soln

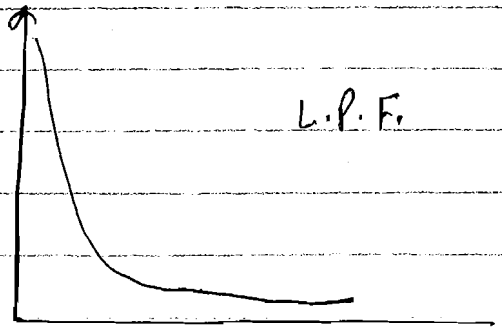
$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1} = \frac{-R_f}{R_{11}\,|\,|\,el}$$

$$= \frac{-R_f}{\frac{R_1 \cdot j\omega L_1}{R_1 + j\omega L_1}} = \frac{-R_f\,(R_1 + j\omega L_1)}{R_1 \cdot j\omega L_1}$$

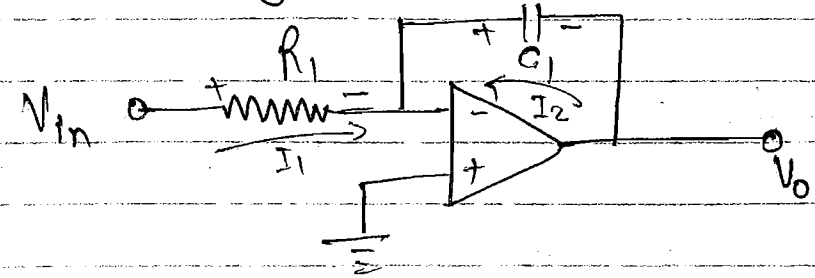
$$\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1} \frac{\sqrt{R_1 + (\omega L_1)^2}}{\omega L_1}$$

$$= \frac{R_f}{R_1} \sqrt{1 + \frac{R}{(\omega L_1)^2}}$$

Since gain decreases so L.P.F.



Qus For the given circuit diagram calculate o/p voltage. R — C



Sol^n By K.C.L. :-

$$I_1 + I_2 = 0$$

$$\frac{V_{in} - 0}{R_1} + C_1 \frac{dv}{dt} = 0 \qquad \left\{ I_c = C \frac{dv}{dt} \right\}$$

$$\frac{V_{in}}{R_1} + C_1 \frac{dv}{dt} = 0$$

$\because (V = V_0 - 0)$

means $V = V_0$

So $$\frac{V_{in}}{R_1} + C_1 \frac{dV_0}{dt} = 0$$

$$C_1 \frac{dV_0}{dt} = \frac{-V_{in}}{R_1}$$

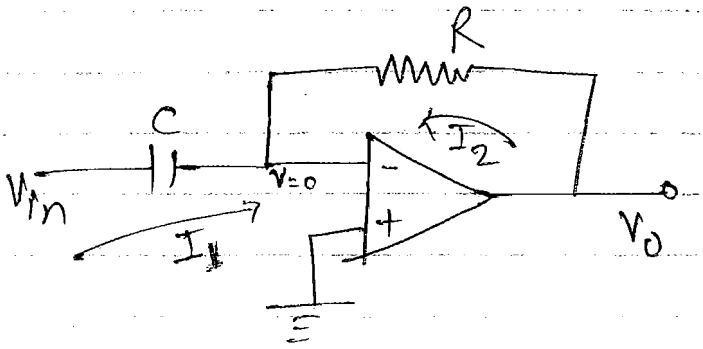
$$\frac{dV_0}{dt} = -\frac{1}{R_1 C_1} V_{in}\, dt$$

$$\int dV_0 = \int -\frac{1}{R_1 C_1} V_{in}\, dt$$

$$V_0 = \frac{-1}{RC} \int V_{in}\, dt$$

"The behaviour of low pass filter is similar to integrator circuit."

Ques



C — R

{ H.P.F. }

Sol" By K.C.L :-

$$I_1 + I_2 = 0$$

$$C\frac{dv}{dt} + \frac{V_0 - 0}{R} = 0$$

$$\frac{V_0}{R} = -C\frac{dv}{dt}$$

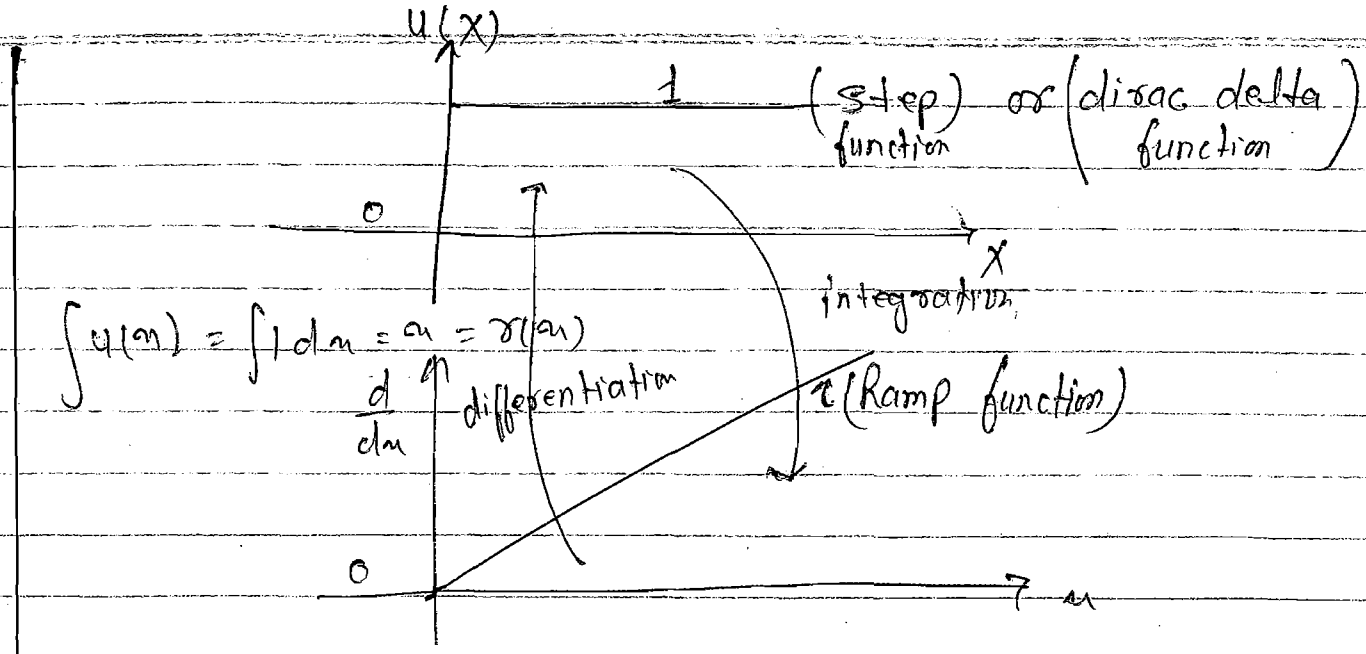
$$V_0 = -CR\frac{dv}{dt}$$

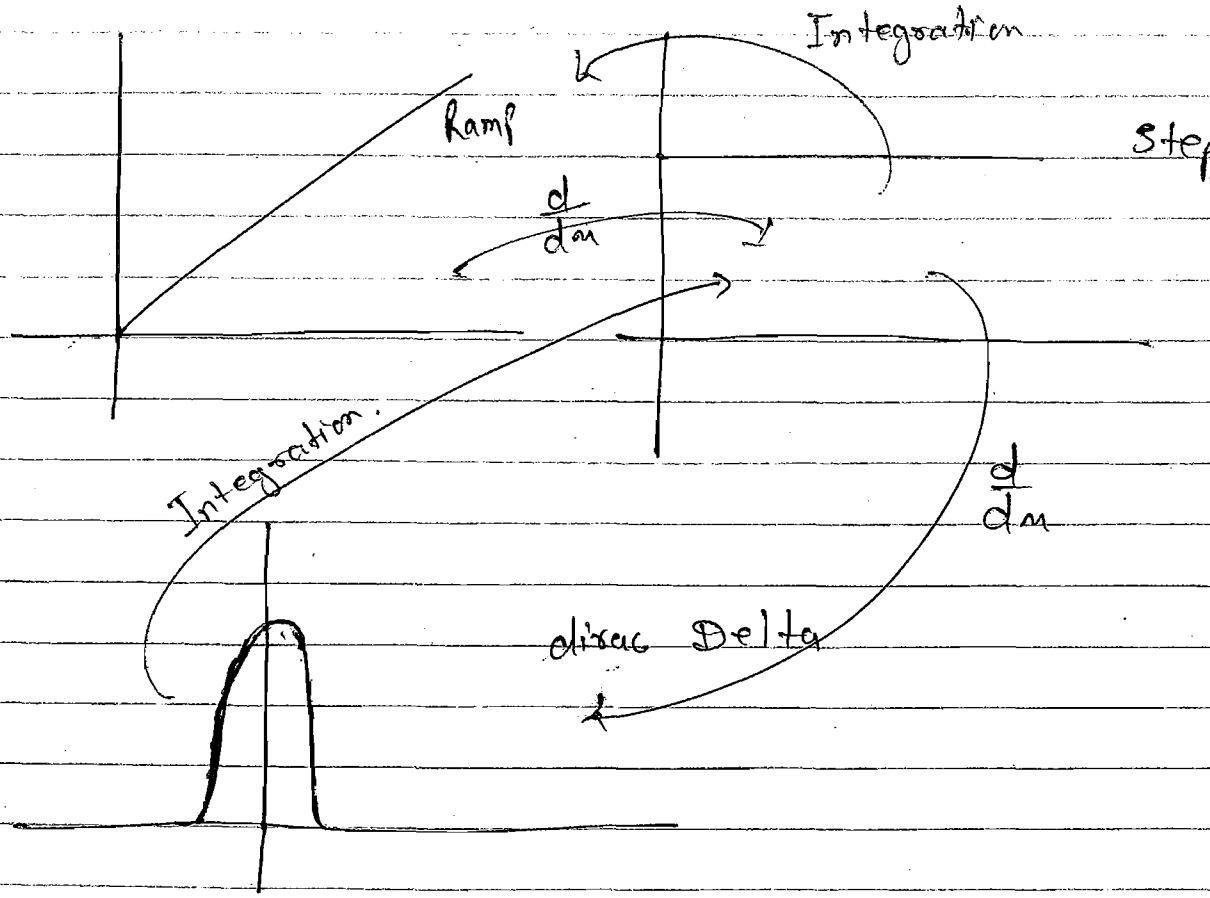
$\because$ $V_{in} = V - 0$

so $V = V_{in}$

$$V_0 = -RC\frac{dV_{in}}{dt}$$

The behaviour of high pass filter is differentiator.

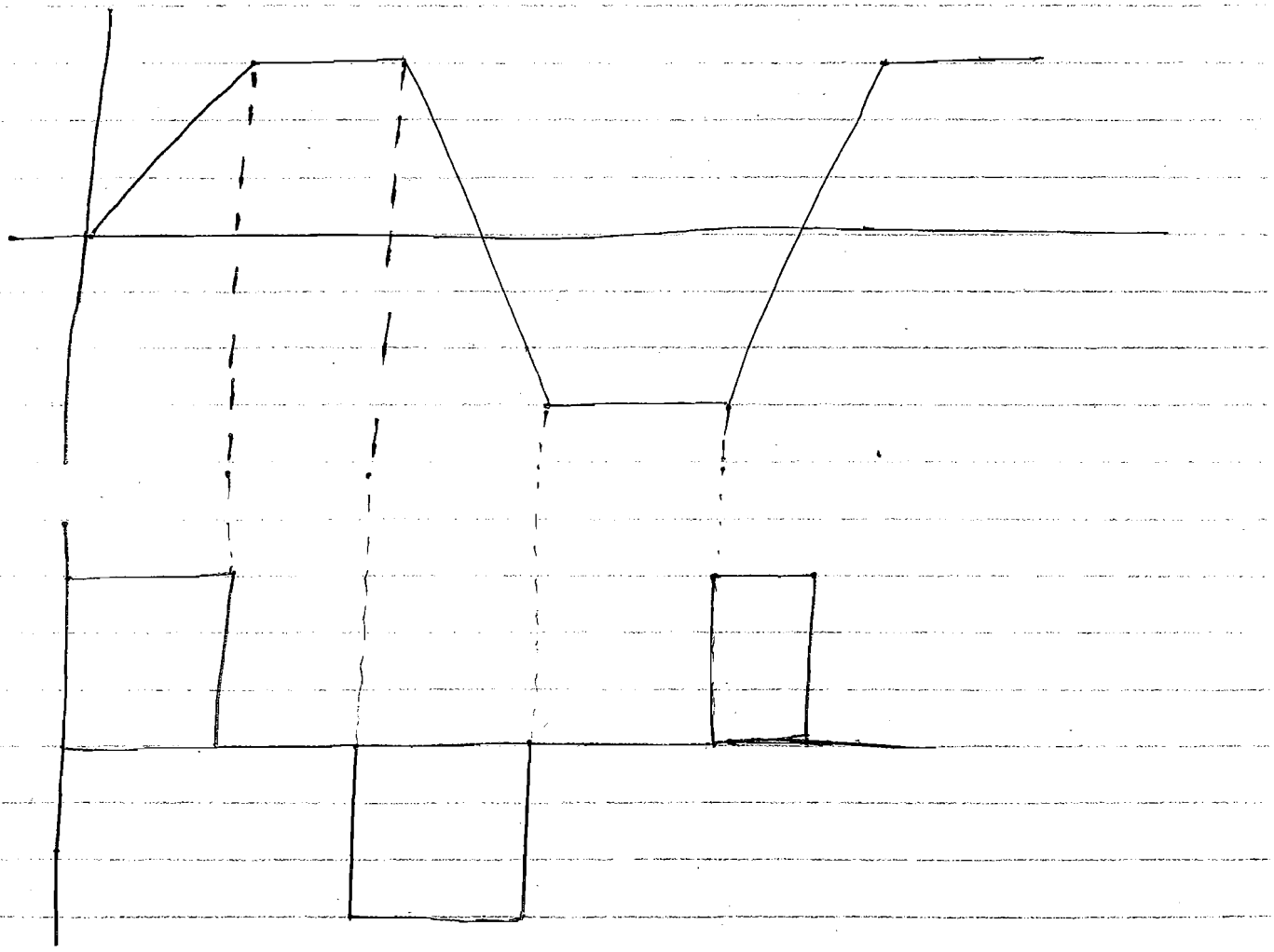




* Ramp $\xrightarrow[\text{diff}]{}$ Step $\xrightarrow[\text{diff.}]{}$ dirac delta

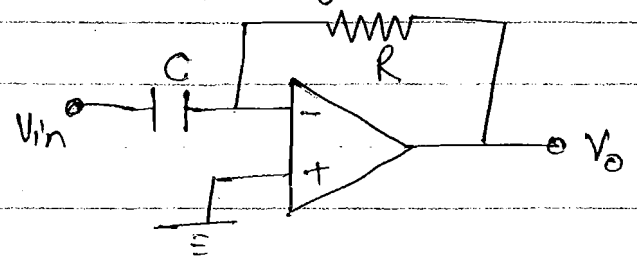
* Ramp $\xleftarrow[\text{inte}]{}$ Step $\xleftarrow[\text{inte.}]{}$ dirac delta.

Qu) The i/p, o/p waveform represented below

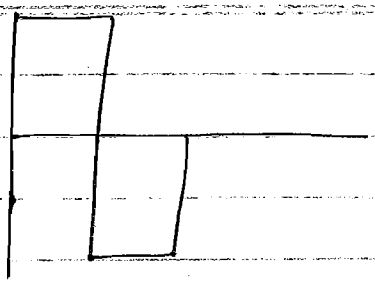


(1) Adder (2) Subtracter (3) Integrater
(4) Differentiator [✓]

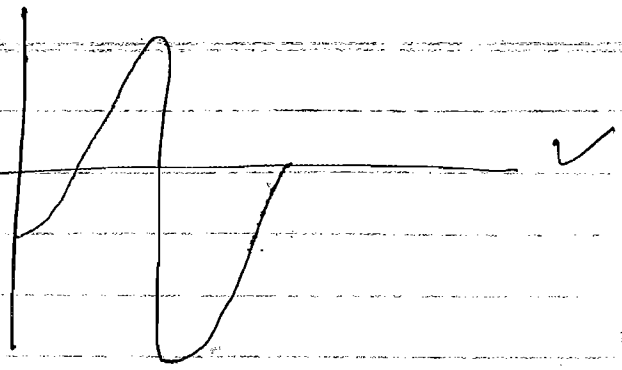
Q.2 For the given circuit diagram find the output current wave form?



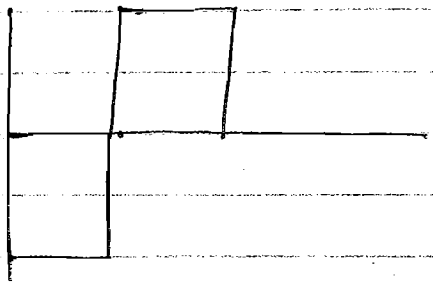
(a)



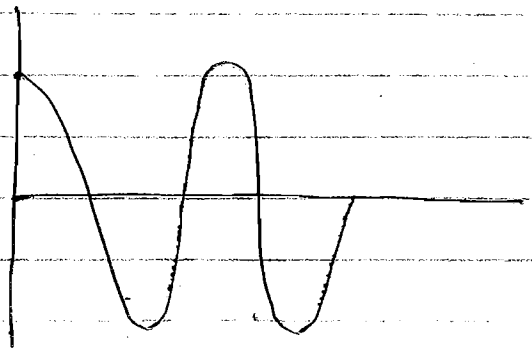
(B)



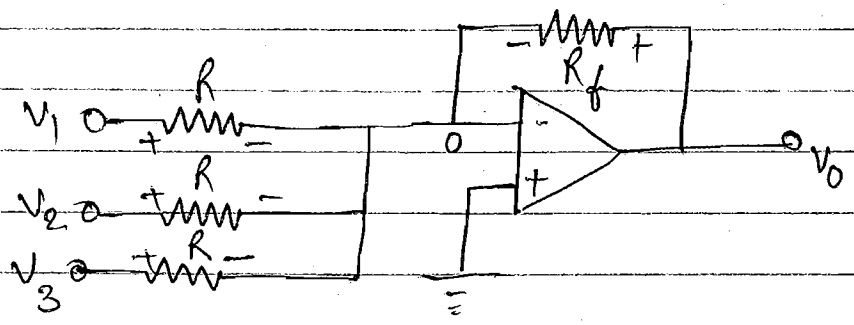
(b)



(d)



Qu Calculate output voltage?



Sol'n

$$I_1 + I_2 + I_3 + I_4 = 0$$

$$\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} + \frac{V_0}{R_f} = 0$$

$$\frac{V_0}{R_f} = -\left(\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}\right)$$

$$\frac{V_0}{R_f} = \frac{-1}{R}\left(V_1 + V_2 + V_3\right)$$

$$V_0 = -\frac{R_f}{R}\left(V_1 + V_2 + V_3\right)$$

Summing Amplifier. (Inverting).

Ques An inverting summing amplifier. output $V_0 = -0.1V_1 - 0.2V_2 - 0.4V_3$, if $R_f = 10K$ calculate R_1, R_2, R_3.

Sol^n

$$V_0 = -0.1V_1 - 0.2V_2 - 0.4V_3 \quad \text{—(I)}$$

$$V_0 = -\frac{R_6}{R_1}V_1 - \frac{R_f}{R_2}V_2 - \frac{R_6}{R_3}V_3 \quad \text{—(II)}$$

$$\frac{R_6}{R_1} = 0.1$$

$$R_1 = \frac{R_6}{0.1} = \frac{10}{0.1} = 100\,k\Omega$$

$$\boxed{R_1 = 100k\Omega}$$

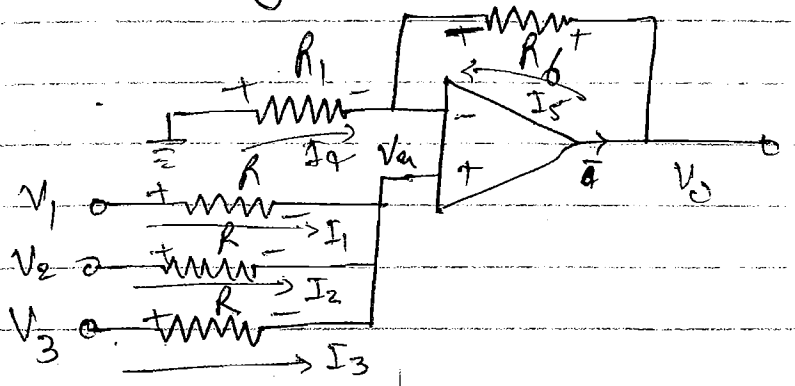
$$\frac{R_6}{R_2} = 0.2 \quad , \quad R_2 = \frac{10}{0.2} = \frac{100}{2} = 50$$

$$\boxed{R_2 = 50k\Omega}$$

$$\frac{R_6}{R_3} = 0.4 \quad , \quad R_3 = \frac{10}{0.4} = \frac{100}{4} = 25$$

$$\boxed{R_3 = 25k\Omega}$$

Qus For the given circuit diagram calculate o/p voltage?



Soln

$$I_1 + I_2 + I_3 = 0$$

$$\frac{V_1 - V_{a1}}{R} + \frac{V_2 - V_{a1}}{R} + \frac{V_3 - V_{a1}}{R} = 0$$

$$\boxed{V_{a1} = \frac{V_1 + V_2 + V_3}{3}}$$

By K.C.L :-

$$I_4 + I_5 = 0$$

$$\frac{0 - V_{a1}}{R_1} + \frac{V_0 - V_{a1}}{R_F}$$

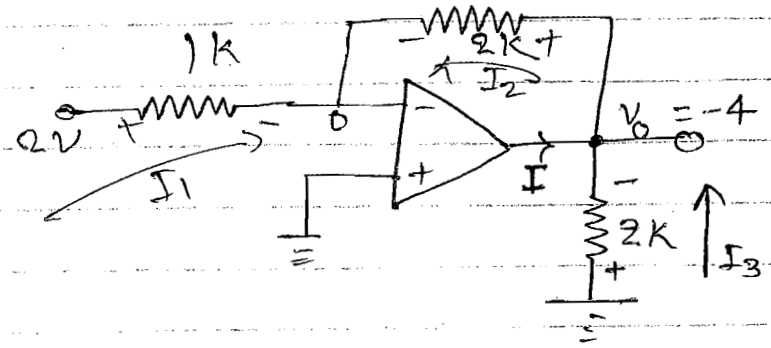
$$\frac{V_0}{R_F} = V_{a1}\left(\frac{1}{R_1} + \frac{1}{R_F}\right)$$

$$V_0 = V_{a1}\left(1 + \frac{R_F}{R_1}\right)$$

$$\boxed{V_0 = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{V_1 + V_2 + V_3}{3}\right)}$$

Averaging amp. & Also non-inverting Summing Amp.

Qus For the given circuit diagram calculate the current I.



Soln

$$I_1 + I_2 = 0$$

$$\frac{2-0}{1K} + \frac{V_0-0}{2K} = 0$$

$$\frac{V_0}{2} = -2$$

$$\boxed{V_0 = -4}$$

$$I_2 = \frac{-4-0}{2K}$$

$$= -2mA$$ (-ve show direc^n of flow of current is opposite)

OR

$$I_2 = \frac{0-(-4)}{2K} = \frac{4}{2} = 2mA.$$

$$I_3 = \frac{0-(-4)}{2} = \frac{4}{2} = 2mA.$$

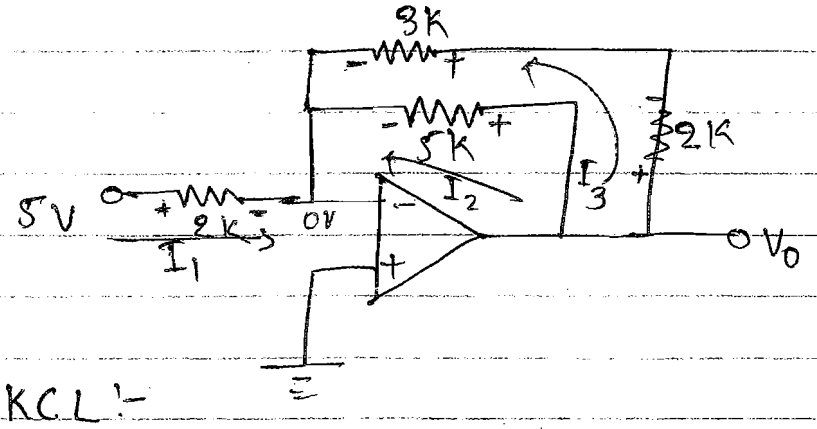
$$\boxed{I_3 = 2mA.}$$

$$I + I_2 + I_3 = 0$$

$$I + 2 + 2 = 0$$

$$\boxed{I = -4\ mA}$$

Qus for the given circuit diagram calculate the current through each and every branch.

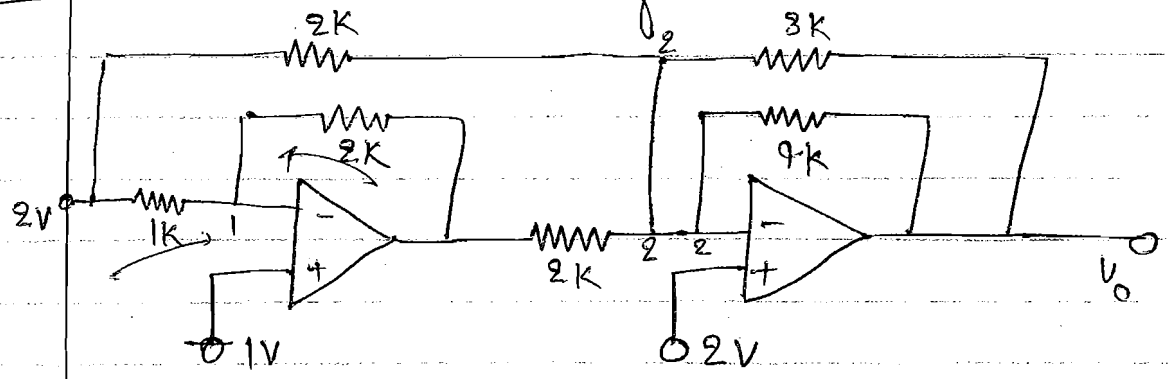


By KCL :-

$$I_1 + I_2 + I_3 = 0$$

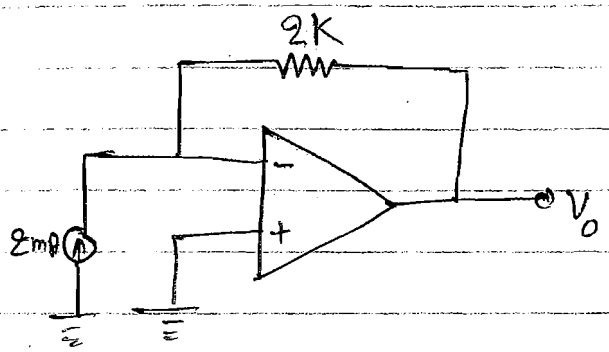
$$\frac{5-0}{2} + \frac{V_0-0}{5} + \frac{V_0-0}{2K+3K} = 0$$

Qus Calculate currents from each branch.

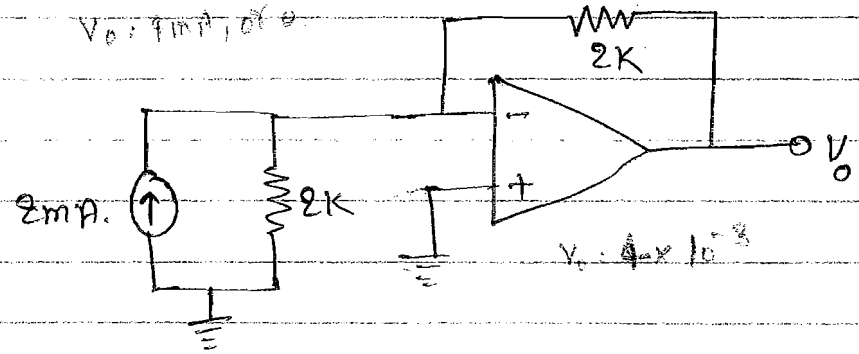


Ques1 for the given circuit diagram calculate the output voltage.

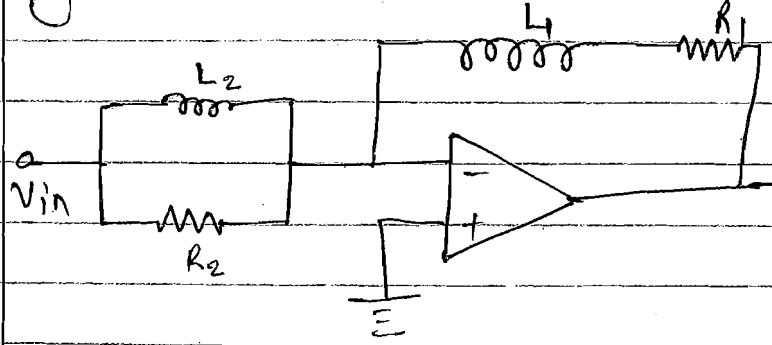
(i)



(ii)

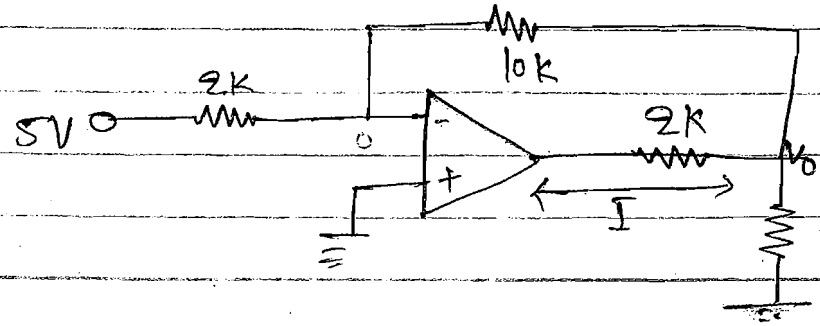


2.2 For the given circuit diagram calculate voltage gain and determine the type of filter.



$$\frac{V_o}{V_{in}} = \frac{-(R_1 + j\omega L_1)(R_2 + j\omega L_2)}{j\omega R_1 R_2}$$

Ques3 For the given op-Amp Network find the current I.

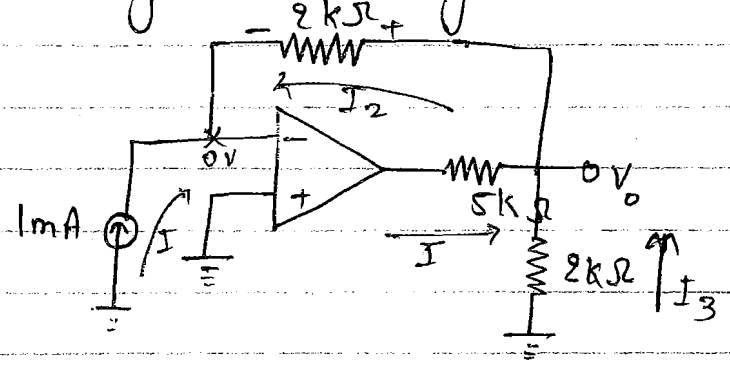


I = 0 Amp.

25/Aug/2014

Q.2. Assume OP-AMP to be Ideal, what is the value of current I, through 5kΩ register?

Sol'n



$I_1 + I_2 = 0$

$1mA + \frac{V_o - 0}{2} = 0$

$V_o = -2V$

$I_2 = \frac{V_o - 0}{2K}$

$\rightarrow \frac{-2}{-2k}$

$I_2 = -1mA$

$I_3 = \frac{V_o - 0}{2}$

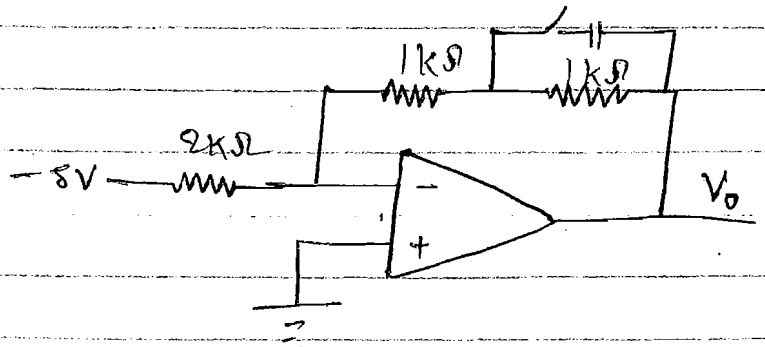
$I_3 = -1mA$

$I + I_2 + I_3 = 0$

$I + 1mA + 1mA = 0$

$I = -2mA$ Ans

Q.3



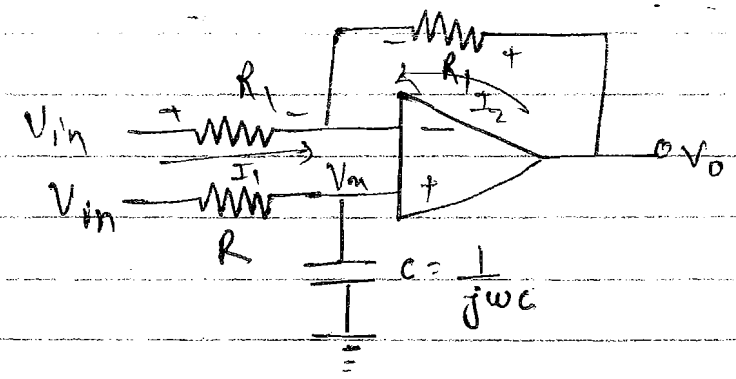
Sol^n

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1}$$

$$V_o = -5 \times -1$$

$$\boxed{V_o = +5V}$$

Q.12 Calculate the value of C if $\omega = 1000$ Rad/Sec $R = 1000\,k\Omega$, R_1 is 100Ω and phase shift between V_o and V_i is 270°



Sol^n

$$\boxed{V_m = \frac{V_{in}}{1+j\omega CR}}$$

$$I_1 + I_2 = 0$$

$$\frac{V_{in} - V_m}{R_1} + \frac{V_o - V_m}{R_1} = 0$$

$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_1} + \frac{2V_m}{R_1}$$

$$V_o = 2V_m - V_{in}$$

$$\boxed{V_o = \frac{2V_{in}}{1+j\omega CR} - V_{in}}$$

$$\frac{V_o}{V_{in}} = \frac{2}{1+jwRC} - 1$$

$$\frac{V_o}{V_{in}} = \frac{1-jwRC}{1+jwRC}$$

$$= \frac{1+j(-wRC)}{1+jwRC}$$

$$= \tan^{-1}(-wRC) - \tan^{-1}(wRC)$$

$$= -\tan^{-1}(wRC) - \tan^{-1}(wRC)$$

$$= -2\tan^{-1}(wRC)$$

$$-2\tan^{-1}(wRC) = 270 \quad 135$$

$$\tan^{-1}(wRC) = -135^{\circ}$$

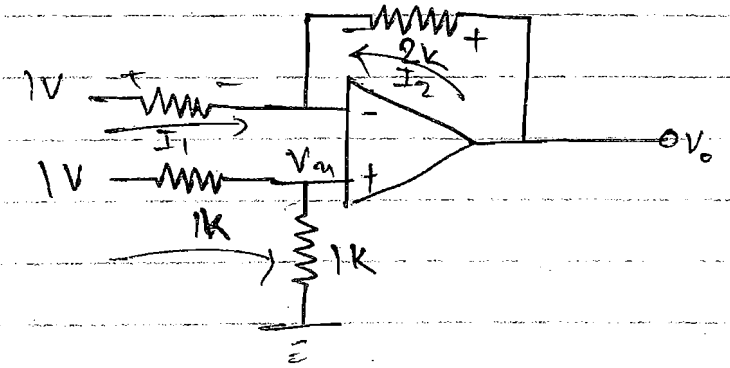
$$wRC = \tan(-135^{\circ})$$

$$1000\pi \times 100k\Omega \times C = \tan(-135)$$

$$C = \frac{\tan(-135)}{1000\pi \times 100}$$

$$C =$$

Q.15



Soln By Voltage divider Rule –

$$\frac{1 - V_a}{1} + \frac{0 - V_a}{1} = 0$$

$$1 = +2V_a$$

$$V_a = \frac{1}{2} = 0.5\,V$$

$$\boxed{V_a = 0.5\,V}$$

$$I_1 + I_2 = 0$$

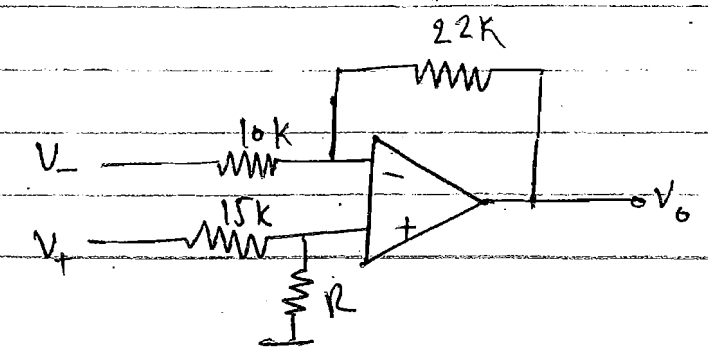
$$\frac{1 - 0.5}{1K} + \frac{V_o - 0.5}{2K} = 0$$

$$\frac{V_o - 0.5}{2} = -0.5$$

$$V_o - 0.5 = -1$$

$$\boxed{V_o = -0.5\,V}$$

Q.27



Sol^n

$$\therefore V_0 = (V_+ - V_-)\left(\frac{R_f}{R_1}\right)$$

$\therefore$ Amplification factor is same -

$$\frac{R_f}{R_1} = \frac{R_3}{R_2}$$

$$\frac{22}{10} = \frac{R}{15}$$

$$R = \frac{22 \times 15}{10} = \frac{330}{10}$$

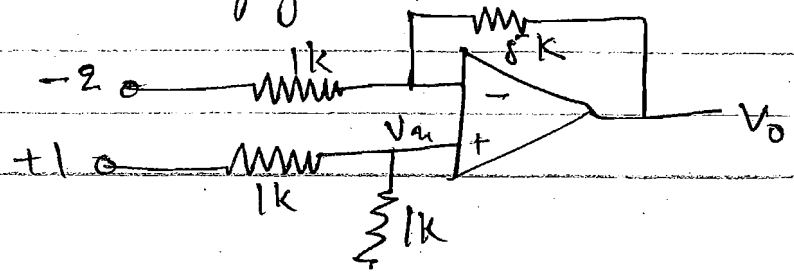
$$\boxed{R = 33\,K}$$

Q.35 Which of the following pair is/are correctly matched?

Waveform	Circuitry and input signal
1. Triangular wave 2. Impulse wave 3. Saw tooth wave	Integrating circuit and square wave

(a) 2 and 3 (b) 1 and 2 ✓ (c) 1 alone (d) 1 and 3

Q.38 The output V_0 of the ideal OP-Amp circuit shown in the figure is -



$$\frac{1 - V_a}{1} + \frac{0 - V_a}{1} = 0$$

$$+2V_a = +1$$

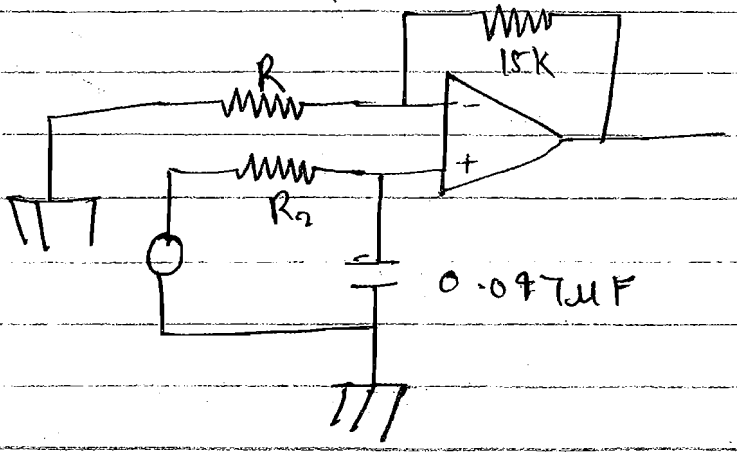
$$V_a = \frac{1}{2} = 0.5$$

$$\boxed{V_a = 0.5\,V}$$

By K.C.L —

$$I_1 + I_2 = 0$$

Q.90



Sol)

$f_c = 2kH_2$, $A = 1.5$

$$\omega_c = \frac{1}{RC}$$

$$2\pi f_c = \frac{1}{RC}$$

$$f_c = \frac{1}{2\pi RC}$$

$$= \frac{1}{2\pi R_2 C}$$

$$R_2 = \frac{1}{2\pi \times 2k \times 0.047\mu F}$$

$$= \frac{1}{2\pi \times 2 \times 0.047 \times 10^{-3}}$$

$$= \frac{10^6}{9\pi \times 47} = \frac{10^6}{9 \times 3.14 \times 47}$$

$$= \frac{1}{9\pi \times 10^3 \times 47 \times 10^{-3} \times 10^{-6}}$$

$$= \frac{10^6}{9\pi \times 47} = 1.7k$$

R_2

D.C gain $= \left(1 + \frac{R_f}{R_1}\right)$

$$1.5 = 1 + \frac{R_f}{R_1}$$

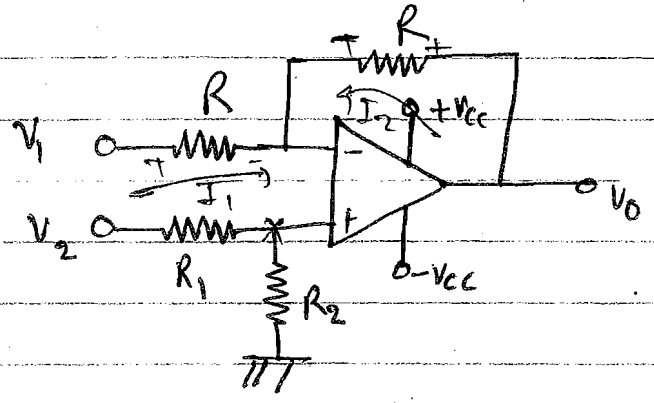
$$\frac{R_f}{R_1} = 0.5$$

$$R_1 = \frac{R_f}{0.5} = 2R_f$$

$$R_1 = 2 \times 15$$

$$\boxed{R_1 = 30\,k\Omega}$$

Q.41



Soln

$$V_a = \frac{V_2 R_2}{(R_1 + R_2)}$$

By K.C.L.

$$I_1 + I_2 = 0$$

$$\frac{V_1 - V_a}{R} + \frac{V_0 - V_a}{R} = 0$$

$$V_0 = 2V_a - V_1$$

$$\boxed{V_0 = \frac{2V_2 R_2}{(R_1 + R_2)} - V_1}$$

$\because$ in question -

$$V_0 = -V_1 + \frac{V_2}{2}$$

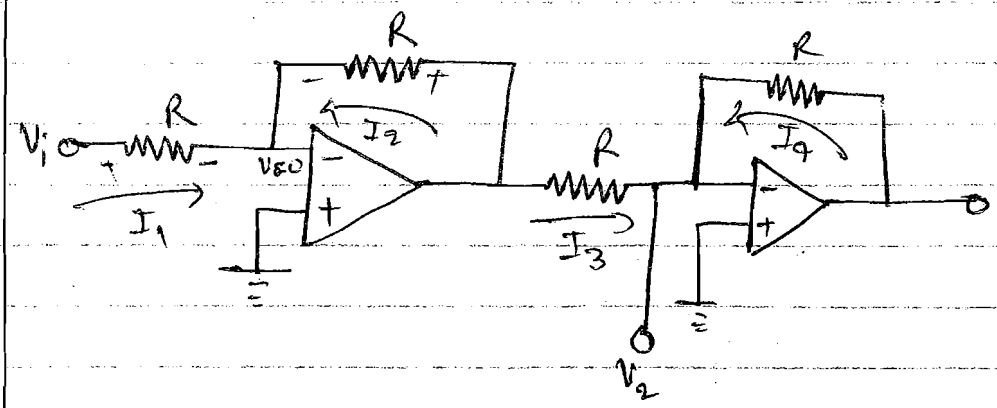
So arranging in given terms -

$$V_0 = -V_1 + V_2\left(\frac{2R_2}{R_2+R_1}\right)$$

$$-V_1 + \frac{V_2}{3} = -V_1 + V_2\frac{2}{\left(1+\frac{R_1}{R_2}\right)}$$

So $\boxed{\frac{R_1}{R_2} = 3}$ Ans

Q18



(a) Subtractor (b) Buffer Amp (c) Adder ✓
(D) divider

Sol^n

$$I_1 + I_2 = 0$$

$$\frac{V_i - 0}{R} + \frac{V_0 - 0}{R}$$

$$\boxed{V_0 = -V_i}$$

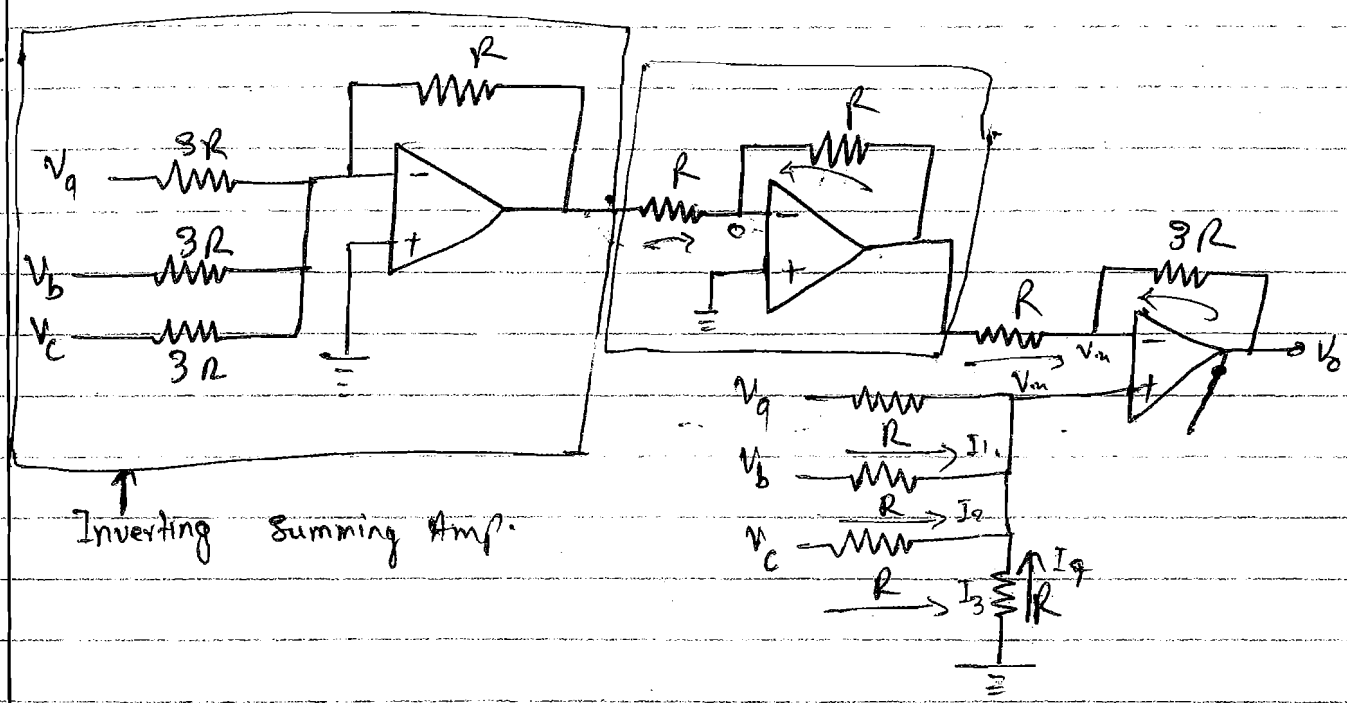
$$I_3 + I_4 = 0$$

$$\frac{-V_1 + V_2}{R} + \frac{V_0 - V_2}{R} = 0$$

$$\boxed{V_o = V_1 + 2V_2}$$

So it is adder.

Q.95



Inverting Summing Amp.

$$\text{So} \quad V_o = -\frac{R_f}{R_1}(V_1 + V_a + V_3)$$

$$= \frac{-R}{3R}(V_a + V_b + V_c)$$

$$\boxed{V_o = -\frac{1}{3}(V_a + V_b + V_c)}$$

By KCL :-

$$\frac{-\frac{1}{3}[V_a + V_b + V_c] - 0}{R} + \frac{V_{o_1} - 0}{R} = 0$$

$$\boxed{V_{o_1} = \frac{1}{3}[V_a + V_b + V_c]}$$