Q. 96

e

Soln

By K.C.L. -

$$I_1 + I_2 + I_3 + I_4 = 0$$

$$\frac{V_a - V_n}{3R} + \frac{V_b - V_n}{R} + \frac{V_c - V_n}{R} + \frac{0 - V_n}{R} = 0$$

$$V_a - V_n + V_b - V_n + V_c - V_n - V_n = 0$$

$$4V_n = V_a + V_b + V_c$$

$$V_n = \frac{1}{4}\left[V_a + V_b + V_c\right]$$

$$\frac{V_{o_1} - V_n}{R} + \frac{V_o - V_n}{3R} = 0$$

$$\frac{\frac{1}{3}\left[V_a + V_b + V_c\right] - \frac{1}{4}\left[V_a + V_b + V_c\right]}{R} + \frac{V_{o_2} - \frac{1}{3}\left[V_a + V_b + V_c\right]}{3R} = 0$$

$$\frac{V_{o_2}}{3} = \left[V_a + V_b + V_c\right]\left(\frac{1}{3} - \frac{1}{4}\right) + \frac{1}{4}\left[V_a + V_b + V_c\right]$$

$$V_{o_2} = \frac{3}{12}\left[V_a + V_b + V_c\right] + \frac{1}{4}\left[V_a + V_b + V_c\right]$$

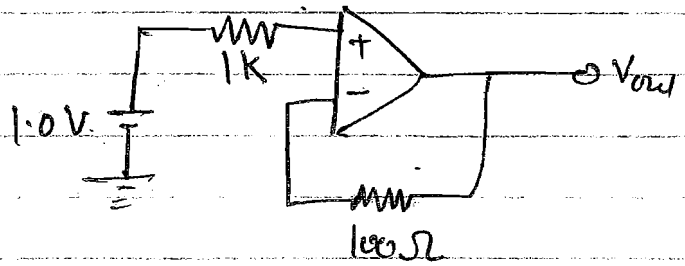
$$\frac{V_{o_2}}{3} = \frac{4V_n - V_{o_1}}{3}$$

$$\frac{V_{o_2}}{3} = \frac{4V_n - V_{o_1}}{3}$$

$$V_{O_2} = \frac{4}{4} \times \frac{(V_a + V_b + V_c)}{4} - \frac{3}{3} \times \frac{(V_a + V_b + V_c)}{3}$$

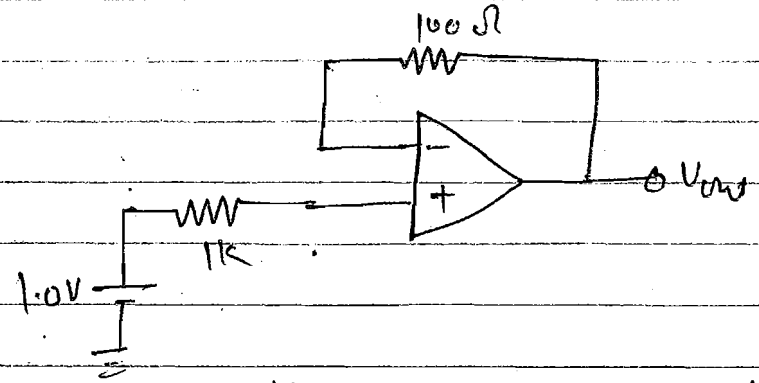
$$\boxed{V_{O_2} = 0}$$

Q.49 The o/p of the circuit on the right will be



(a) 1V (b) 11V (c) −10V (d) 0V

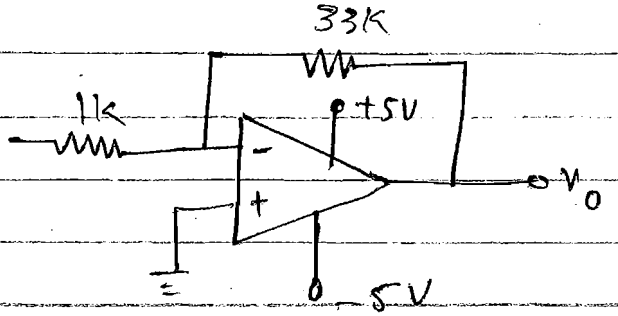
Soln



∵ it is voltage follower

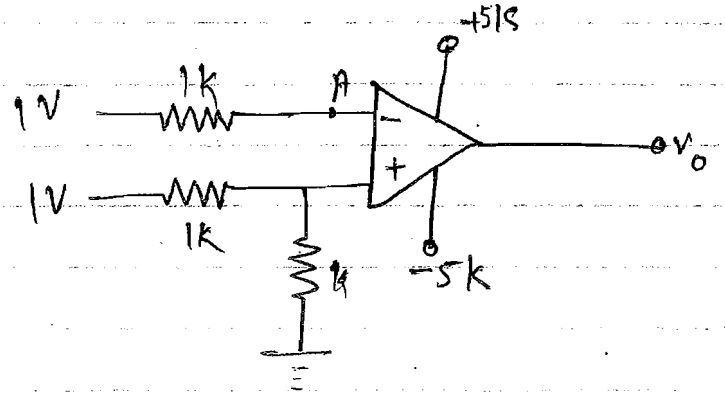
So $\boxed{V_0 = 1V}$

Q.54



Since it is inverting amp.
So it is invert in input so option (d) is correct.

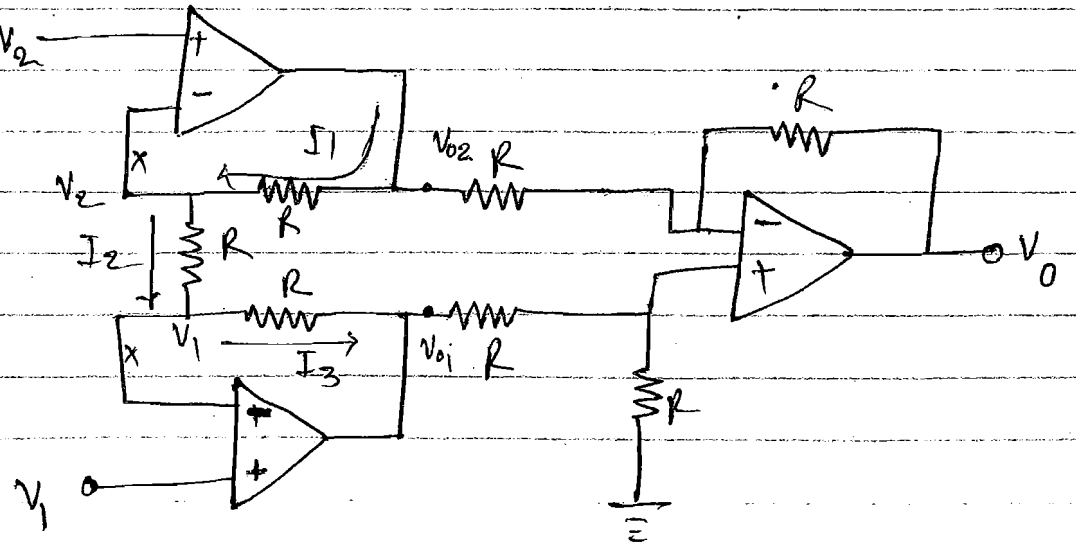
Q50



∴ there is no negative feedback so virtual shot concept are not conceder
So voltage is at A = 1 V.

JEST

Q. Calculate the voltage gain -



Soln

$$I_1 = I_2$$

$$\frac{V_{02} - V_2}{R} = \frac{V_2 - V_1}{R}$$

$$\boxed{V_{o_2} = 2V_2 - V_1}$$

$$I_2 = I_3$$

$$\frac{V_2 - V_1}{R} = \frac{V_1 - V_{o1}}{R}$$

$$\boxed{V_{o_1} = 2V_1 - V_2}$$

∴ Now it is diff. Amp.

$$V_o = (V_{o1} - V_{o2}) \frac{R_f}{R_1}$$

$$V_o = \{(2V_1 - V_2) - (2V_2 - V_1)\} \frac{R_f}{R_1}$$

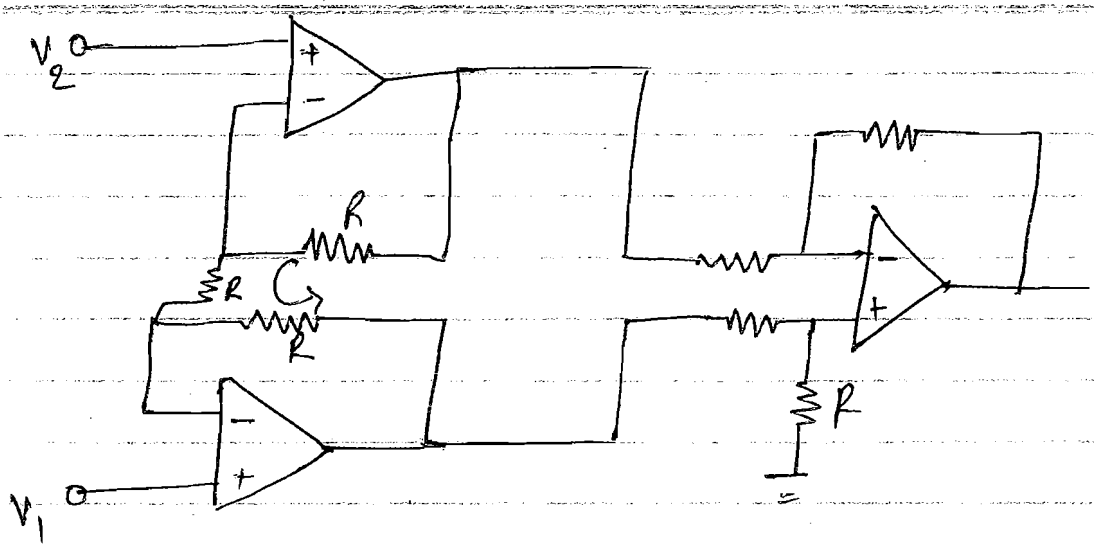
$$= \{3V_1 - 3V_2\} \frac{R_f}{R_1}$$

$$= 3(V_1 - V_2) \frac{R_f}{R_1}$$

$$\frac{V_o}{(V_1 - V_2)} = 3 \frac{R_f}{R_1}$$

$$\boxed{\frac{V_o}{(V_1 - V_2)} = 3} \quad \left\{ \because \begin{matrix} R_f = R \\ R = R \end{matrix} \right\}$$

OR

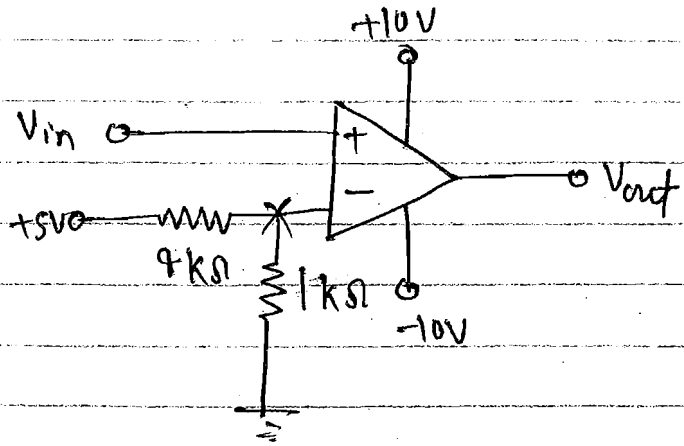


$$\left(1+\frac{2R_f}{R}\right)\left(\frac{R_6}{R_1}\right)$$

$\therefore R_6 = R$

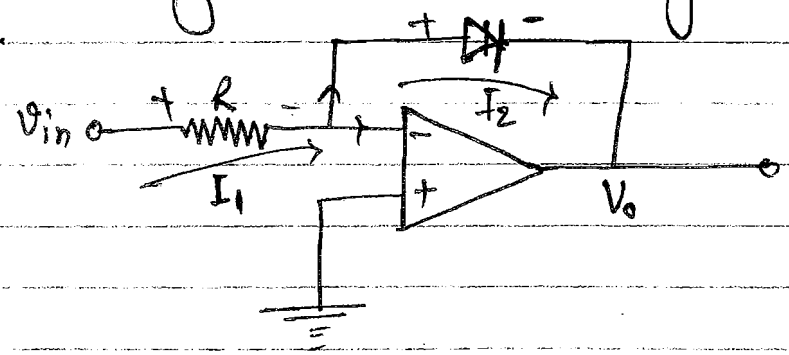
So $(1+2)1 = 3$ Ans

Q.17



So (a)

Ques for the given circuit diagram calculate o/p voltage V_o.



$$I_1 = I_2$$

$$\frac{V_i - 0}{R} = I_0 e^{V/\eta V_T} \qquad \left\{ I_D = I_0 e^{V/\eta V_T} \right\}$$

$$\frac{V_i}{R} = I_0 e^{V/\eta V_T} \qquad \left\{ \because \text{here } V = 0 - V_o = -V_o \right\}$$

$$\frac{V_i}{R} = I_0 e^{-V_o/\eta V_T}$$

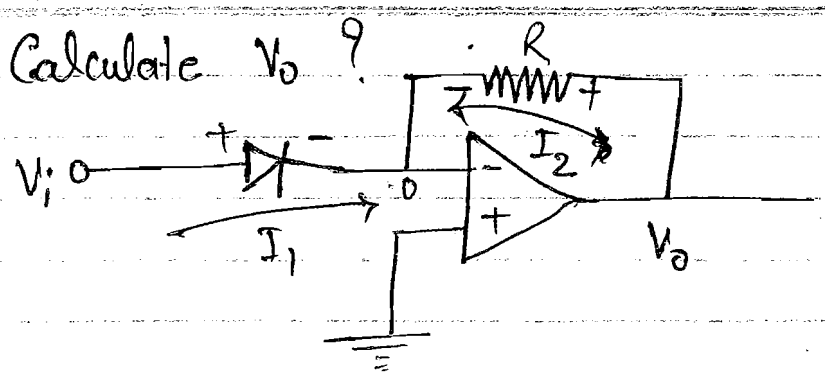
$$\frac{V_i}{I_0 R} = e^{-V_o/\eta V_T}$$

$$\ln \frac{V_i}{I_0 R} = \frac{-V_o}{\eta V_T}$$

$$\Rightarrow \boxed{V_o = -\eta V_T \ln \frac{V_i}{I_0 R}}$$

So it is logarithmic Amplifier.

Q. Calculate V_0 ?



Sol^n

$$I_1 + I_2 = 0$$

$$I_0 e^{V/\eta V_T} + \frac{V_0 - 0}{R} = 0$$

$$I_0 e^{V/\eta V_T} = -\frac{V_0}{R}$$

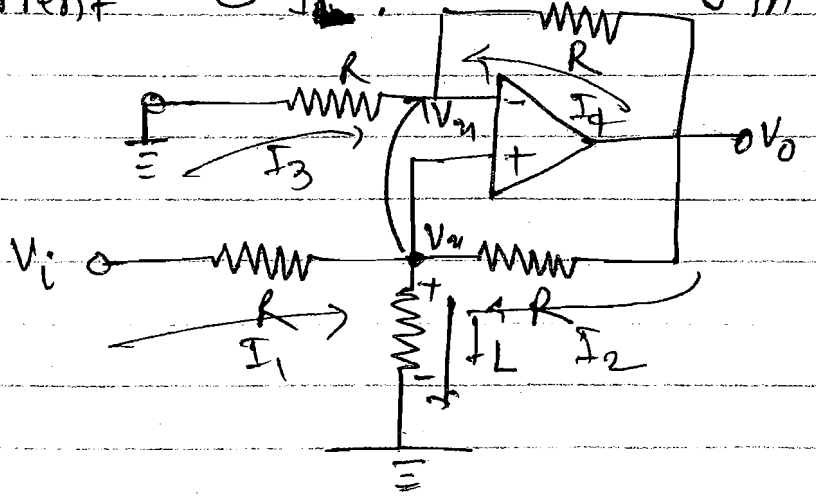
$$\boxed{V_0 = -I_0 R e^{V/\eta V_T}}$$

$\because V = V_i - 0$
$= V_i$

So $\boxed{V_0 = -I_0 R e^{V_i/\eta V_T}}$

So it is exponential Amplifier or Antilogarithm amplifier.

Q. for the given circuit diagram determine current I_L in terms of V_i.



$$I_L = \frac{V_a - 0}{R_1} = \frac{V_a}{R_L}$$

By K.C.L –

$$\frac{V_i - V_a}{R} + \frac{V_0 - V_a}{R} = \frac{V_a}{R_L}$$

$$\frac{V_i}{R} - \frac{V_a}{R} + \frac{V_0}{R} - \frac{V_a}{R} = \frac{V_a}{R_L}$$

$$\frac{V_i}{R} + \frac{V_0}{R} = \frac{V_a}{R_L} + \frac{2V_a}{R}$$

$$\frac{V_i + V_0}{R} = V_a\left(\frac{1}{R_L} + \frac{2}{R}\right)$$

$$V_i + V_0 = V_a\left[\frac{R}{R_L} + 2\right] \quad \text{— (I)}$$

Again By K.C.L :-

$$I_3 + I_4 = 0$$

$$\frac{0 - V_a}{R} + \frac{V_0 - V_a}{R} = 0$$

$$\boxed{V_0 = 2V_a} \quad \text{— (II)}$$

from (I)

$$V_i + 2V_a = V_a\left[\frac{R}{R_L} + 2\right]$$

$$V_i + 2V_a = \frac{RV_a}{R_L} + 2V_a$$

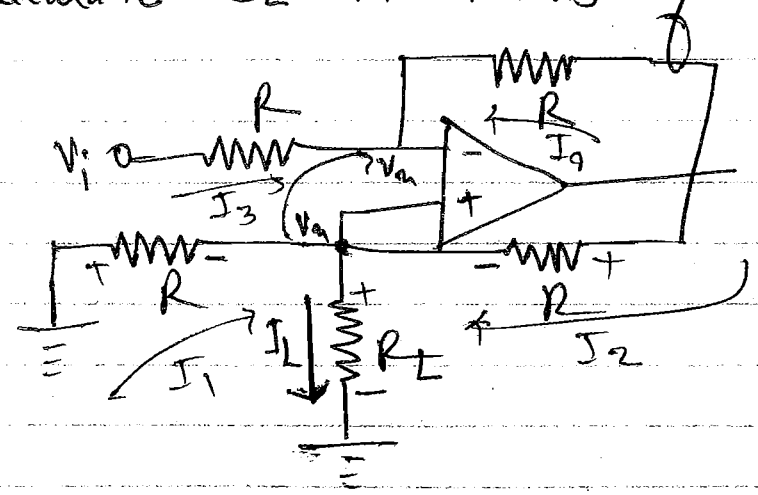
$$\boxed{V_a = V_i \cdot \frac{R_L}{R}} \quad \text{— (3)}$$

So $I_L = \frac{V_a}{R_L}$

$= V_i \cdot \frac{R_L}{R} \cdot \frac{1}{R_L}$

$$\boxed{I_L = \frac{V_i}{R}}$$

Q. Calculate I_L in terms of V_i ?



Sol^n

$$I_1 + I_2 = I_L$$

$$\frac{0 - V_a}{R} + \frac{V_0 - V_a}{R} = \frac{V_a - 0}{R_L}$$

$$-\frac{V_a}{R} + \frac{V_0}{R} - \frac{V_a}{R} = \frac{V_a}{R_L}$$

$$\frac{V_0}{R} = \frac{V_a}{R_L} + \frac{2V_a}{R}$$

$$\frac{V_0}{R} = V_a \left[\frac{1}{R_L} + \frac{2}{R} \right]$$

$$\boxed{V_0 = V_a \left[\frac{R}{R_L} + 2 \right]}$$

$$I_3 + I_4 = 0$$

$$\frac{V_i - V_a}{R} + \frac{V_o - V_a}{R} = 0$$

$$\boxed{V_i = 2V_a - V_o} \quad \text{---(11)}$$

$$V_i = 2V_a - \left[V_a \cdot \frac{R}{R_L} + 2V_a\right]$$

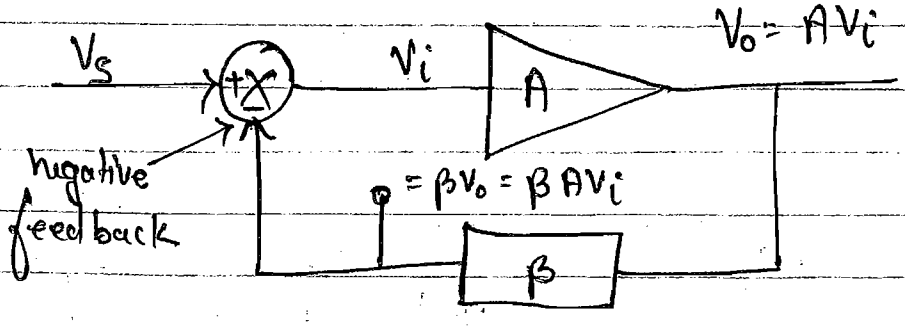
$$\boxed{V_i = -V_a \cdot \frac{R}{R_L}}$$

$$\boxed{V_a = -V_i \frac{R_L}{R}}$$

$$\therefore I_L = \frac{V_a - 0}{R_L} = \frac{-V_i R_L / R}{R_L}$$

$$\boxed{I_L = \frac{-V_i}{R}} \quad \text{Ans}$$

* Note :-



$$V_s - \beta A V_i = V_i$$

$$V_s = V_i + \beta A V_i$$

$$V_s = V_i [1 + A\beta]$$

$$V_i = \left(\frac{V_s}{1 + A\beta}\right)$$

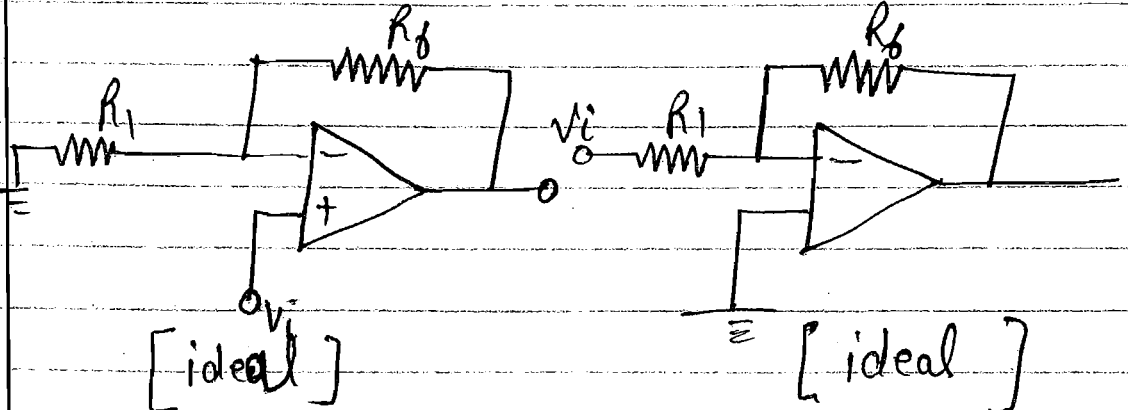
$$V_o = A \frac{V_s}{1 + A\beta}$$

$$\boxed{\frac{V_o}{V_s} = \frac{A}{1 + A\beta}} \longrightarrow (*) \quad \{\text{Memorise}\}$$

* Negative feedback is used to {decrease the gain} or provide gain in the controlled manner, the controlling parameter is $(1 + A\beta)$.

Where β = Feedback factor.

(2)



$$\boxed{\frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1}} \quad \text{for } A_{OL} = \infty \quad \boxed{\frac{V_o}{V_{in}} = \frac{-R_f}{R_1}} \quad [\text{For } A_{OL} = \infty]$$

If gain is not infinity =

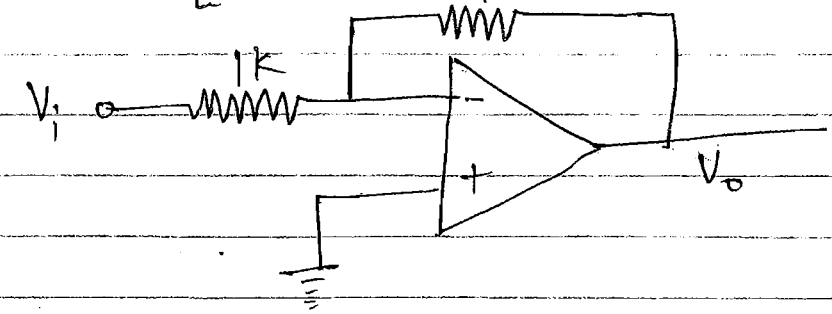
$A_{OL} \neq \infty$

$$\frac{V_o}{V_{in}} = 1 + \frac{R_6}{R_1} \quad , \quad \frac{V_o}{V_{in}} = -\frac{R_6}{R_1}$$

$$\boxed{\frac{V_o}{V_{in}} = 1 + \left(1 + \frac{R_1}{R_1}\right) \Big/ A_{OL}} \qquad \boxed{\frac{V_o}{V_{in}} = 1 + \left(1 + \frac{R_6}{R_1}\right) \Big/ A_{OL}}$$

Ques for the given circuit diagram calculate the closed loop voltage gain if open loop gain $A_{OL} = 50$

Sol^n =



$\because A_{OL} = 50$

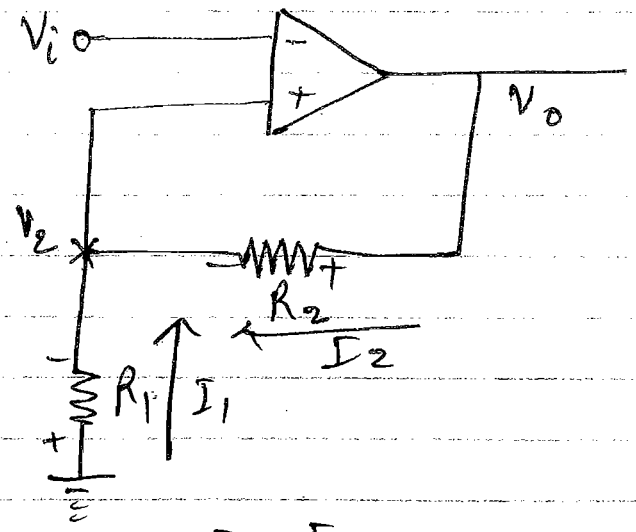
$$\frac{V_o}{V_{in}} = \frac{-R_6}{1 + \frac{\left(1 + \frac{10K}{1K}\right)}{50}}$$

$$\frac{V_o}{V_{in}} = \frac{-10}{1 + \frac{11}{50}} = \frac{-500}{61}$$

$$\boxed{\frac{V_o}{V_{in}} = -8.196}$$ Ans

* Positive Feedback Op-Amplifier:-

The basic circuit diagram is used for positive feedback is Schmitt trigger. it is a square wave generator also called as regenerative comparator. The basic operation of positive feedback is similar to open loop condition.



$$I_1 + I_2 = 0$$

$$\frac{0 - V_2}{R_1} + \frac{V_o - V_2}{R_2} = 0$$

$$\frac{-V_2}{R_1} - \frac{V_2}{R_2} = -\frac{V_o}{R_2}$$

So $$\frac{V_o}{R_2} = V_2\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$\Rightarrow \boxed{\frac{V_2}{R_2} = \frac{R_1 R_2 V_o}{(R_1 + R_2)}}$$

$$\frac{V_o}{R_2} = \frac{(R_2+R_1)}{R_2 R_1} V_2$$

$$\boxed{V_2 = \frac{V_o R_1}{(R_1+R_2)}}$$

Case I :- $V_2 > V_i \Rightarrow V_o = +V_{sat}$

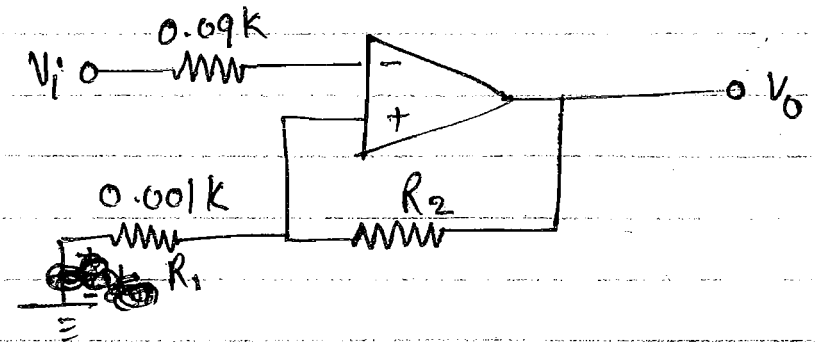
So $\boxed{V_2 = \frac{+V_{sat} \cdot R_1}{R_1+R_2}} = V_{UT}$ = Upper Threshold voltage.

Case II :- $V_2 < V_i \Rightarrow V_o = -V_{sat}$

$\Rightarrow \boxed{V_2 = \frac{-V_{sat} \cdot R_1}{R_1+R_2}} = V_{LT}$

Here $\boxed{\beta = \frac{R_1}{R_1+R_2}}$ = feed back factor.

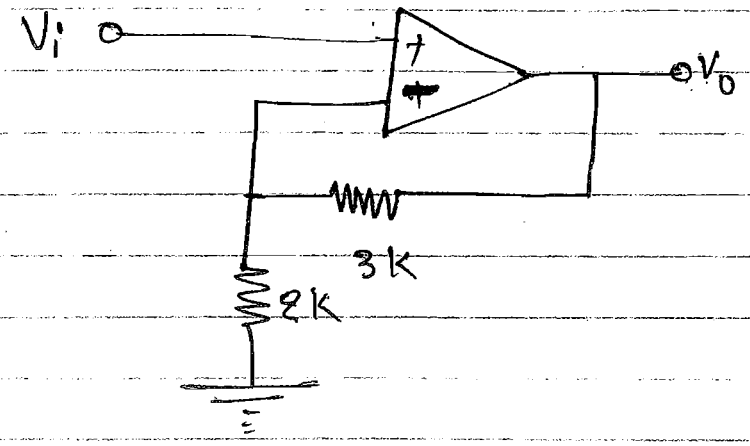
Q.5 Feedback factor (β) of circuit is -



(a) 0.33 (b) 0.67 (c) Data is insufficient

(d) 0.03.

Q. For the given circuit diagram calculate overall input resistance and overall output resistance with feed back shown in figure.



$A_{OL} = 10^6$

$R_{in} = 10\,K\Omega$

$R_O = 2k$

$R_{in}' = ?$

$R_O' = ?$

Soln

$$\beta = \frac{R_1}{R_1 + R_2}$$

$$= \frac{2k}{2k+3k} = \frac{2K}{5K} = 0.4$$

$$\boxed{\beta = 0.4}$$

$$R_{in}' = R_{in}(1 + A\beta) \quad \{\because R_{in}' \to \infty\}$$

$$R_O' = \frac{R_O}{(1 + A\beta)} \quad \{\because R_O' \to 0 \text{ for op-amp}\}$$

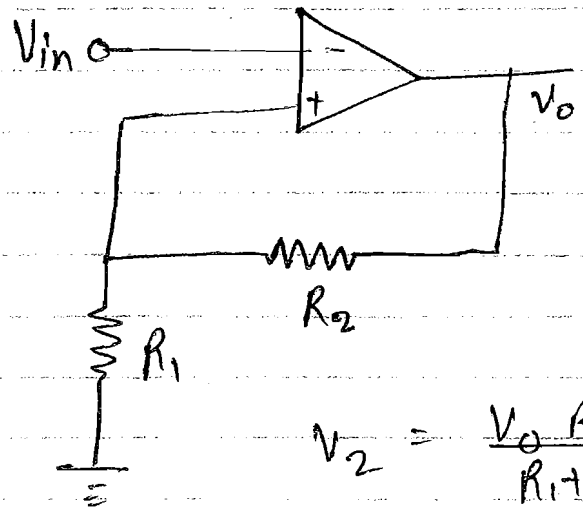
So $R_{in}' = 10k\,[1 + 10^6 \times 0.4] = 10 + 10^6 \times \frac{10^3 \times 2}{5}$

$= (10 + 4 \times 10^6) =$

$$R_O' = \frac{2k}{1 + 10^6 \times 0.4} = \frac{2}{1 + 10^6 \times \frac{2}{5}}$$

=

*



$$V_2 = \frac{V_o R_1}{R_1 + R_2}$$

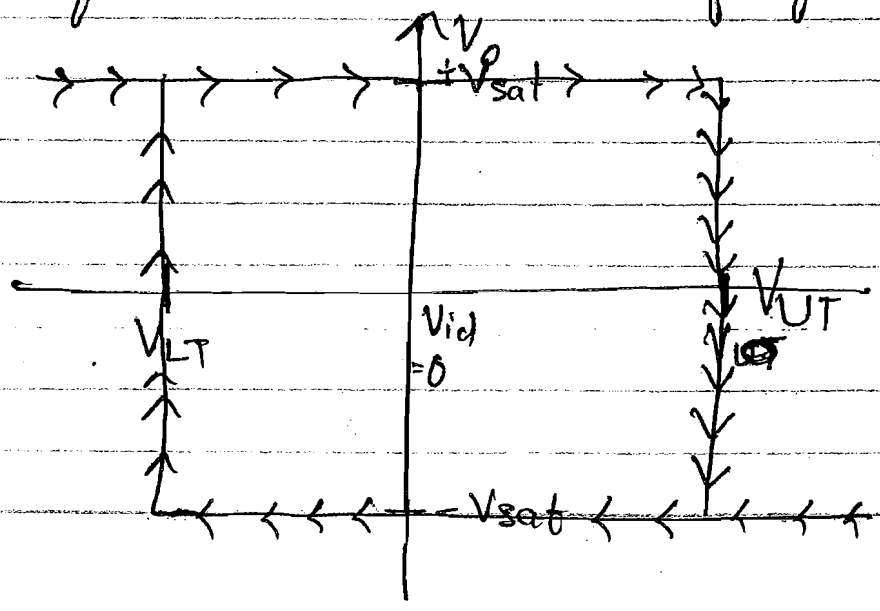
$V_2 \geq V_{in}$ $\quad V_o = +V_{sat}$

So $\boxed{V_2 = \frac{+V_{sat} R_1}{R_1 + R_2}} = V_{UT}$

When $V_2 < V_{in}$ $\quad V_o = -V_{sat}$.

$$\boxed{V_2 = \frac{-V_{sat} R_1}{R_1 + R_2} = V_{LT}}$$

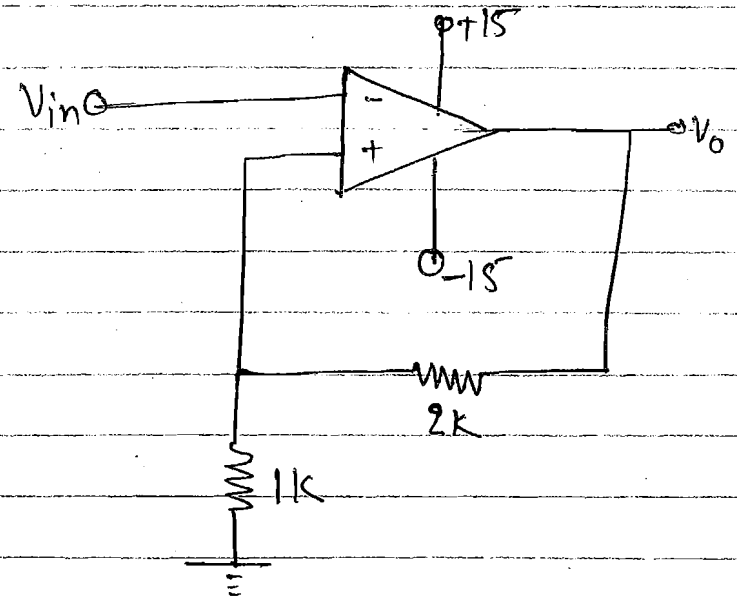
* Transfer Characteristics of feedback Op-Amp:-



$$V_H = V_{UT} - V_{LT}$$

V_H = Hysteresis Voltage

Ques for the given circuit diagram draw the transfer characteristic and hence calculate Hysteresis voltage.



Sol:

$$V_2 = \frac{V_o R_1}{R_1 + R_2}$$

{ Consider R_1 which is nearer to ground }

$$= \frac{V_o \cdot 1K}{1K + 2K}$$

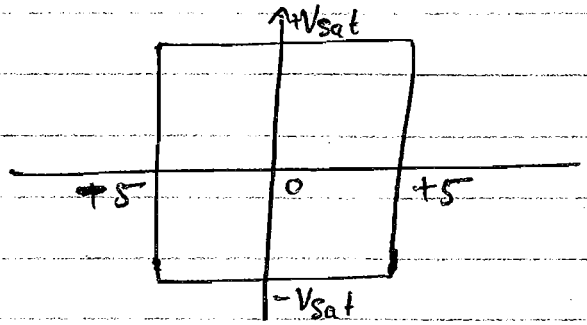
$$\boxed{V_2 = \frac{V_o}{3}}$$

$$V_{UT} = V_2 = +\frac{V_{sat}}{3} = \frac{+15}{3} = +5V$$

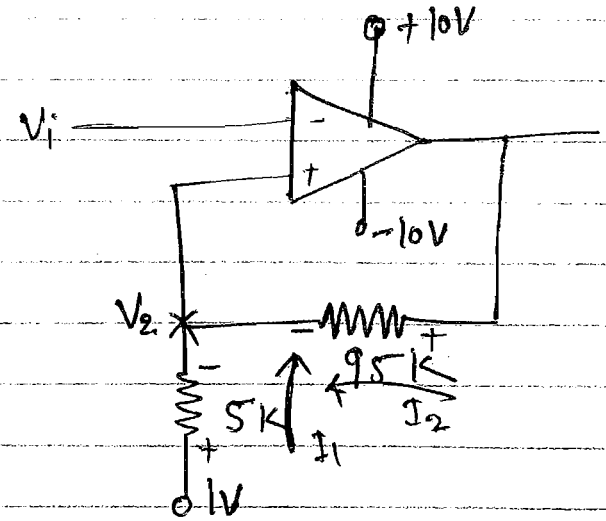
$$V_{LT} = V_2 = -\frac{V_{sat}}{3} = \frac{-15}{3} = -5V$$

$$V_H = 5 - (-5) = 10V$$

$$\boxed{V_H = 10V}$$



P.g-20
Q.1



Soln

$$I_1 + I_2 = 0$$

$$\frac{1 - V_2}{5K} + \frac{V_0 - V_2}{95K} = 0$$

$$\frac{1}{5} + \frac{V_0}{95} = \frac{V_2}{5K} + \frac{V_2}{95K}$$

$$1 - V_2 + \frac{V_0}{19} - \frac{V_2}{19} = 0$$

$$\frac{20V_2}{19} = \frac{V_0 + 19}{19}$$

$$V_2 = \frac{V_o - 19}{20}$$

$$V_{UT} = \frac{10 + 19}{20} = \frac{29}{20}$$

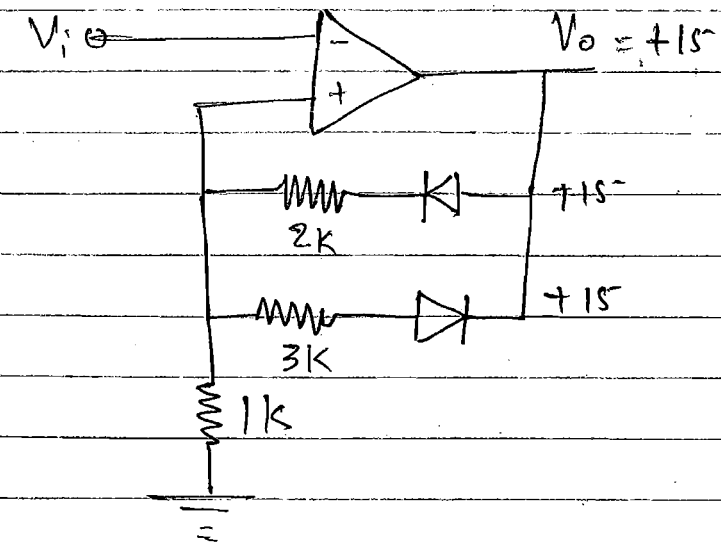
$$V_{LT} = \frac{-10 + 19}{20} = \frac{9}{20}$$

$$V_H = V_{UT} - V_{LT} = \frac{29}{20} - \frac{9}{20}$$

$$= \frac{20}{20} = 1$$

$$\boxed{V_H = 1V}$$

Qus for the given circuit diagram calculate Hysterisis Voltage



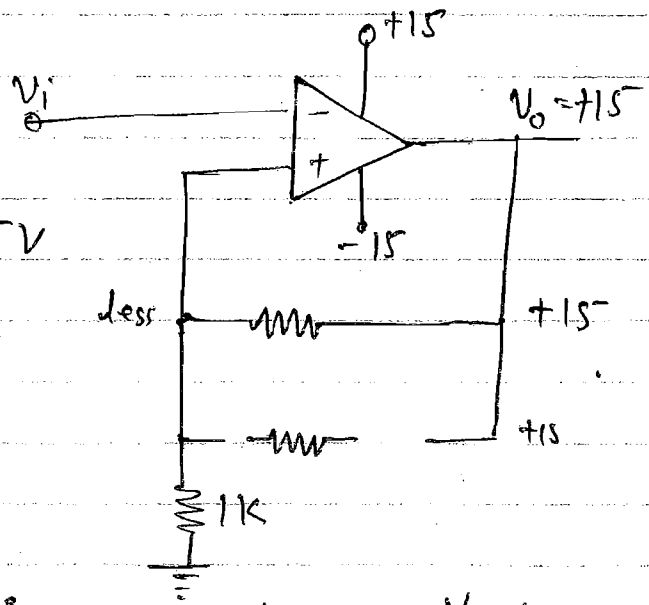
Sol^n

$$V_2 = \frac{V_o R_1}{R_1 + R_2}$$

$$\boxed{V_2 = \frac{V_o \, 1K}{1K + R_2}} \quad (1)$$

$$\therefore V_2 = \frac{V_0 \cdot R_1}{R_1 + R_2}$$

When $V_2 > V_{in}$ $\quad V_0 = +V_{sat} = +15$



$$V_2 = \frac{15}{3} = +5V$$

$$\boxed{V_2 = +5\ V}$$

When $V_2 < V_{in}$ $\quad V_0 = -V_{sat} = -15$

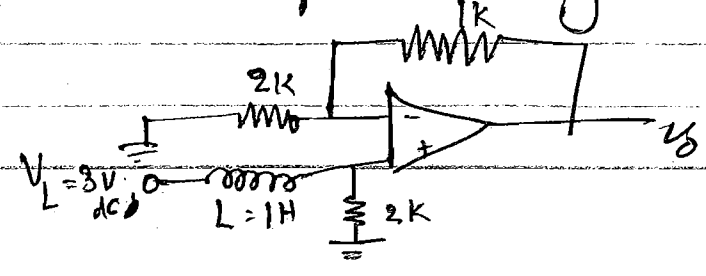
$$V_2 = V_{UT} = \frac{-15 \cdot R_1}{R_1 + R_2}$$

$$V_{UT} = -15\ \frac{1K}{1K + R_2}$$

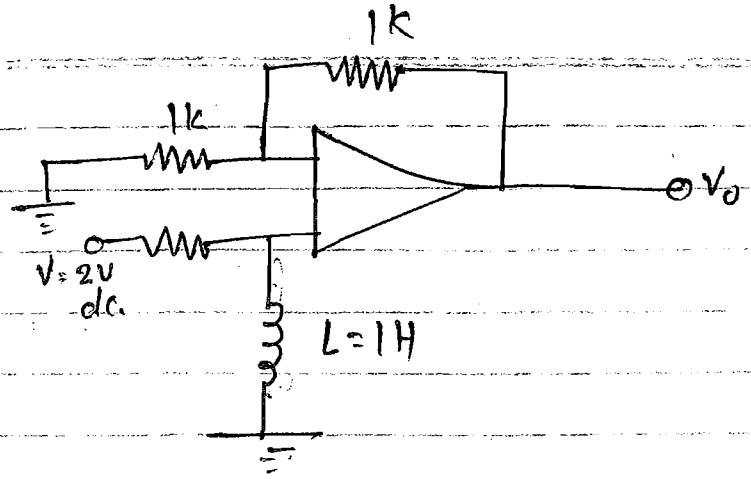
$$V_{LT} = \frac{-15K}{9K} = 3.75$$

$$\boxed{V_H = 0.75}$$

2. Calculate output voltage V_o = ?

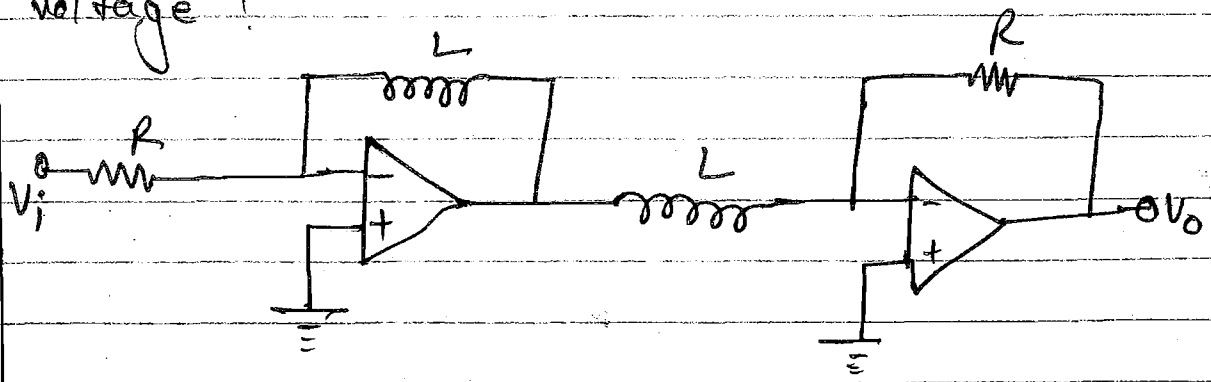


(ii)



Q.1/2 Calculate the current through each and every branch

Q.2 For the given circuit diagram determine the output voltage ?



* Characteristic Parameters of Op-Amp :-

(i) Open Loop voltage gain $A_{OL} = \infty$
(ii) Input resistance $R_i = \infty$
(iii) Output resistance $R_o = 0$
(iv) Slew Rate (SR) :-

$$SR = \frac{dV_o}{dt}$$

Rate of change of output voltage with respect to time is called as "Slew Rate".

$$SR = \left.\frac{dV_o}{dt}\right|_{max}$$ {ideally $V_o = \infty$}

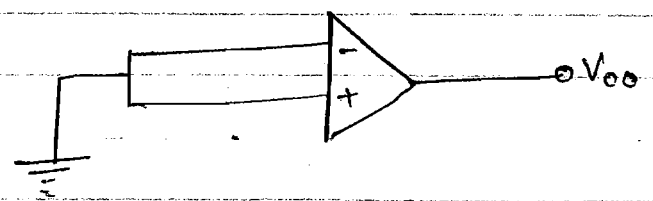
S.I. Unit -

Volt / sec

Standered Unit :-

Volt / μ.s

(v) Output Offset Voltage :- $\{V_{oo}\}$



Whenever both the inputs are grounded, some ~~output~~ voltage is available at

the output that is called Output offset voltage. Ideal value of Output offset voltage is zero.

vi) Input offset voltage :- $\{V_{io}\}$:-

To reduced the effect of output offset voltage the voltage used at the input is called as input offset voltage.

vii) CMRR (Common Mode Rejection Ratio) :-

$$CMRR = \frac{A_d}{A_c}$$

A_d = differential gain
A_c = common gain or Noise gain.

Ideal value of CMRR = ∞

Noise is send for -ve or +ve terminal of op-Amp.

It is used to reject the effect of noise.

It is defined as noise rejecting ability of the system.

OR

The ratio of the differential gain A_d and A_c common mode gain.

$$(CMRR)_{db} = 20 \log \frac{A_d}{A_c}$$

Ques A voltage follower circuit having input voltage $V_{in} = V_m \sin \omega t$. Calculate the maximum frequency At which slew rate becomes maximum?

Soln:

$$\because \quad S.R = \left.\frac{dV_o}{dt}\right|_{max}$$

$$V_i = V_o = V_m \sin \omega t$$

$$= \left.\frac{d\, V_m \sin \omega t}{dt}\right|_{max}$$

$$S.R. = \left. V_m \cos \omega t \cdot \omega \right|_{max}$$

At maximum $\cos \omega t = 1$

$$S.R. = V_{in}\, \omega$$

$$\boxed{\omega_{max} = \frac{S.R}{V_m}} \qquad \left\{ \because \left. SR \right|_{max} = \omega_{max} \right.$$

$$\boxed{\omega_{max} \quad \frac{S.R}{2\pi V_m} \text{ Hz}}$$

{ P-N Junction Theory }

* Crystal Structure of p-type and n-type semi-conductor :-

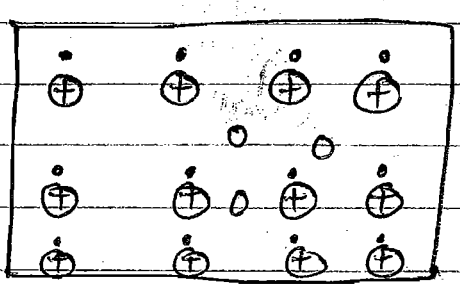
Intrinsic pure ($\sigma \downarrow\downarrow$)

to increase σ doping performed

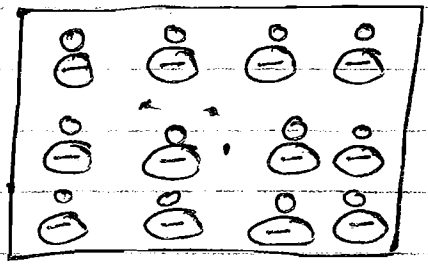
n-type
intrinsic + pentavalent Impurity
5 + 4
8 + 1
Negative type Semiconducter

p-type
intrinsic + trivalent
4 + 3
7 + −
Positive type Semiconducter.

N- type Semiconductor :-

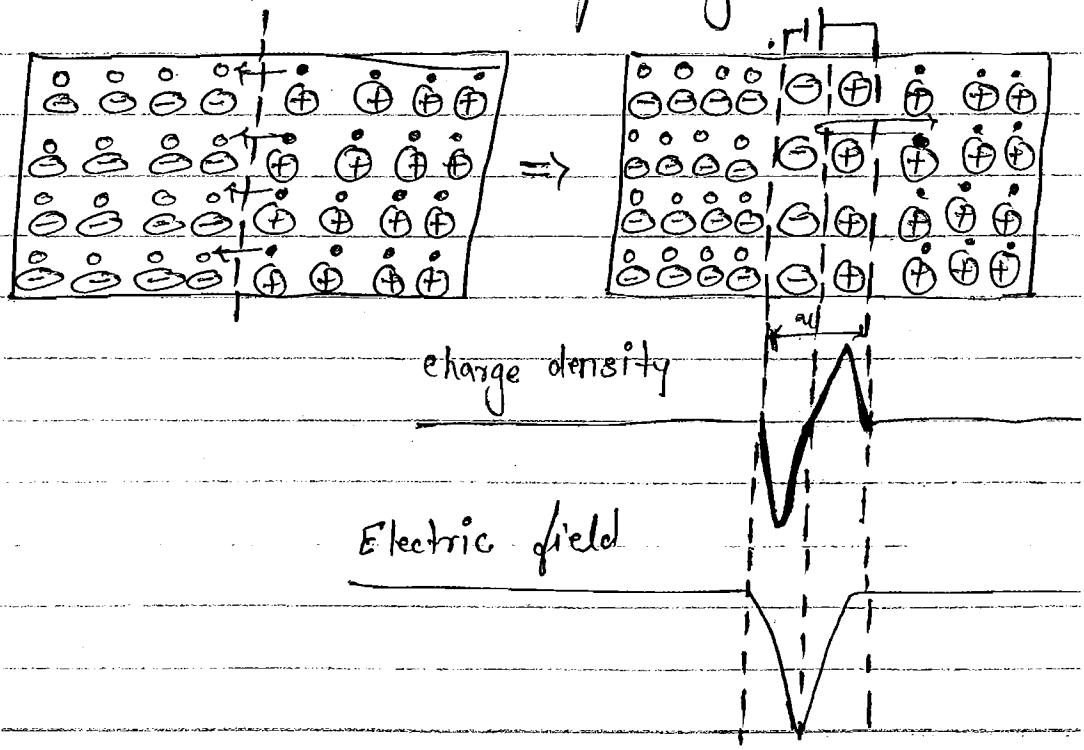


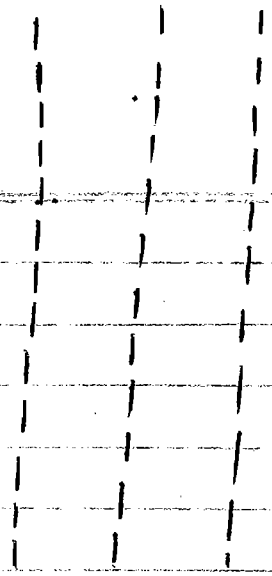
P-type semiconductor :-



Whenever a propercovalent bonding take place between a p-type and n-type semiconducter the resultant crystal is called as p-n junction diode.

"In an intrisic semiconductor from one side p-type substance and another side n-type substance is diffuse the point at which they will meet will form a junction is called as p-n junction."





Once a p-n junction is formed initial diffusion is take place from one region to another region. After certain ammount of diffusion a potential is created which opposes the further flow of charge carreer. hence called as barrier potential, or contact potential or build in potential seprated by (V_0).

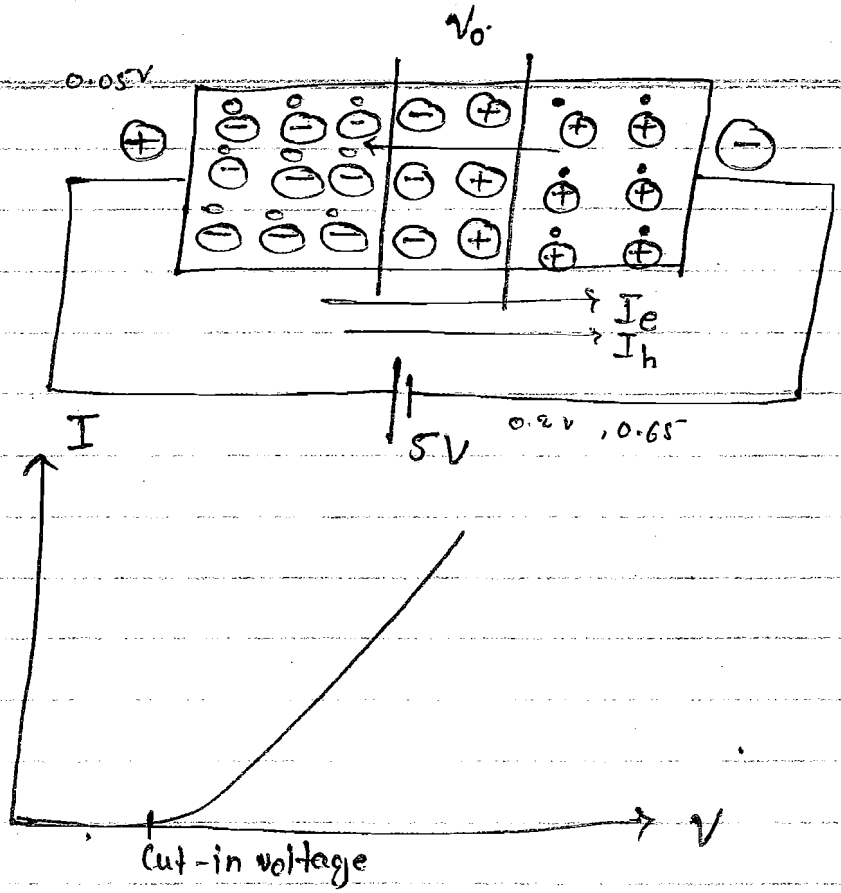
The region in which potential barrier created there is no free charge carriers hence called as depletion region. The value of contact potential can never be measured by ordinary voltmeter.

* Baising :-

For the practical application of diode certain voltages are applied at both end is called as "baising."

Forward Baising :-

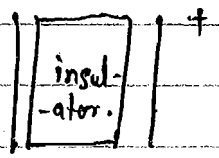
Under forward bais condition the width of the depletion region decreases as applied voltage increases.



Under forward bais condition as the forward voltage increases the current across the diode increasee exponentially.

The direction of curren under forward condition will be along the p to n type.

The minimum voltage after which the current increases to the large ammount is calleed as cut in voltage or threshold voltage.



Under forward bais condition a capacitor is exist called as diffusion capacitor.

Capacitance approx to negligible becouse depliton layer is very thin.

* DC Resistance & the Resistance under forward Bais Condition :-

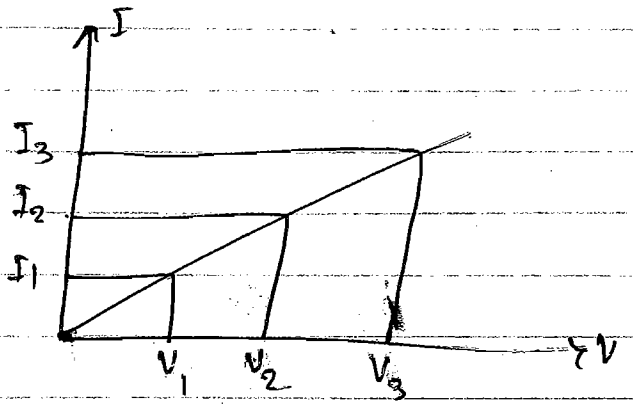
For linear characteristic both $\frac{V}{I}$ & $\frac{dv}{dI}$ is same.

$V \propto I$

$V = RI$

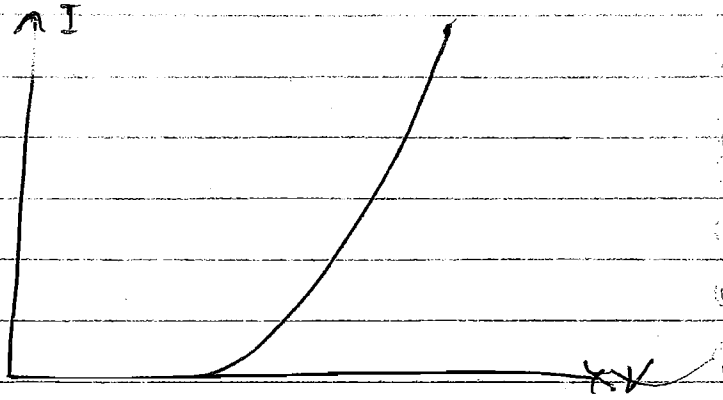
$\frac{V}{I} = R$

$\frac{d(V_2 - V_1)}{d(I_2 - I_1)} = \frac{dv}{dI} = R$



In straight line graph.

> This selection gives value as $\frac{V}{I}$

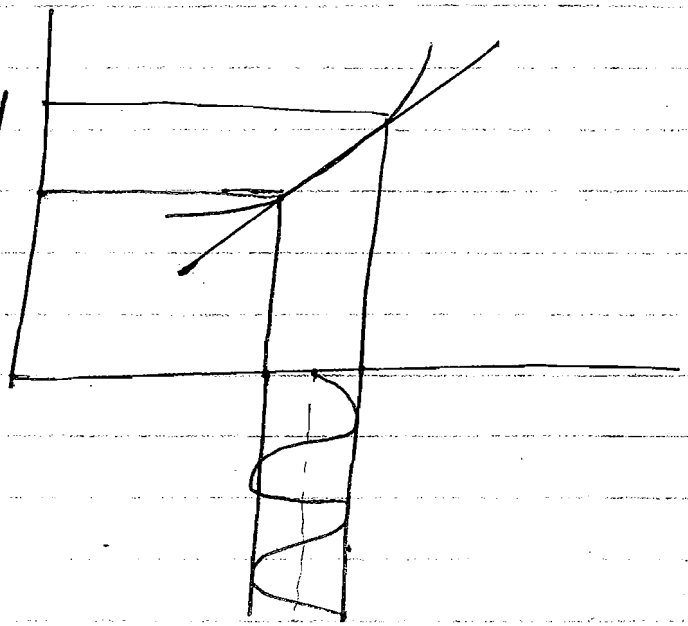


⇒ for any circuit at a fixed voltage the circuit is operating at a fixed current that voltage & current will give the operating point of circuit.

dc - means point analysis.

AC :- When our curve is non linear -

The A.C. analysis define about neighbourd point.



AC Resistance :-

$$I = I_0 e^{V/\eta V_T}$$

OR

$$I = I_0\left[e^{V/\eta V_T} - 1\right] = I_0 e^{V/\eta V_T} - I_0$$

(I_0 very small so it is neglected.)

So $$I = I_0 e^{V/\eta V_T}$$

η = Recombination factor.

If η (increase ↑) → width of deplition layer also increases.

$$R_{ac} = \frac{dV}{dI} = \frac{1}{dI/dV}$$

$$\frac{I_2 - I_1}{V_2 - V_1} = \text{slope} \Downarrow \frac{dI}{dV}$$

$$R_{ac} = \frac{1}{\text{slope}}$$

$$R_{ac} = \frac{1}{\frac{d\left(I_0 e^{-V/\eta V_T}\right)}{dV}}$$

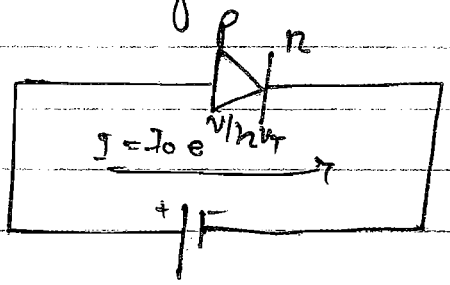
$$\frac{d}{dv} I_o e^{v/(\eta V_T)} = \frac{I_o e^{v/\eta V_T}}{\eta V_T}$$

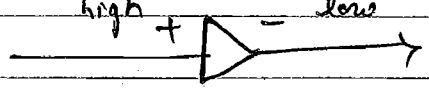
$$\therefore \quad R_{ac} = \frac{\eta V_T}{I_o e^{v/\eta V_T}}$$

$$R_{ac} = \frac{\eta V_T}{I}$$

I = forward Current
V_T = Thermal voltage.
η = Recombination factor

* Equivalent Symbol of representation of pn-junction diode under forward bais Condition :-





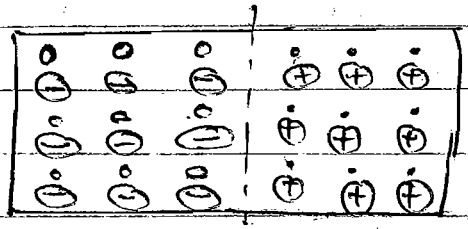
$\equiv$ (wire)

I = max
V = cut in

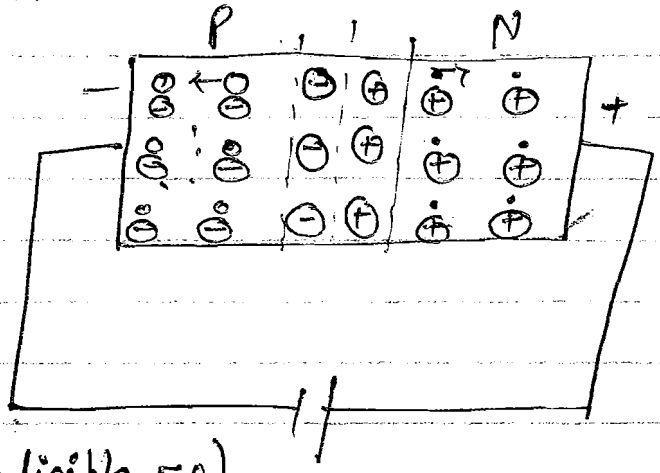
$=$

$V_\gamma = 0.7$ V Si
$= 0.3$ Ge
} imp

* Reverse Baising :-

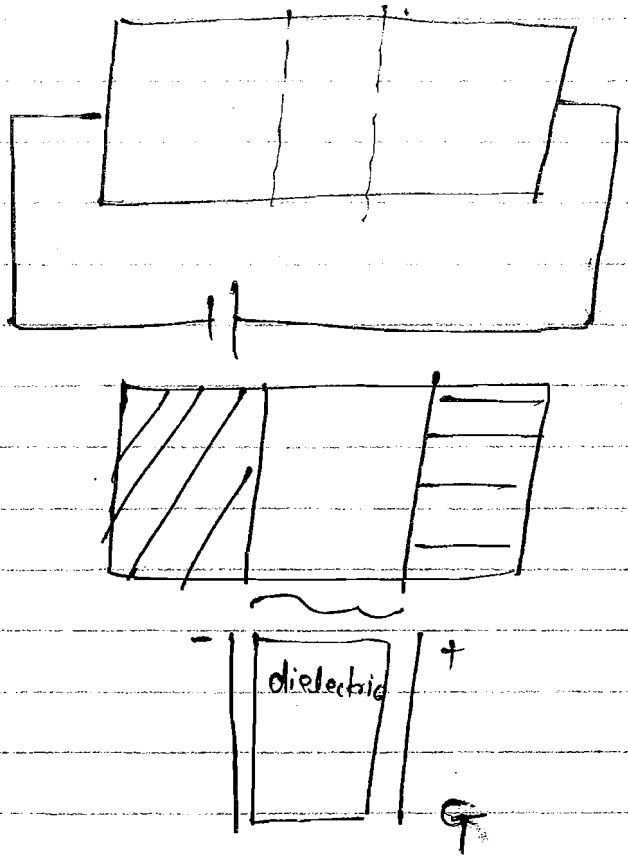


⇒ Under reverse bais condition the width of depletion layer increases.

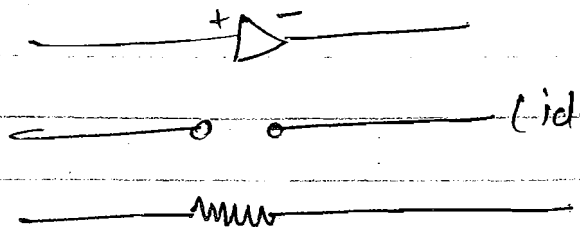


⇒ Under reverse bais condition minority carriers crosses the junction hence the current is becoz of minority carriers is very less (negligible ≈ 0)

⇒ Under reverse bais condition a capacitance exist called transition capacitance C_T.



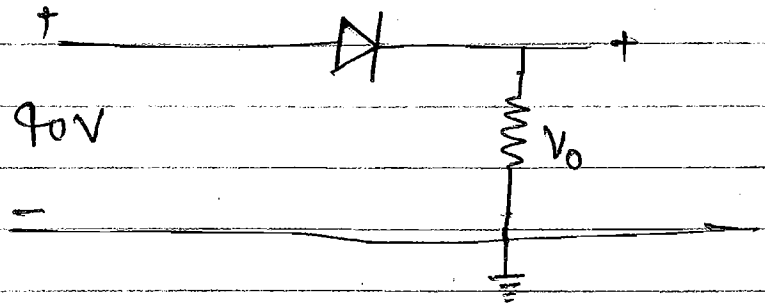
* Equivalent Representation of Reverse bais:-



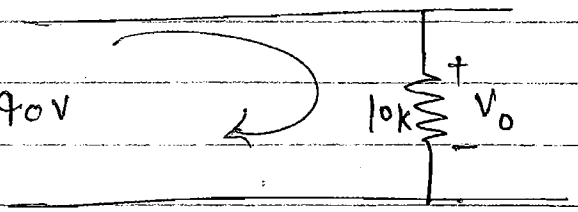
Dynamic — Ans.

* Ideal Case :-

for the given circuit diagram calculate current I and o/p voltage V_o and hence calculate dynamic resistance.



Equivalent symbol :-



$$-40 + V_o = 0$$

$$\boxed{V_o = 40\ V}$$

$$I = \frac{V}{R} = \frac{40}{10} = 4\ \text{Amp.}$$

OR

$$-40 + I\,10k = 0$$

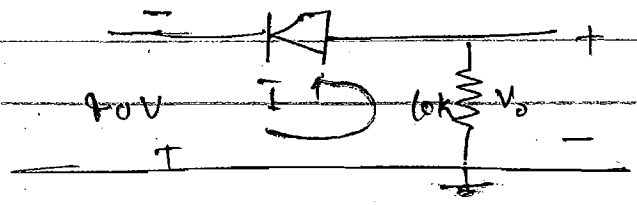
$$\boxed{I = \frac{40}{10}} = 4\ \text{m.A.}$$

Dynamic Resistance :-

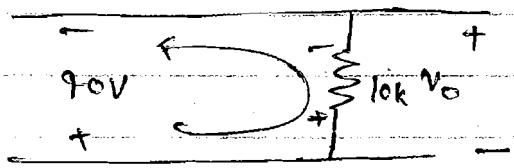
$$R_{ac} = \frac{\eta V_T}{I} = \frac{1 \times 26\ mV}{4\ mA}$$

$$\boxed{R_{ac} = 6.5\ \Omega}$$

Q. for the given circuit diagram determine o/p voltage and current across circuit.



Equivalent circuit :-



$-40 + V_o = 0$

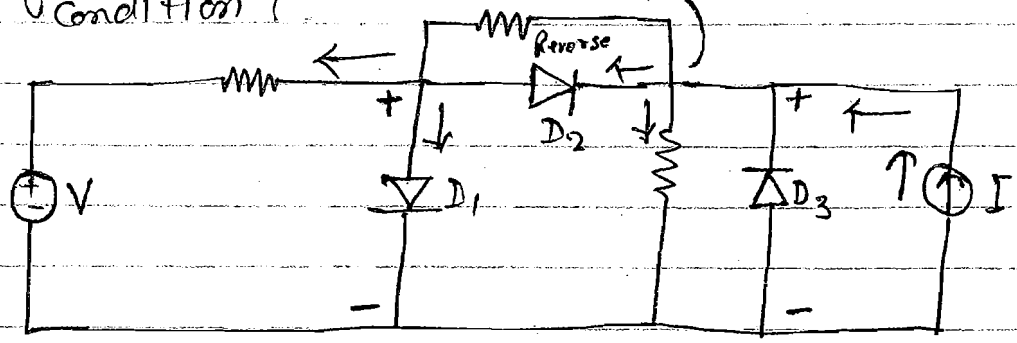
$\boxed{V_o = -40}$

Curren :- $-40 + I \times 10 = 0$

$I \cdot 10 = 40$

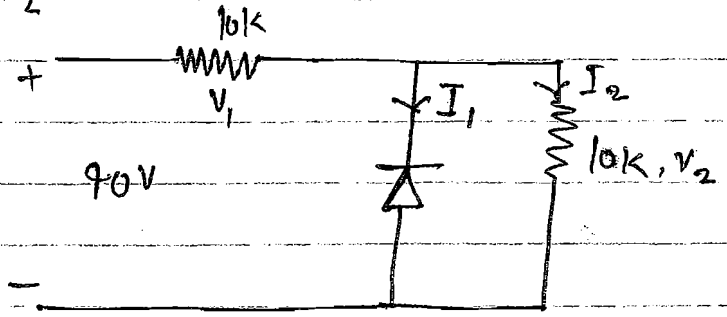
$\boxed{I = 4mA}$

Q. For the given circuit diagram identify which of the diodes are under forward bais condition?

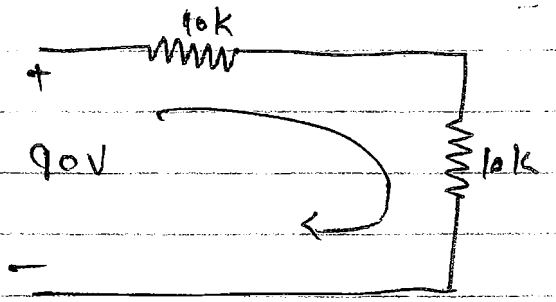


	D_1	D_2	D_3
(a)	on	off	off
(b)	on	on	off
(c)	off	on	off
(d)	off	on	on.

Q. For the given circuit diagram determine the current I_1 and I_2.



$I_1 = 0$ (Because of reverse bais)



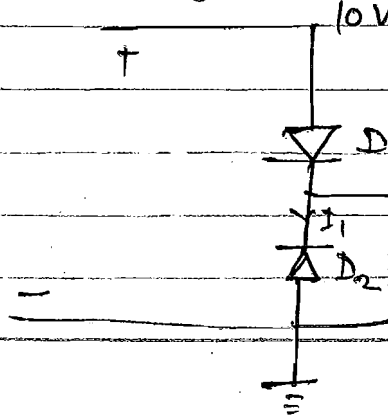
$$-90 + 20I_2 = 0$$

$$\boxed{I_2 = 2\text{mA}}$$

$$V_2 = \frac{90 \times 10}{20} = 20V$$

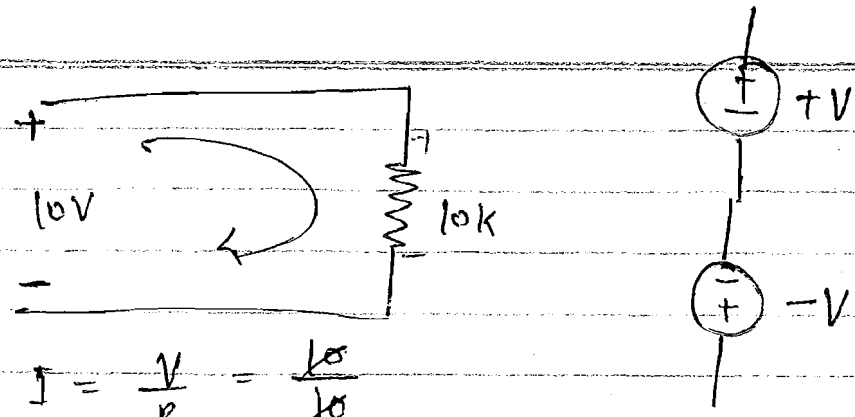
$$V_1 = \frac{90 \times 10}{20} = 20V$$

Q. For the given circuit diagram determine I_1 and I_2



∵ D_2 is Reverse

So $\boxed{I_1 = 0}$

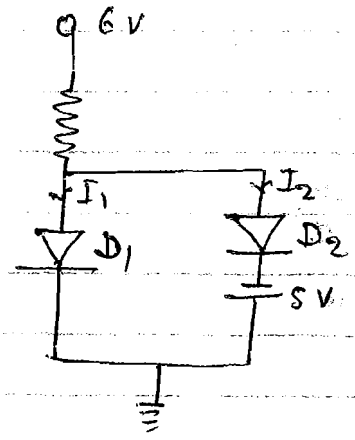


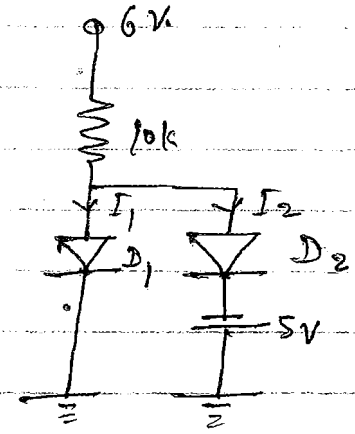
$$I = \frac{V}{R} = \frac{10}{10}$$

$$\boxed{I = 1\ mA}$$

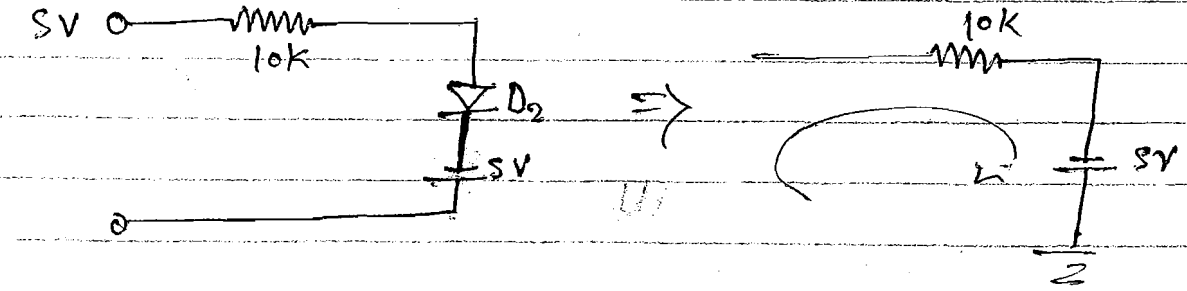
Ques For the given circuit diagram calculate I_1, I_2 ? Hence identify which of the diodes are under forward bais?

Sol^n





∵ D_1 is reverse bais So $I_1 = 0$

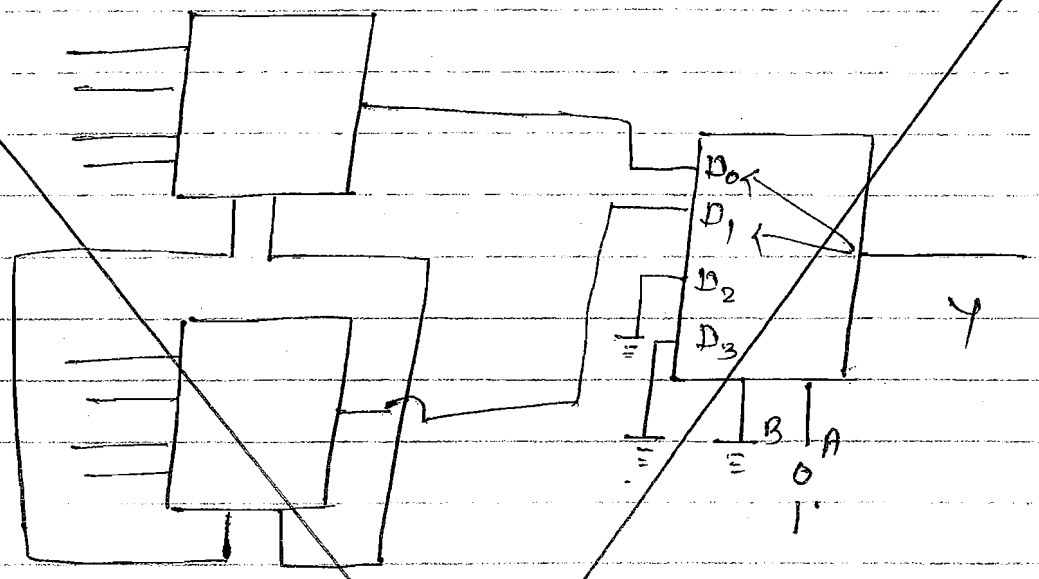


$$-5 + I \times 10 - 5 = 0$$

$$10I = 10$$

$$\boxed{I = 1\ mA}$$

8 x 1 ⟶ 4 x 1



$$\overline{\overline{XC}.\overline{AB}} = \overline{\overline{XC}} + \overline{\overline{AB}}$$

$$= XC + AB$$

$$= C(A\bar{B} + \bar{A}B) + AB$$

$$= A\bar{B}C + \bar{A}BC + AB$$

$$= A\bar{B}C + B(\bar{A}C + A)$$

$$= A\bar{B}C + (A+C)B$$

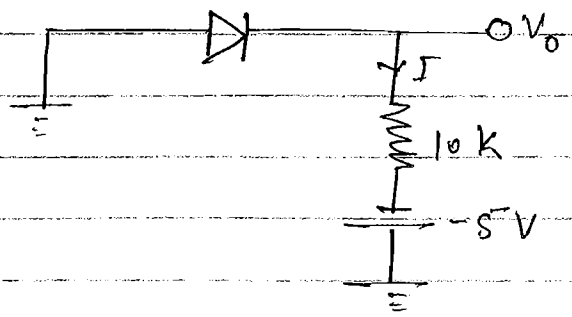
$$= A\bar{B}C + AB + BC$$

$$= A(B + \bar{B}C) + BC$$

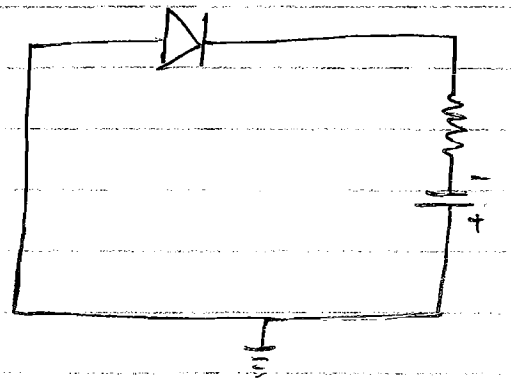
$$= A(B + C) + BC$$

$$= AB + AC + BC$$

Q. for the given circuit diagram calculate I and V_o.



soln



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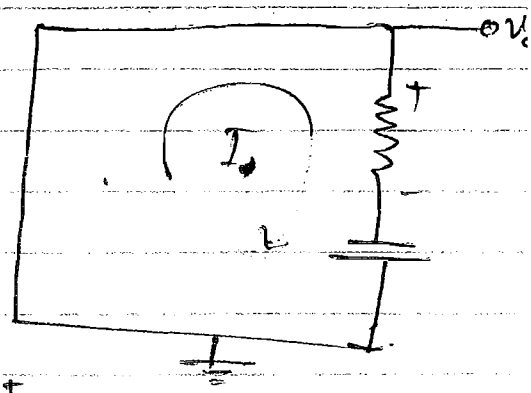
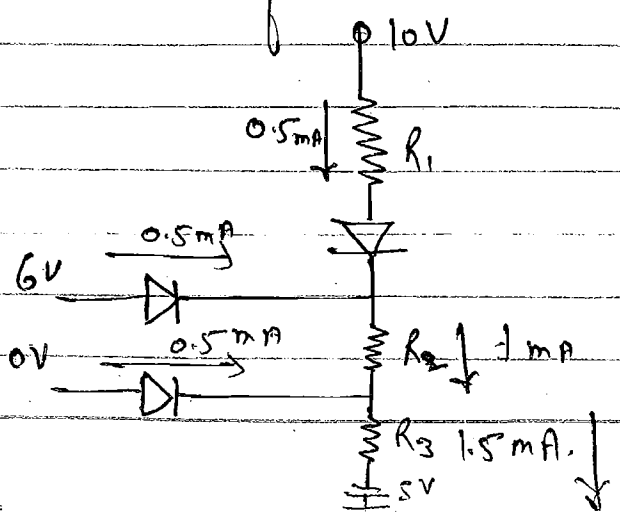


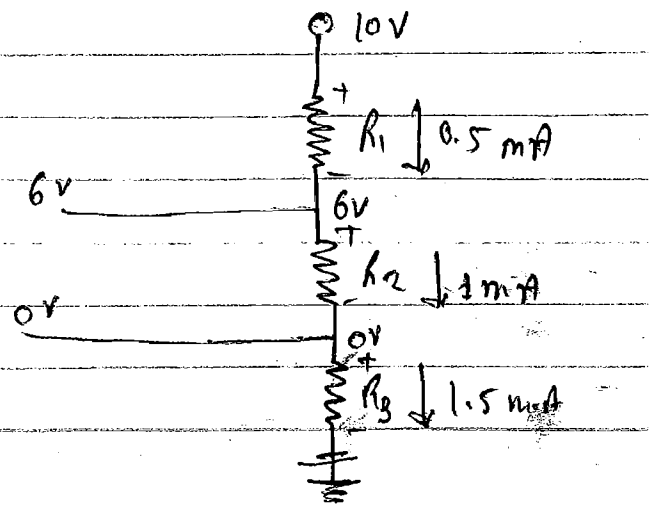
$10I - 5 = 0$

$I = 0.5\,mA$

$V_o = 0$ { becoz V_o is connected to ground }

Q. for the given circuit diagram assum all the diode are forward bcais, each diode having a current of 0.5 mA. Calculate the value of R_1, R_2, R_3.





$\because I = \frac{V_a - V_b}{R}$

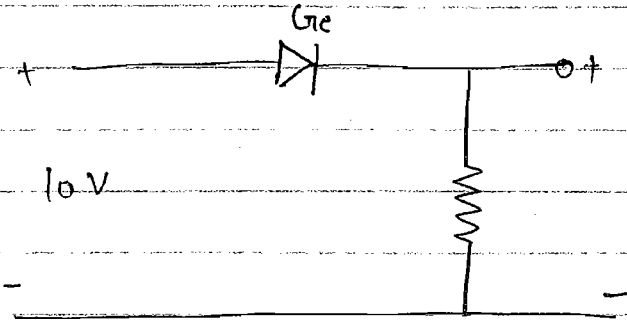
$\Rightarrow R = \frac{V_a - V_b}{I} = \frac{10 - 6}{0.5^-}$

$$R_1 = \frac{9}{0.5^-}$$

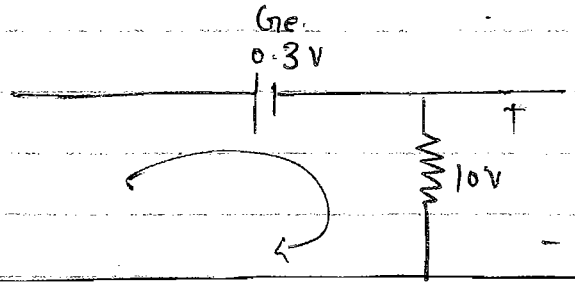
$R_2 =$

* Practical Diodes :-

Qu. For the given circuit diagram determine output voltage and current accross the circuit.



Soln



$\Rightarrow \quad -10 + 0.3 + V_0 = 0$

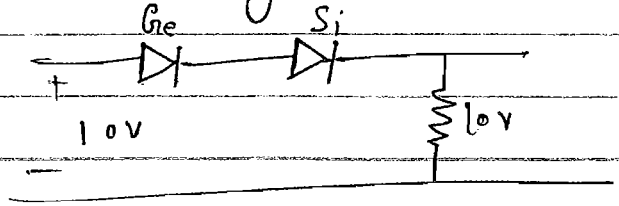
$$\boxed{V_0 = 9.7\,V}$$

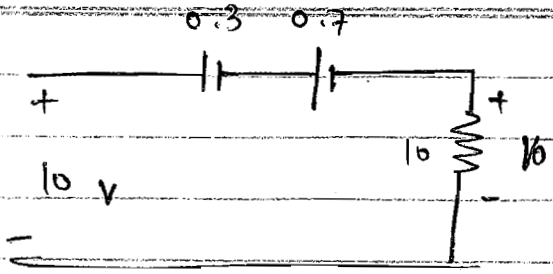
$\Rightarrow \quad -10 + 0.3 + I \times 10k = 0$

$\Rightarrow \quad I = \dfrac{9.7}{10k} = 0.77\,mA$

$\Rightarrow \quad \boxed{I = 0.77\,mA}$

Q Calculate output voltage and current -





$$-10 + 0.3 + 0.7 + V_0 = 0$$

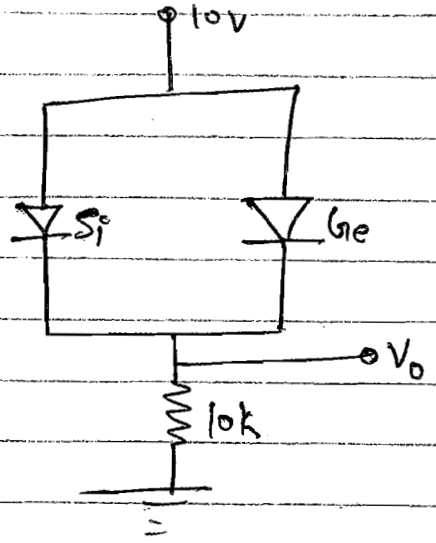
$$\boxed{V_0 = 9V}$$

$$-10 + 0.3 + 0.7 \times I \times 10 = 0$$

$$I = \frac{9}{10}$$

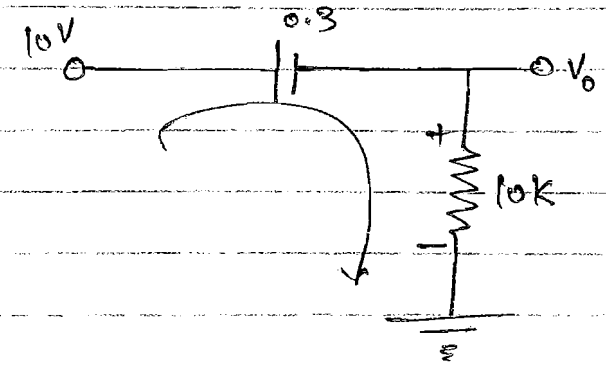
$$\boxed{I = 0.9\ mA}$$

Q. Calculate output voltage and current -



When two diodes are in parallel the diode which is having lesser cut in voltage will replace the diode of higher cut in voltage.

So equivalen circuit diagram



$$-10 + 0.3 + V_0 = 0$$

$$\boxed{V_0 = 9.7V}$$

$$-10 + 0.3 + 10I = 0$$

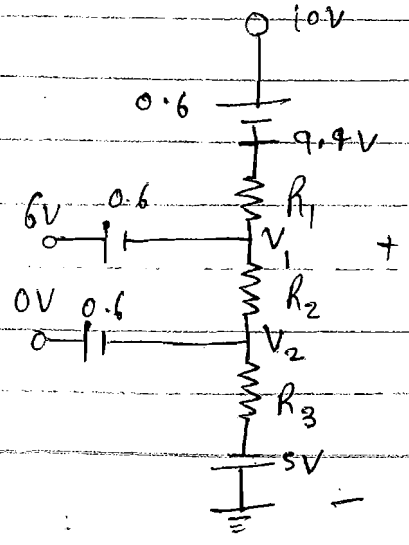
$$10I = 9.7$$

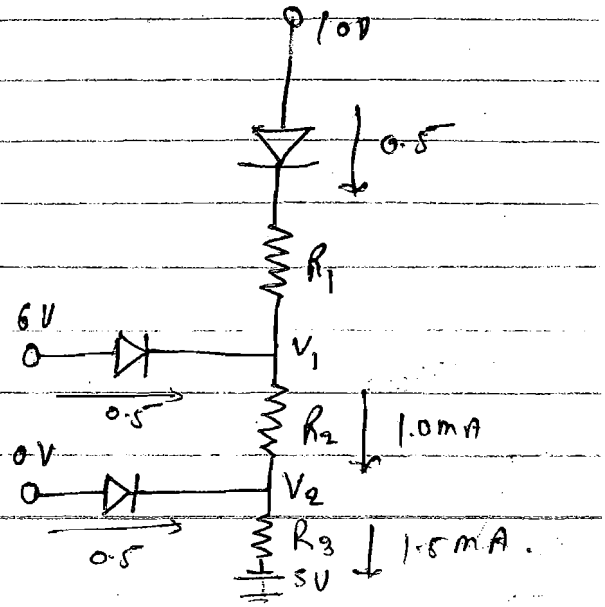
$$I = \frac{9.7}{10}$$

$$\boxed{I = 0.97\ mA}$$

Ques For the given circuit diagram calculate the value of R_1, R_2, R_3 assume each diode is having a voltage drop of 0.6V and current across each diode is 0.5mA.

Soln





$\Rightarrow -6 + 0.6 + V_1 = 0$

$$\boxed{V_1 = 5.4\,V}$$

$\Rightarrow 0 + 0.6 + V_2 = 0$

$$\boxed{V_2 = 0.6\,V}$$

$$\Rightarrow R_1 = \frac{9.9 - 5.9}{0.5\,mA} = \frac{9}{0.5}$$

$$\boxed{R_1 = 8k}$$

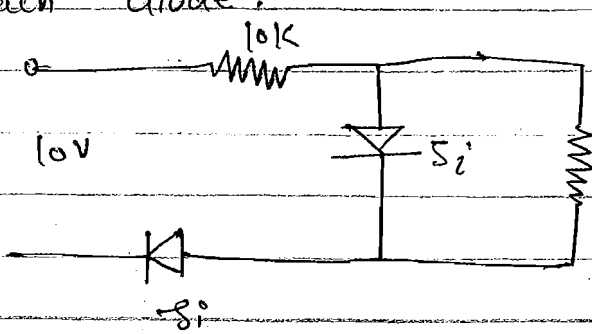
$$\Rightarrow R_2 = \frac{5.9 - (-0.6)}{1.mA} = \frac{6}{1}$$

$$\boxed{R_2 = 6k}$$

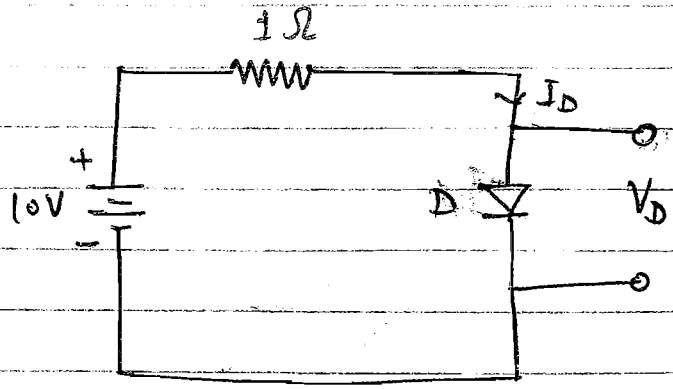
$$\Rightarrow R_3 = \frac{-0.6 - (-5)}{1.5} = \frac{4.9}{1.5}$$

$$\boxed{R_3 = 2.76k}$$

Q. For the given circuit diagram calculate current across each diode.



2.15



$$I_D = \begin{cases} V_D^2 + 2V_D & \text{for } V_D > 0 \\ 0 & \text{for } V_D \leq 0 \end{cases}$$

$$-10 + I_D \cdot 1 + V_D = 0$$

$$-10 + V_D^2 + 2V_D + V_D = 0$$

$$V_D^2 + 3V_D - 10 = 0$$

$$x^2 + 3x - 10$$

$$x = \frac{-3 \pm \sqrt{9 - 4 \times 1 \times 10}}{2 \times 1} = 5, -2$$

$$\boxed{V_D = 5\ V}$$

* Wave Shaping Circuits :-

Wave shaping circuits are classified as -

1 Clippers
2
3

1. Clipper :-

These are used to cut the certain portion of waveform. Hence called as slicers or chopper or clipper.

If positive waveform is clipped so called as positive clipper. If negative portion is clipped then it is called negative clipper. If both operation is performed then it is called as double clipper.

The basic circuit elemets are register, diode.

2. Clampers :-

These are used to shift the waveform either towards positive or negative.

If shift is towards +ve side called as positive clamper, otherwise negative clampers.

⇒ Basic circuit elements are capacitor, diode. In the clamper circuit addition of dc takes place hence, shift occurs.

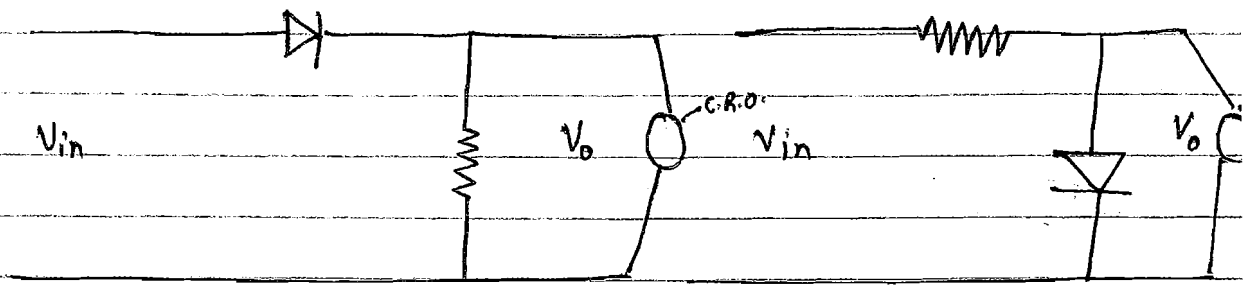
3 Rectifiers :-

Rectifiers are used to convert A.C. signal into pulse like d.c. or pulsating d.c.

1. Clippers :-

Clippers are classified as ~~series~~

1 Series Clippers
2 Shunt Clippers.



Series Clipper
(Diode and o/p in series)

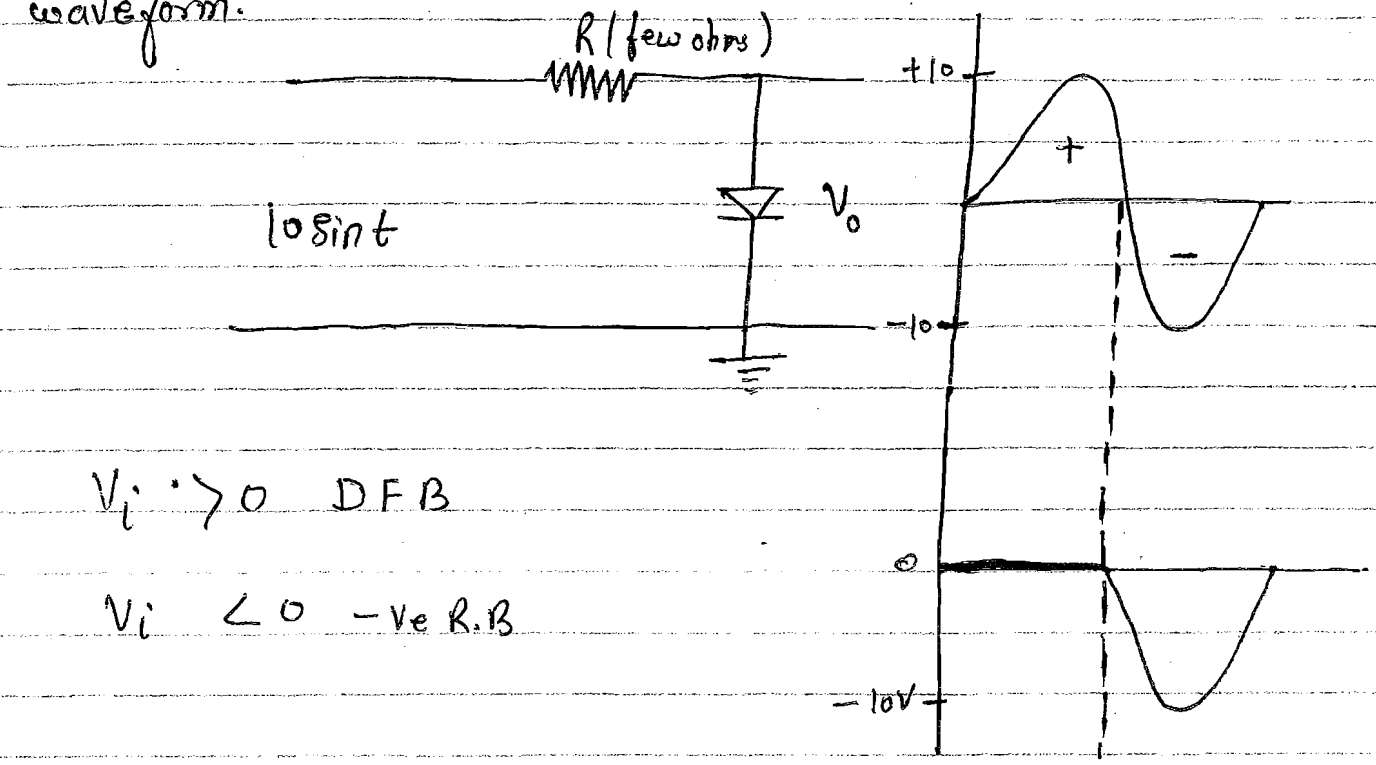
Shunt Clipper
(Diode and o/p in parall

If o/p is taken in series of the diode then it is called as series

If the o/p is taken in parallel of the diode then it is called as Shunt.

Shunt clipper is more preffered over series clipper becoz chances of diamage of diode is very less.

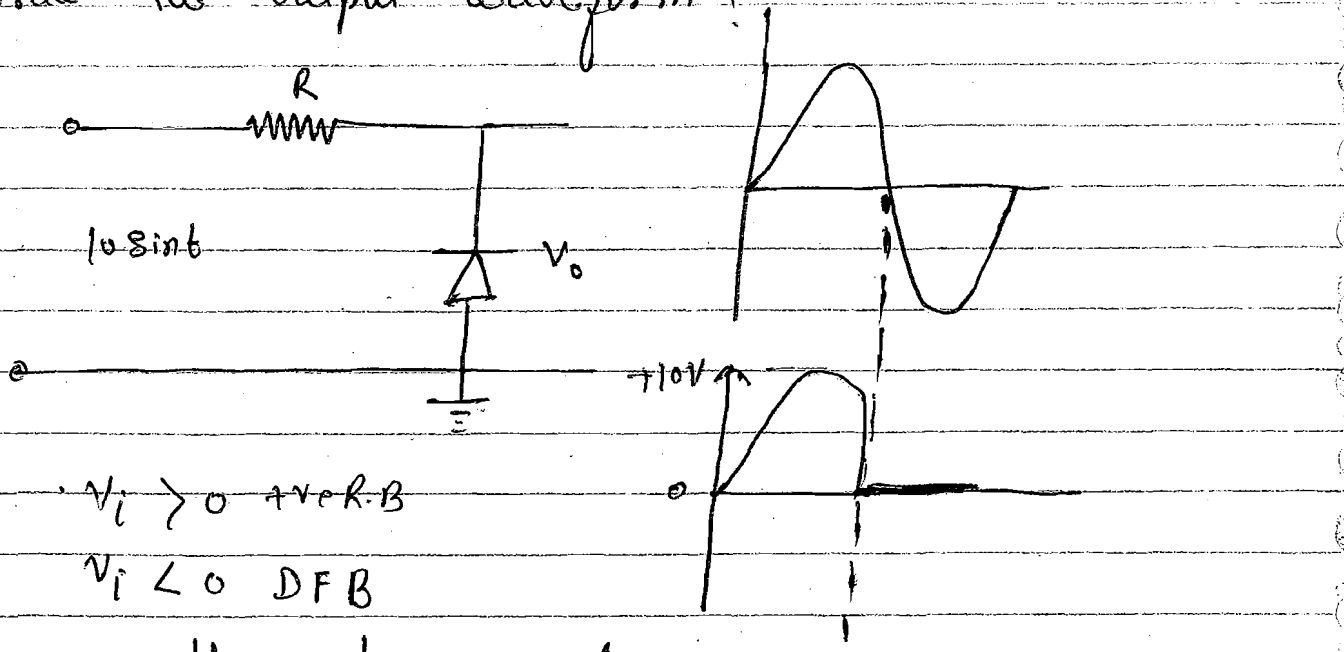
Qus for the given circuit diagram draw the output waveform.



$V_i > 0$ DFB

$V_i < 0$ -Ve R.B

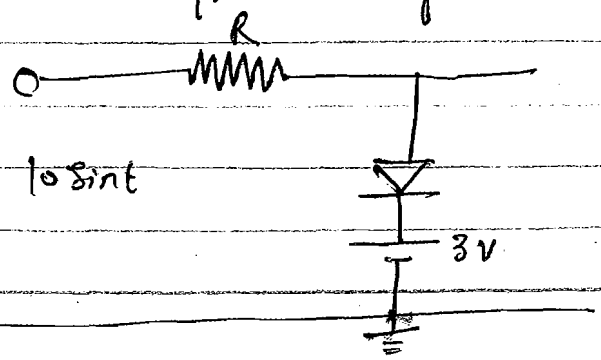
Qus Draw the output waveform ?



$V_i > 0$ +Ve R.B

$V_i < 0$ DFB

Q. Draw the o/p waveform.

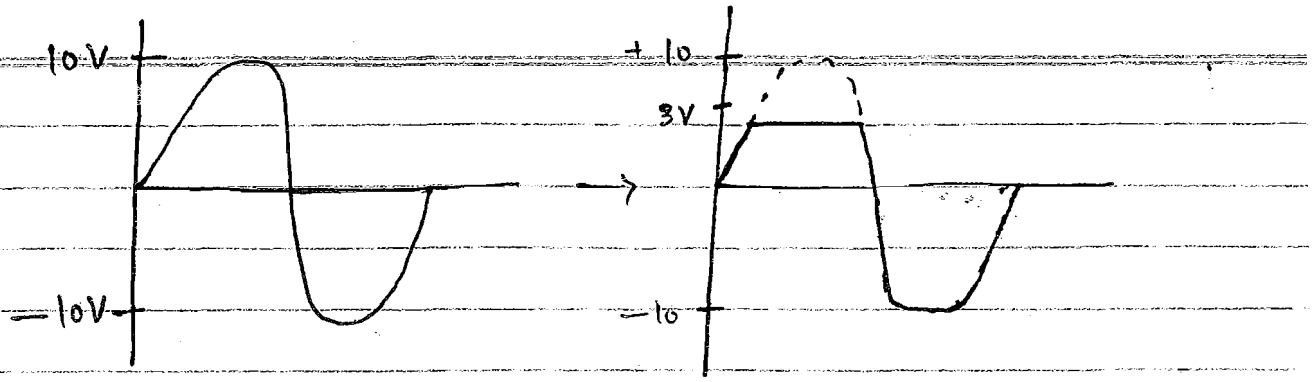


DFB

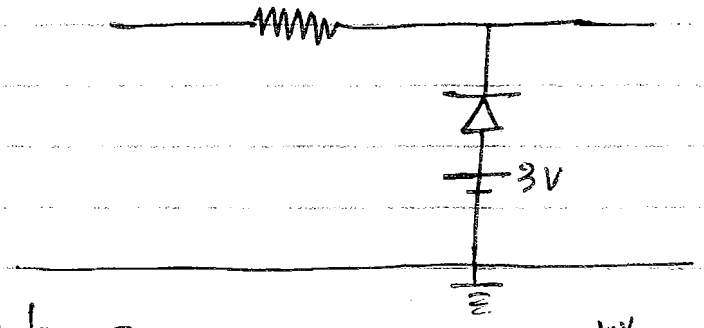
$V_i > 3$ (3.1 to 10)

$V_i < 3$ (2.9 to -10)

R.B

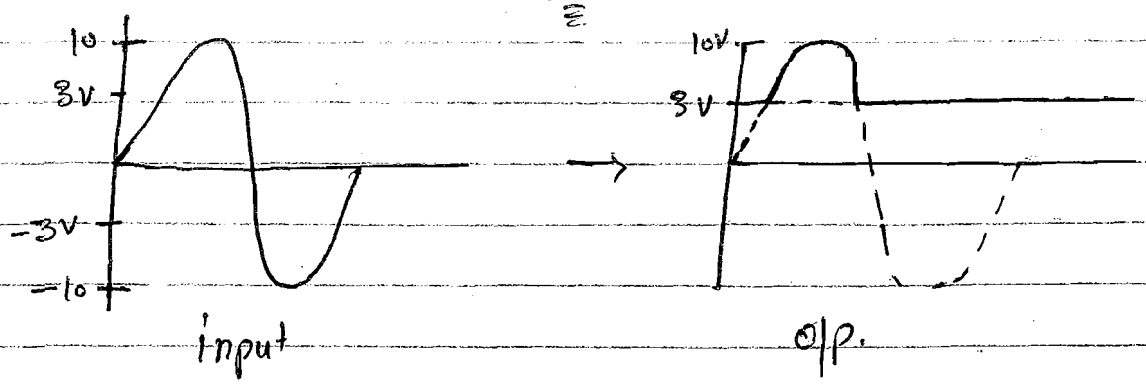


Qm Draw the output waveform.

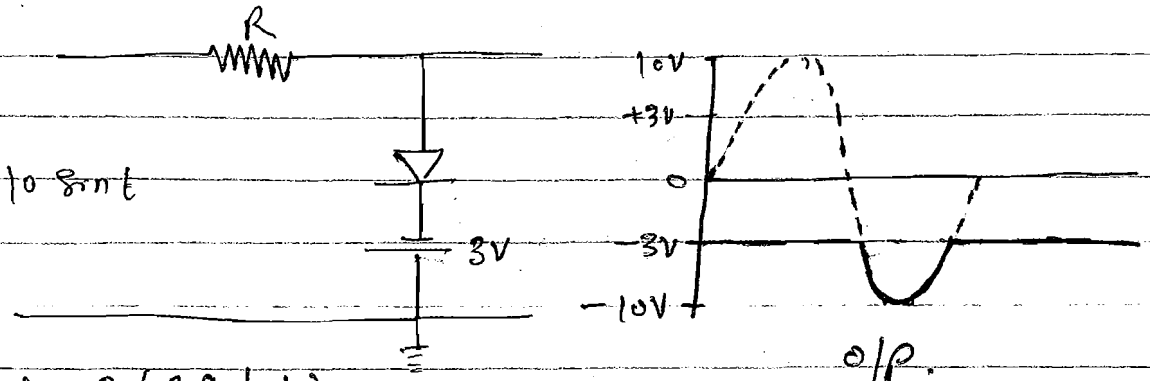


$V_i > 3$ (3.1 to 10) D.R.B

$V_i < 3$ (2.9 to -10) D F B



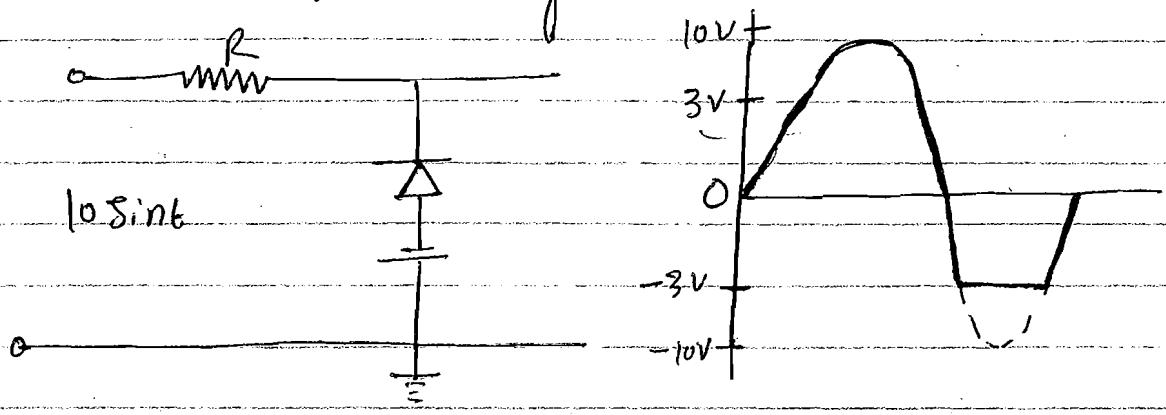
Q. Draw the o/p waveform.



$V_i > -3$ (2.9 to 10) FB

$V_i < -3$ (3.1 to 10) R.B

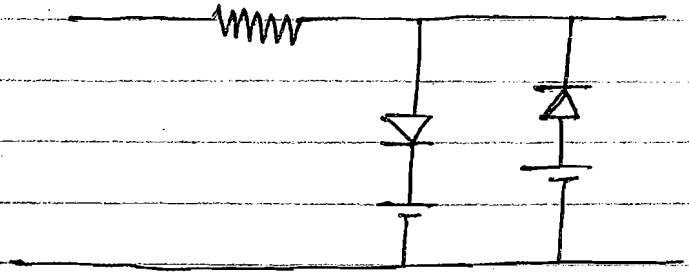
Q. Draw the output waveform.



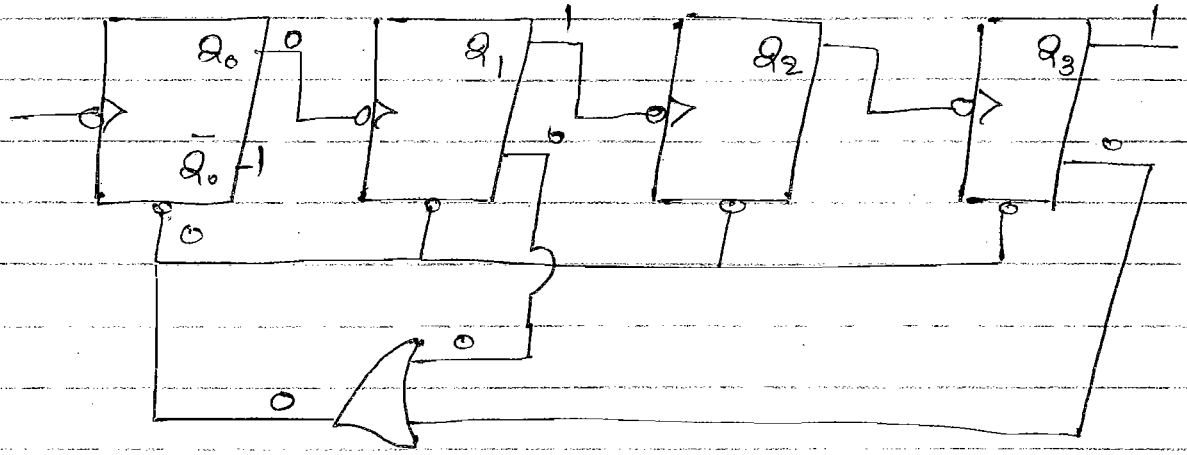
$V_i > -3$ (-2.9 to 10)

$V_i < -3$ (3.1 to 10)

Q. Draw the output waveform.

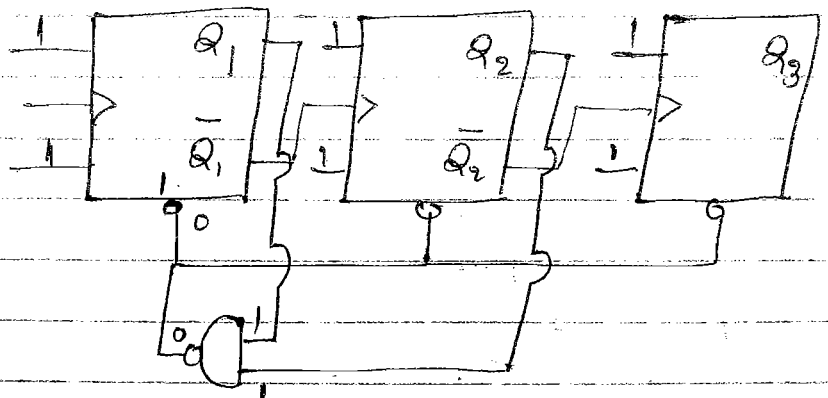


Q. For the given circuit — Up Counter



Mod – 10 Ans

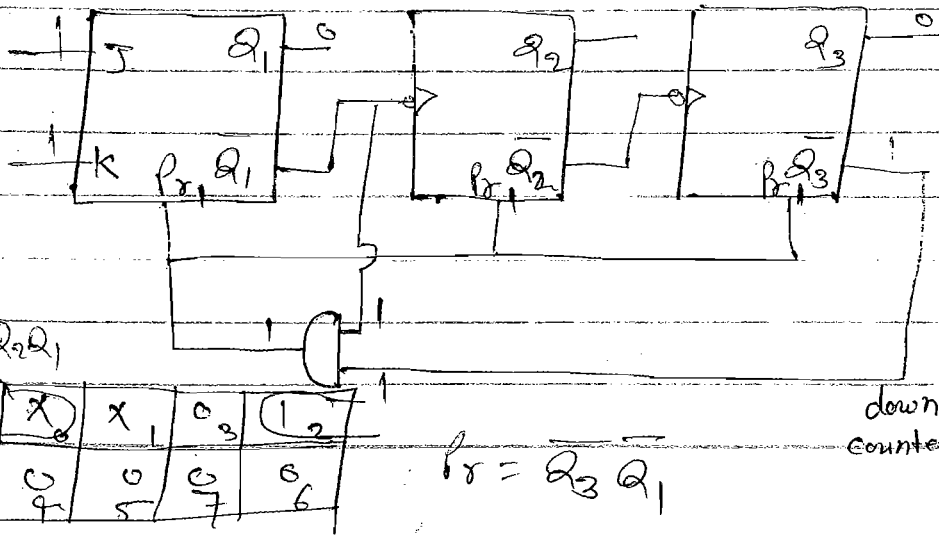
Ques For the given circuit diagram identify the Mod?



Q_3	Q_2	Q_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

This is up counter
Mod-3 up counter.

Q. Design a Mod-5 down counter?



Q_3	Q_2	Q_1	Pr
0	0	0	X
0	0	1	X
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	

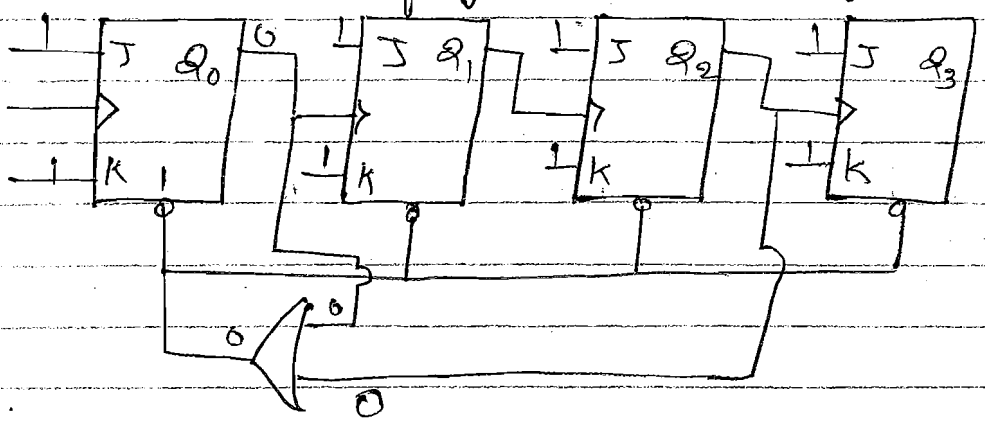
down counter

Q_2Q_1 / Q_3

x_0	x_1	0_3	1_2
0 4	0 5	0 7	0 6

$Pr = \bar{Q}_3 Q_1$

Ques Identify the Mod of given circuit diagram?



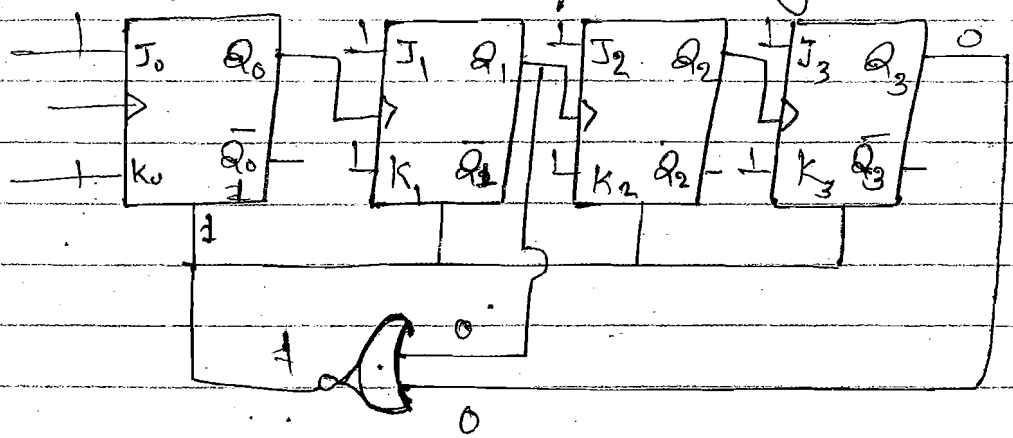
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Down Counter

This is down Counter

Ans :- Mod 5 down counter

Ques Identify the Mod of the given circuit diagram?



Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	1

down Counter

This is down counter

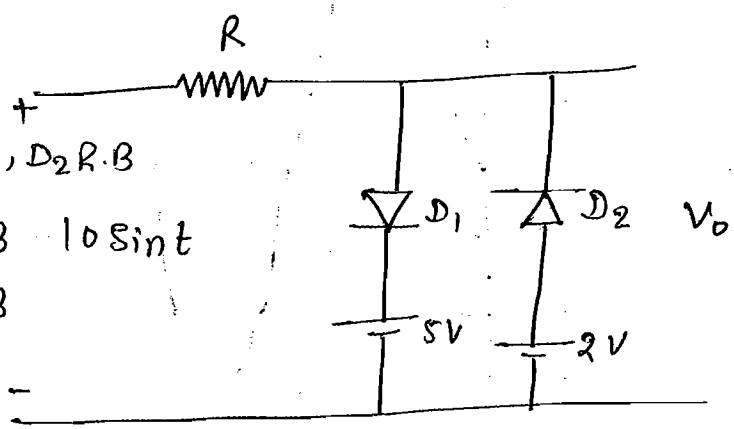
Ans :- Mod-10 down Counter.

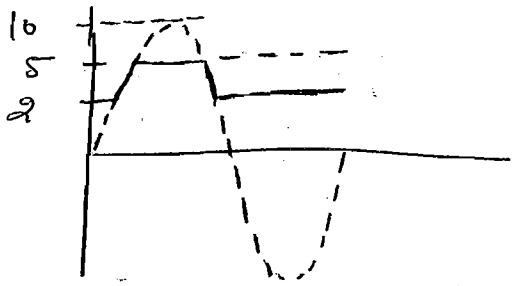
$V_i > 5$ (5.1 to 10) D_1 FB, D_2 R.B

$V_i < 2$ (1.9 to −10) D_1 RB 10 Sin t

D_2 FB

$2 < V_i < 5$ =





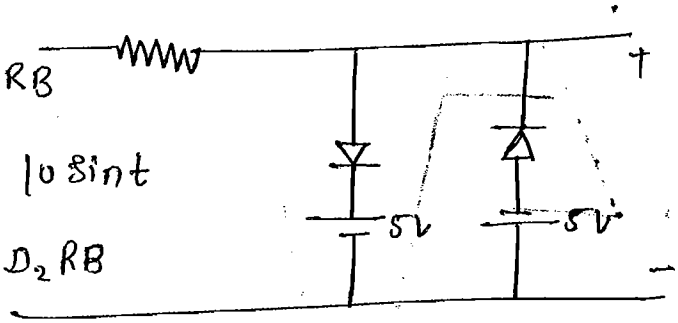
o/p.

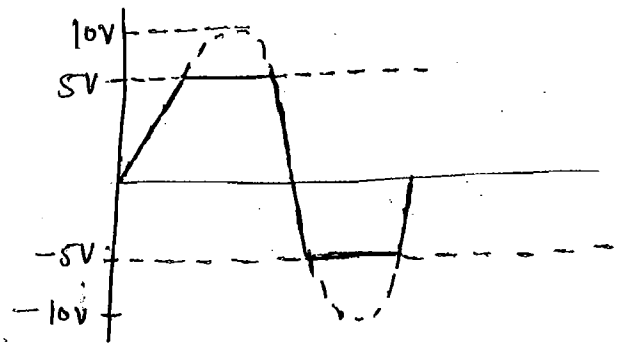
Q. For the given circuit diagram draw the o/p.

$V_i > 5^- \rightarrow D_1$ FB, D_2 RB

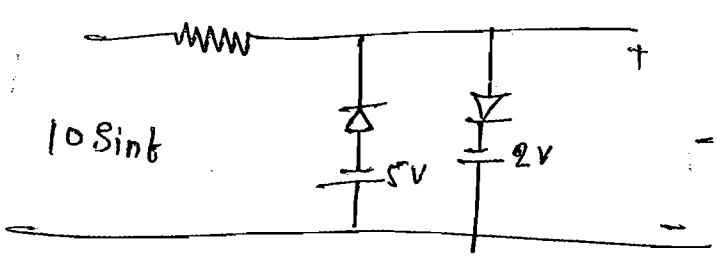
$V_i > -5^- \rightarrow D_1$ RB, D_2 FB 10 Sin t

$-5 < V_i < +5^- \rightarrow D_1$ RB, D_2 RB





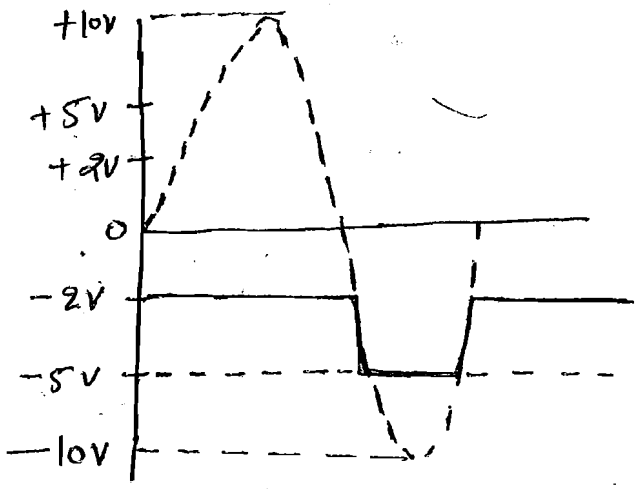
Q. Draw the o/p waveform ?



$V_i > 5 \rightarrow D_1$ FB, D_2 R

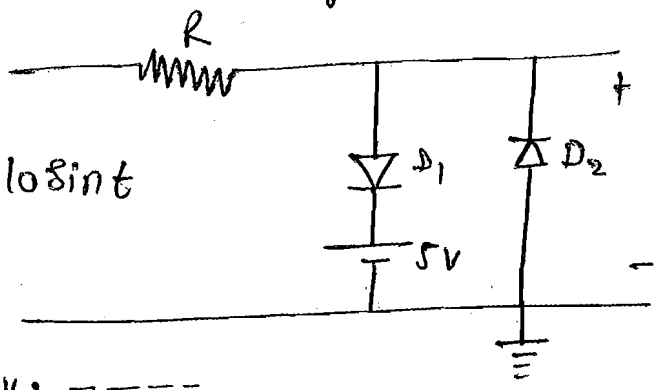
$V_i < -2 \rightarrow D_1$ RB, D_2 FB

$-2 < V_i < 5 \rightarrow D_1$ & D_2 R



o/p

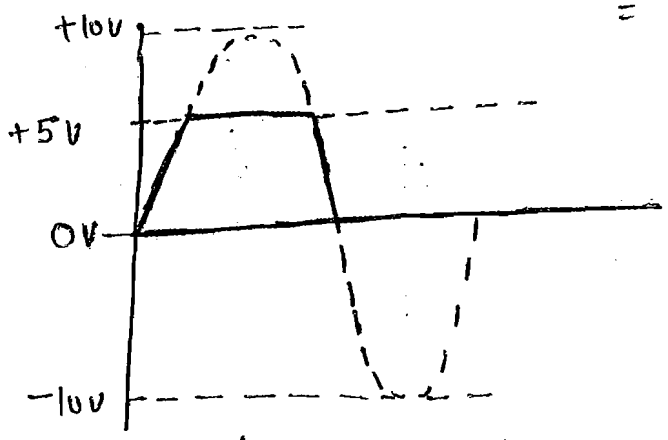
Q. Draw the output waveform ?



$V_i > 5 \rightarrow D_1$ FB, D_2 RB

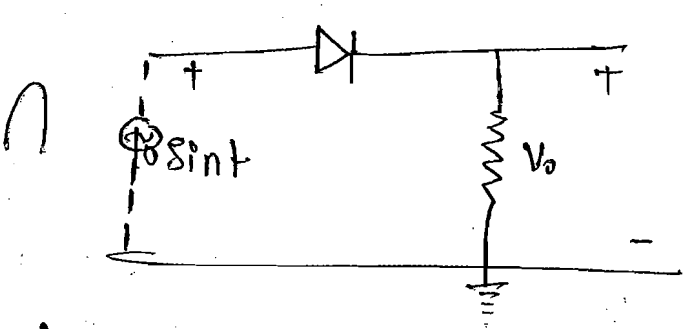
$V_i < 0 \rightarrow D_1$ RB, D_2 FB

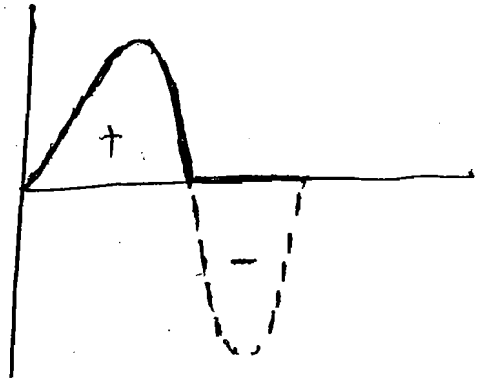
$0 < V_i < 5 \rightarrow D_1$ RB, D_2 RB



o/p.

Q. For the given circuit diagram draw the o/p waveform.

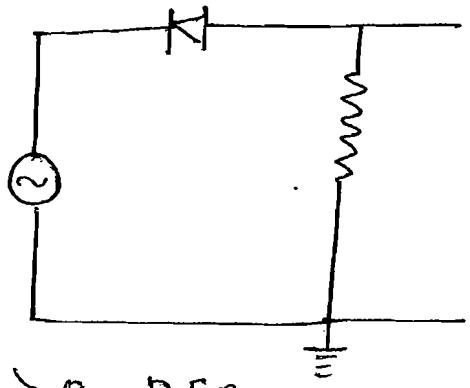


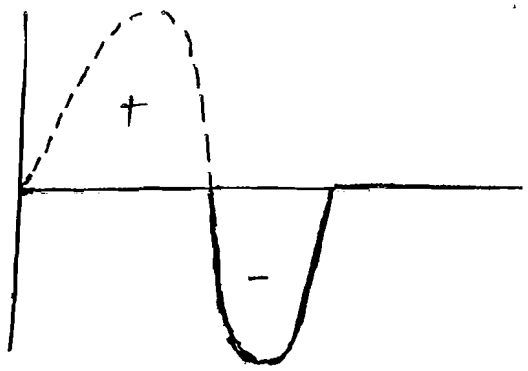


$V_i > 0$ FB

$V_i < 0$

Q. Draw the o/p waveform ?



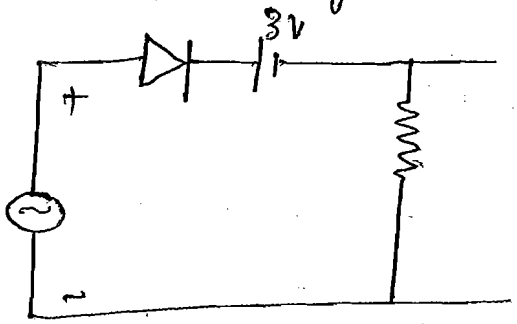


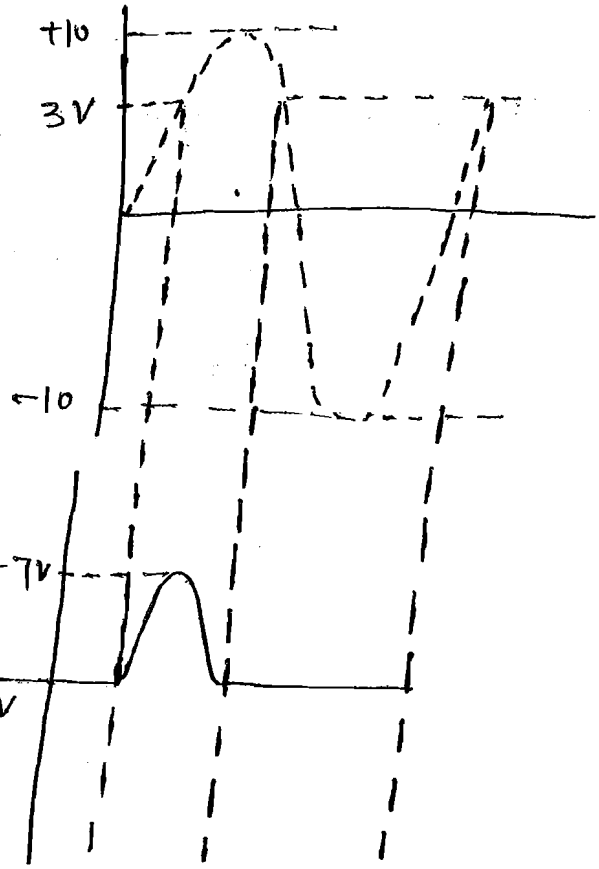
$V_i > 0$ DFB

$V_i < 0$ -V RB

o/p.

Qu Draw the o/p wave form ?





$V_i < 3 \rightarrow$ R.B o/p voltage

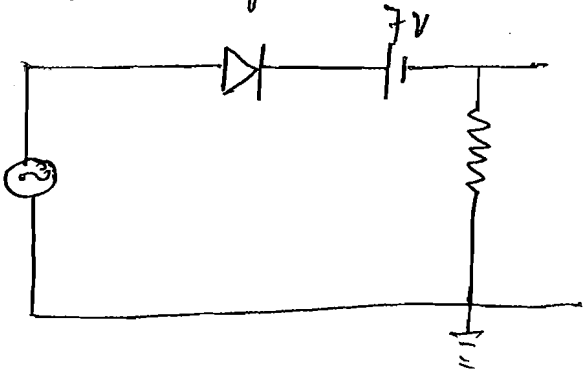
$-10 + 3 + V_o = 0$

$V_i > 3 \rightarrow$ F.B

$\boxed{V_o = 7}$

o/p waveform

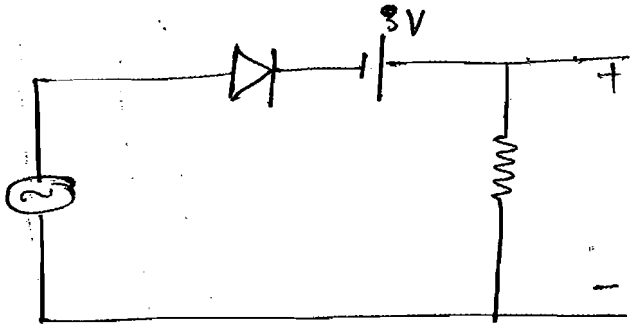
Qu Draw the o/p waveform ?



$V_i < 7 \rightarrow$ R.B

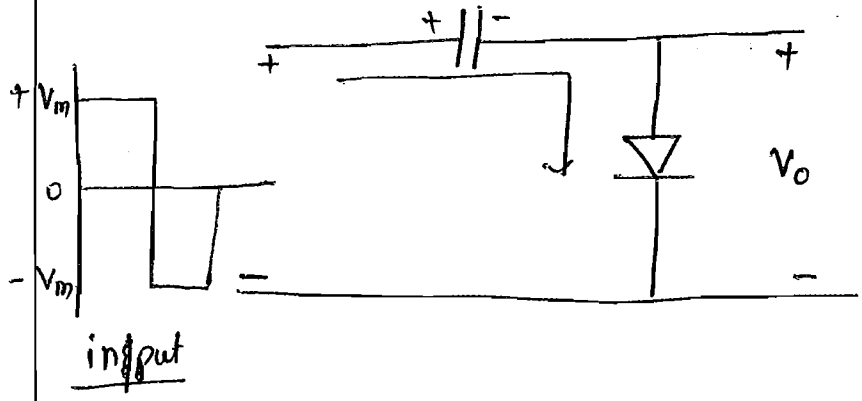
$V_i > 7 \rightarrow$ F.B.

Ques Draw the output waveform ?

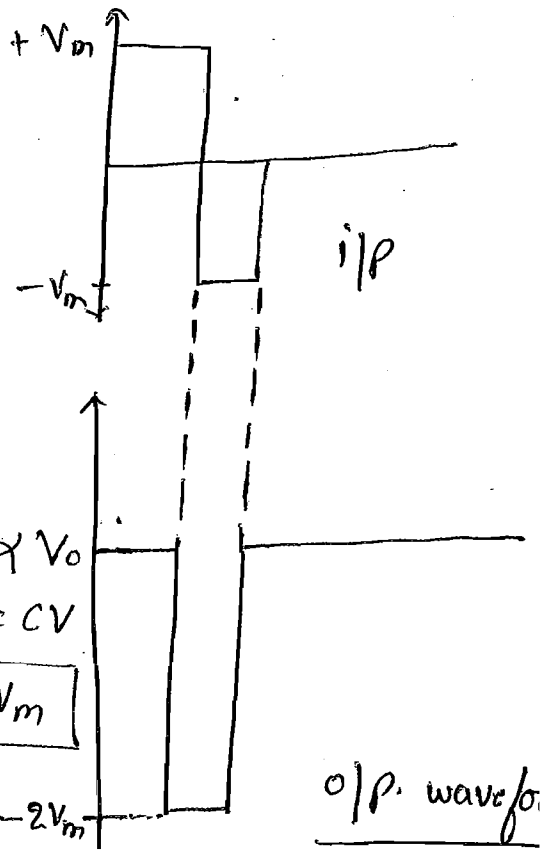


* **Clampers :-**

These are used to shift the level of the waveform by providing certain d.c. ammount The basic circuit elements are capacitor and diodes.



input



by KVL :-

$$-V + V_c + V_o = 0$$

$$\boxed{V_o = V - V_c}$$

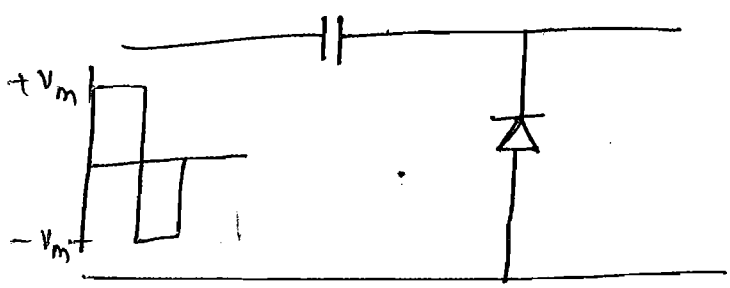
Case I :- $V = V_m$

$V_o = 0$

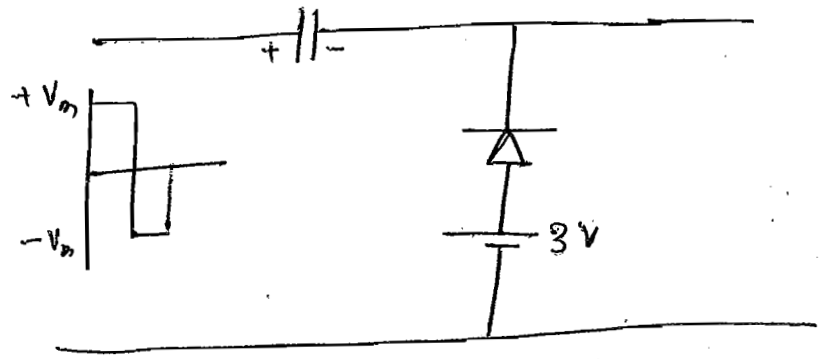
Case II :- $V = -V_m$

$$\boxed{V_o = -2V_m}$$

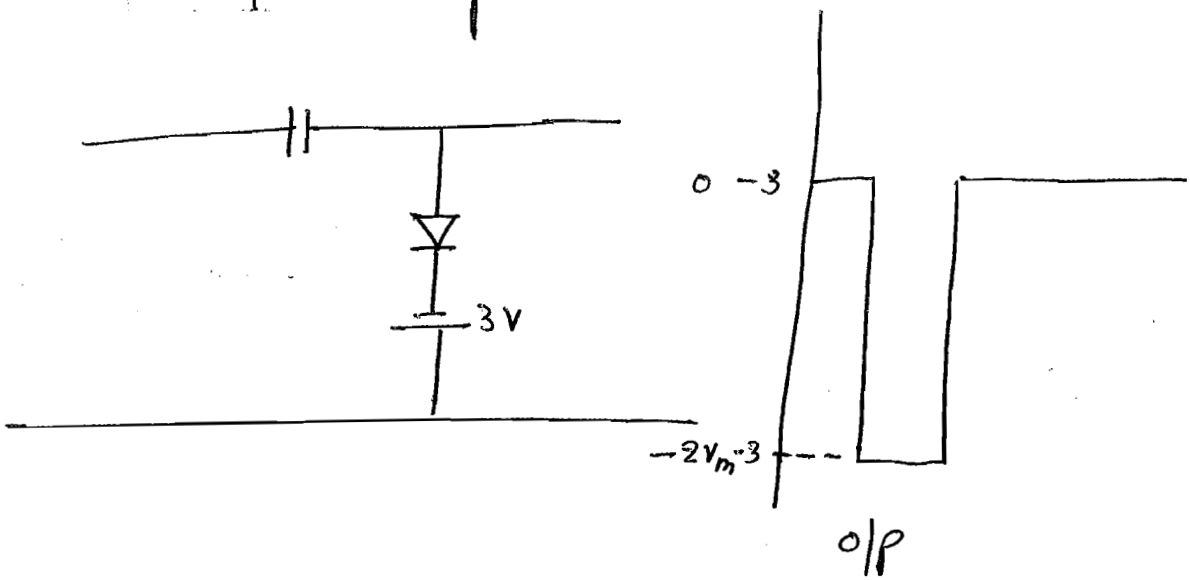
Q. for the given circuit diagram draw the o/p waveform.



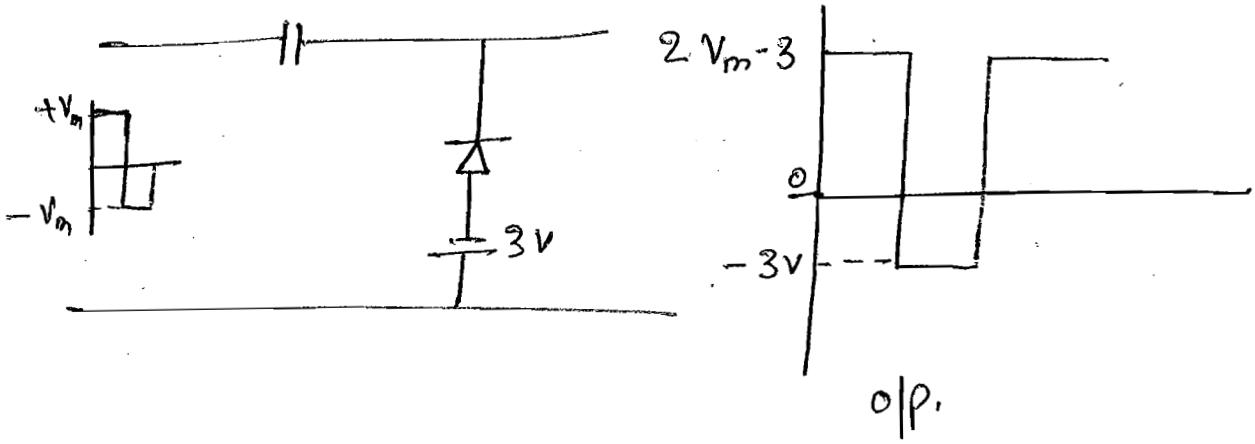
Q. For the given circuit diagram draw the o/p waveform.



Q. Draw the o/p waveform



Draw the o/p waveform



Zener Diode

Specially fabricated diode (only fabricated with Si's) the dopping level of zener diode is very high as compaired to ordinary diode.

Under forward bais condition it behaves as ordinary diode.

"The main application of zener diode is to operate under reverse bais condition."

* The application of zener diode is ~~:to operate~~

(i) Voltage Regulator

(ii) Voltage Refrence.

Note :- Si Ge

Conductivity :- $\sigma_{Si} < \sigma_{Ge}$

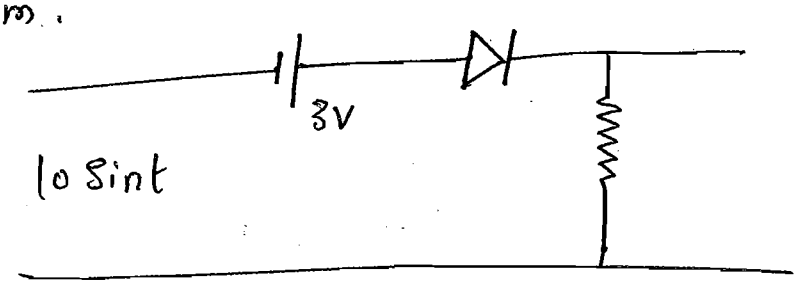
Leakage Current :- $I_{O\,Si} < I_{O\,Ge}$

$I_{O\,Si}$ ↓ nAmp. order

$I_{O\,Ge}$ ↓ μAmp. order

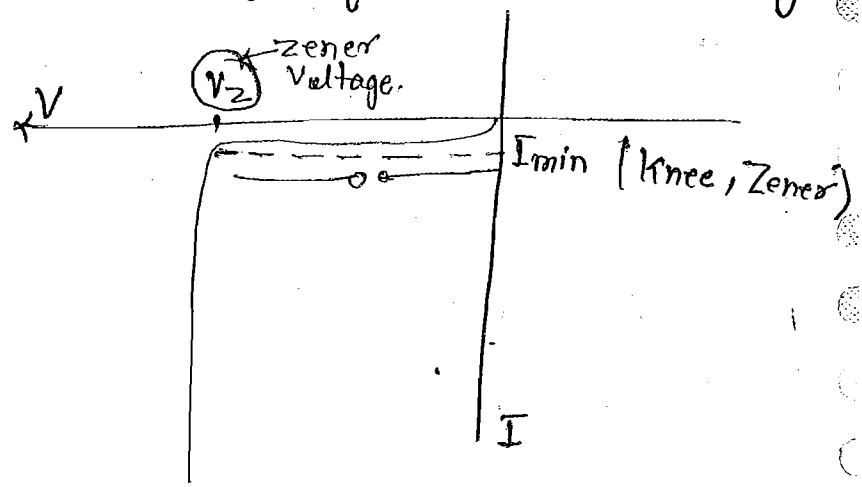
So Ge is not preferred over Si

Q. for the given diode Circuit. draw the o/p waveform.

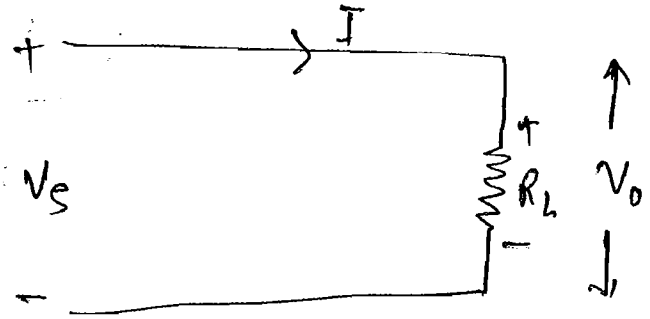


Under reverse bais condition before achiving breakdown voltage the current across zener ~~diode~~ diode is minimum, represented by broken wire.

Once the breakdown voltage achived or crosses the breakdown voltage zener diode will maintain a constant voltage of breakdown voltage.



* Zener Diode as Regulater :-



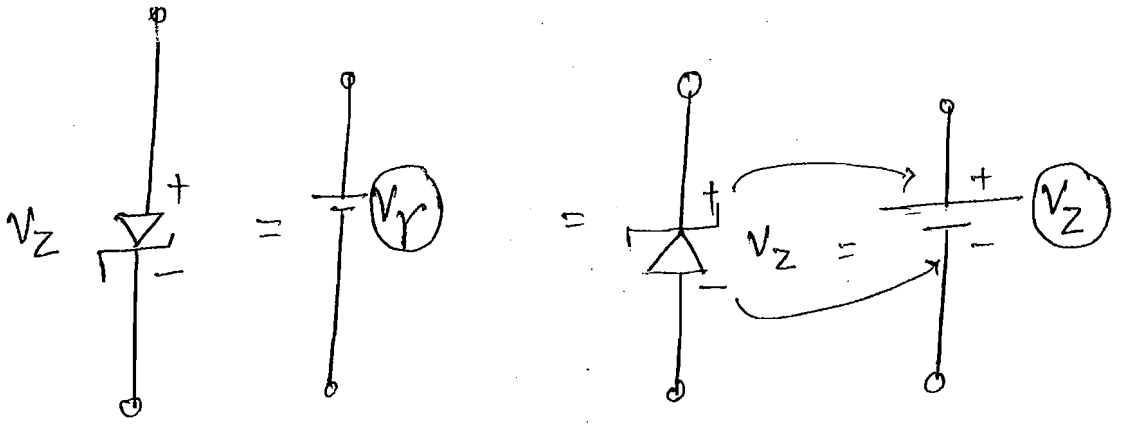
$-V_s + I R_L = 0$ $\quad \therefore \boxed{V_o = I R_L}$

(or) $\quad -V_s + V_o = 0$

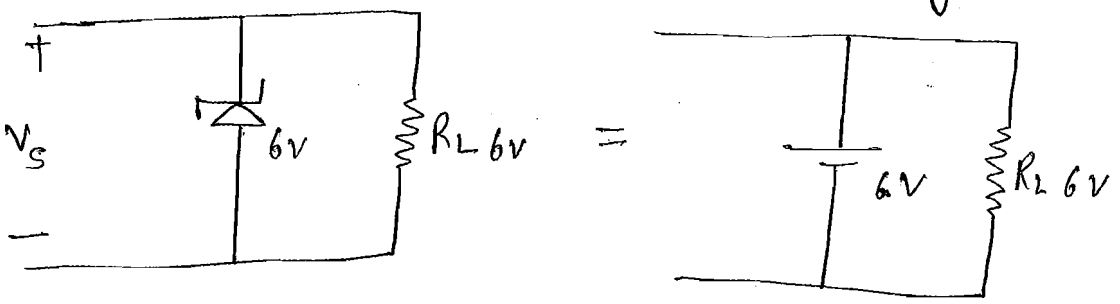
$$\boxed{V_o = V_s}$$

The output voltage. get ~~flat~~ fluctuates because of variatim in supply votage or variation in load resistance. R_L.

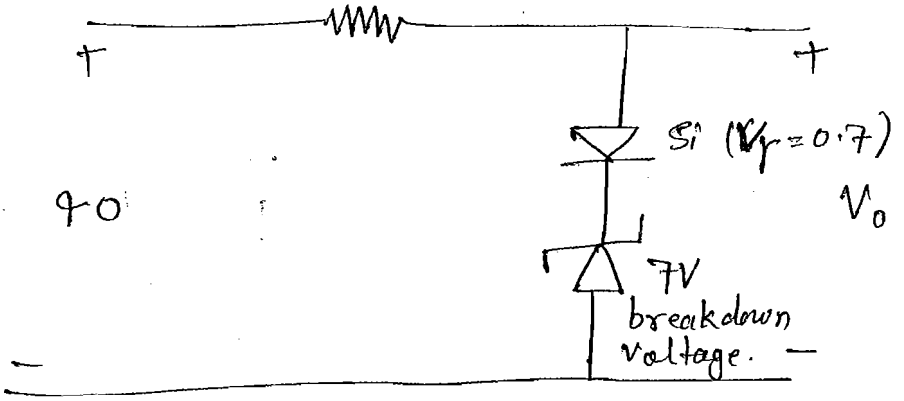
Equivalent symbol representation of Zener diode :-



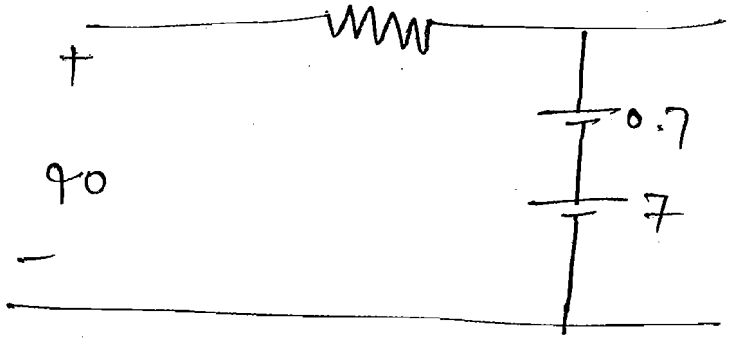
To maintain a constant output voltage a zener diode connected parallel with the load show that it maintains a constant output voltage.



Q. Soln for the given circuit diagram calculate output voltage?



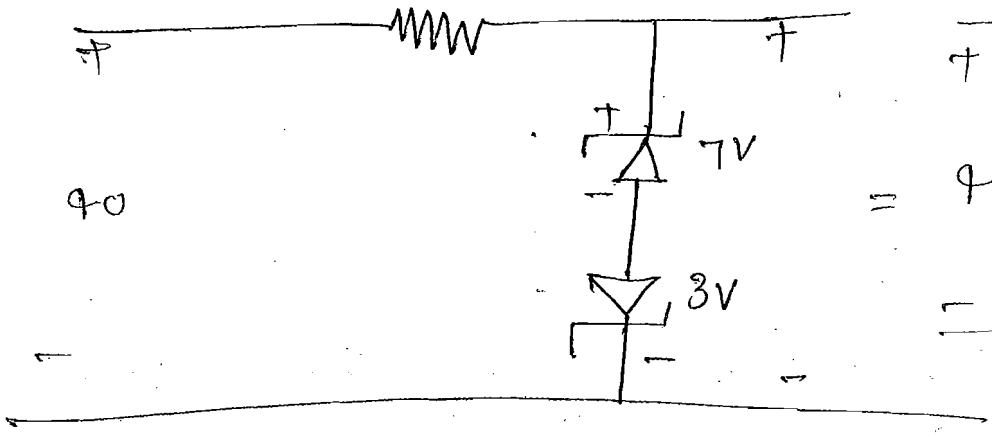
Soln Equivalent circuit diagram



$+0.7+7 = V_0$

$\boxed{V_0 = 7.7}$

Q. Calculate the output voltage?

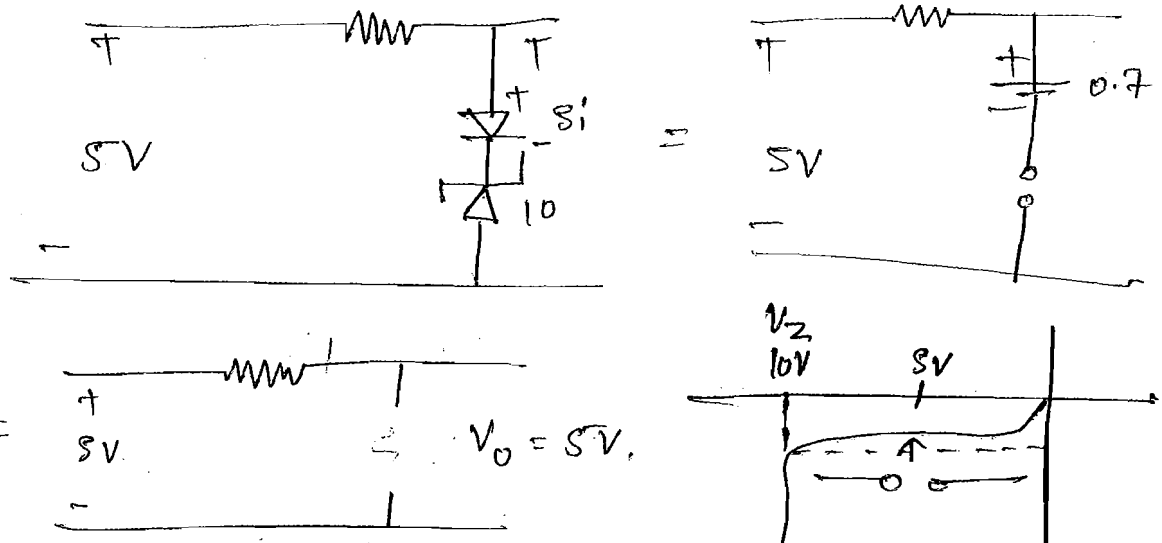


$+7+0.7 = V_o$

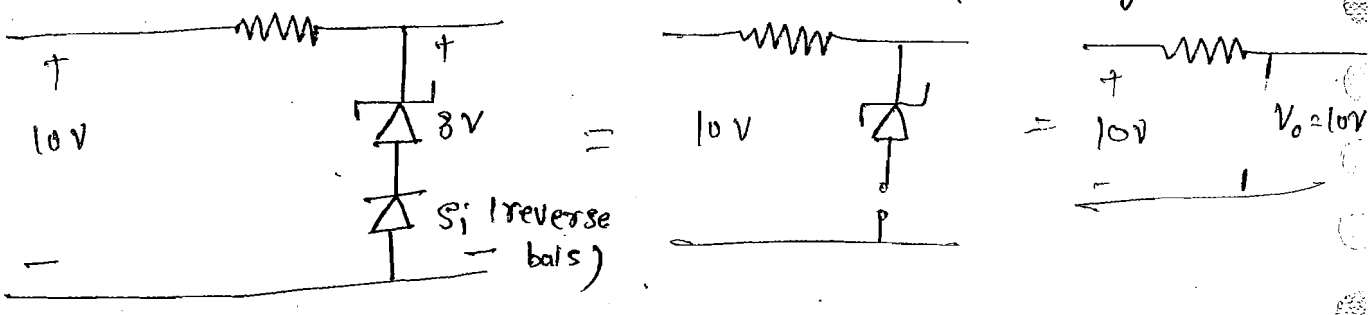
$\boxed{V_o = 7.7\,V}$

V. imp

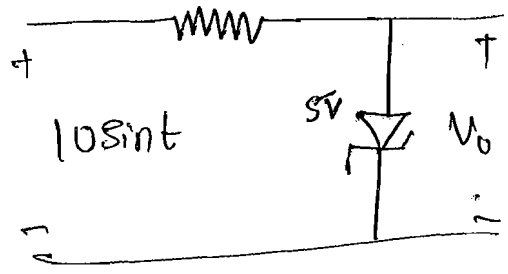
Q. Calculate the output voltage?

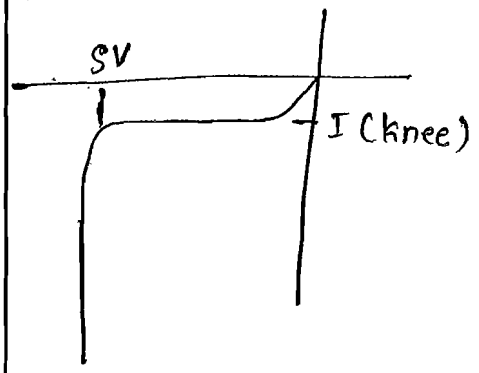


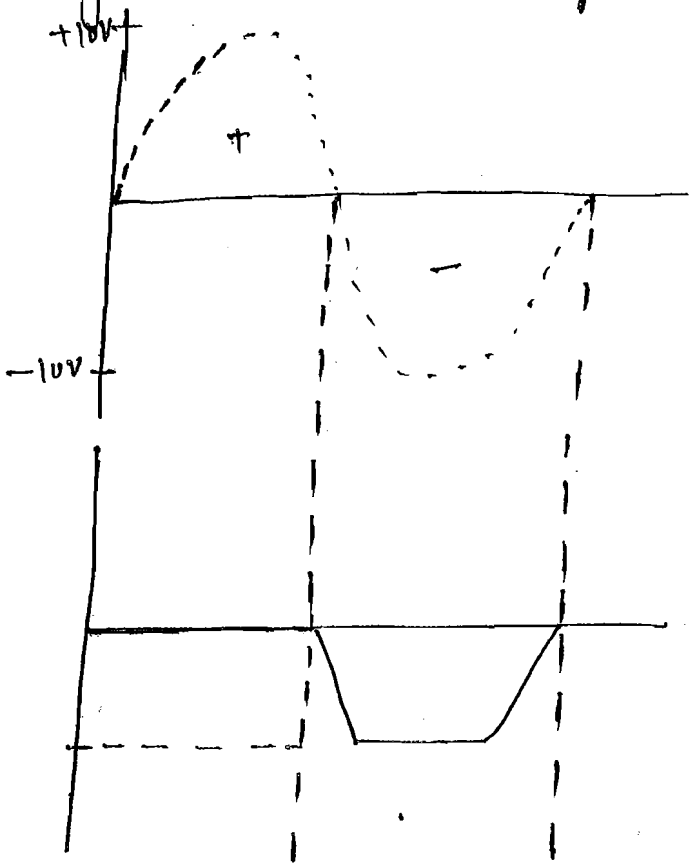
Q for the given circuit diagram calculate o/p voltage?



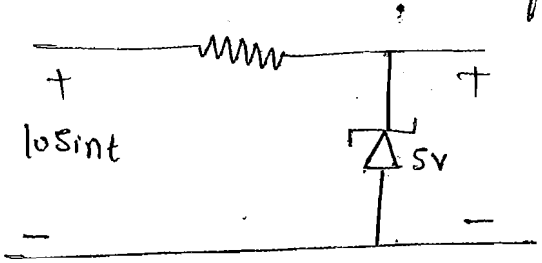
Q. For the given circuit diagram draw the output waveform

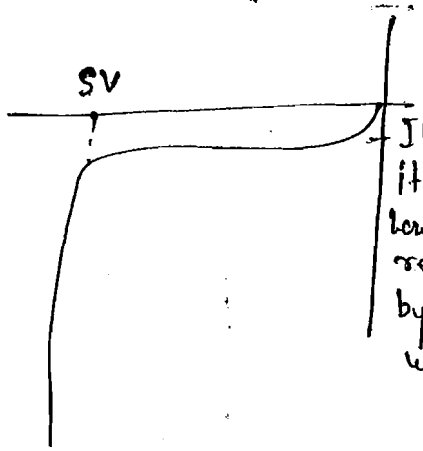


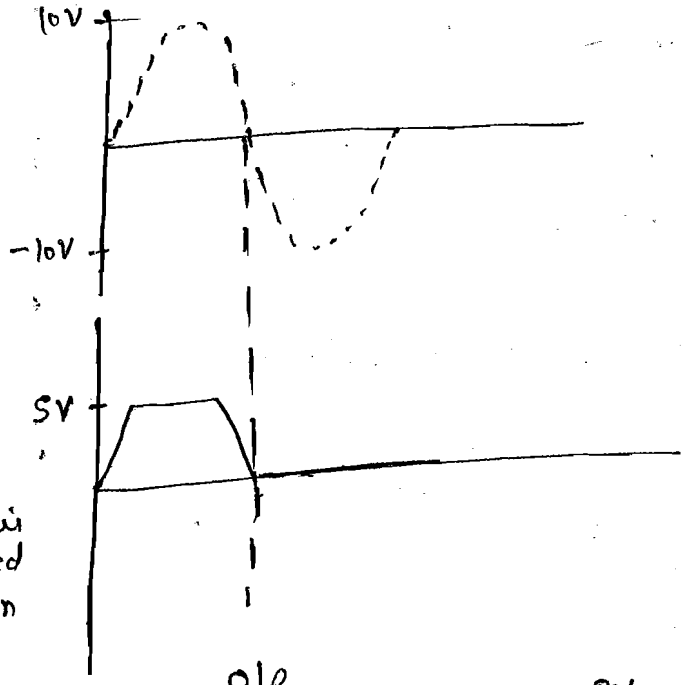




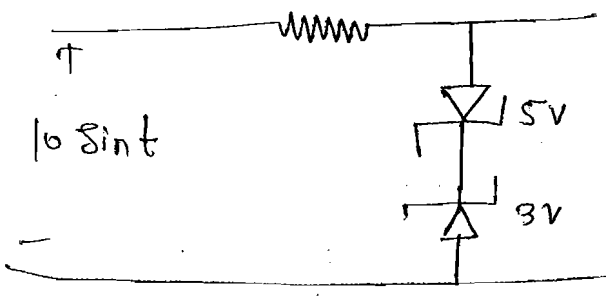
Q. Draw the o/p waveform ?

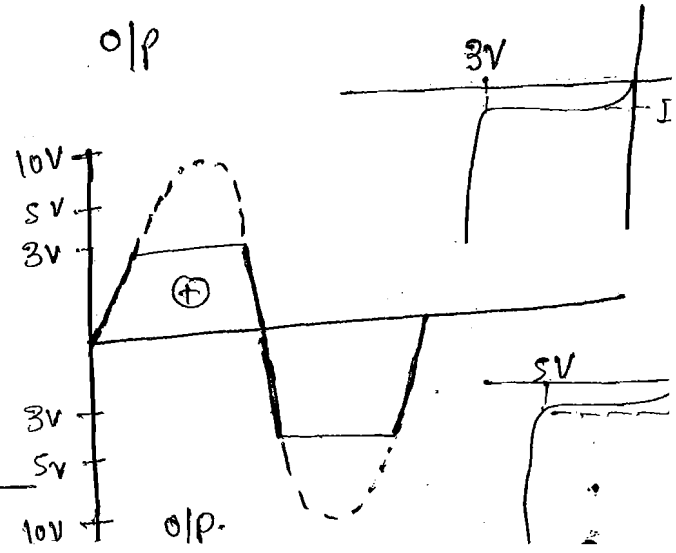




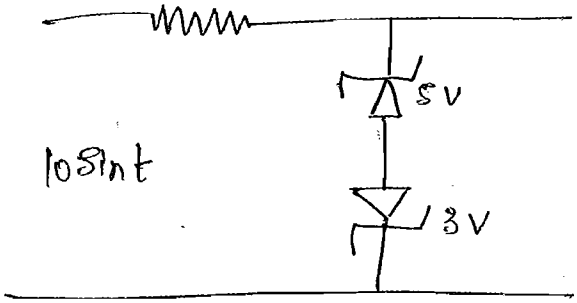


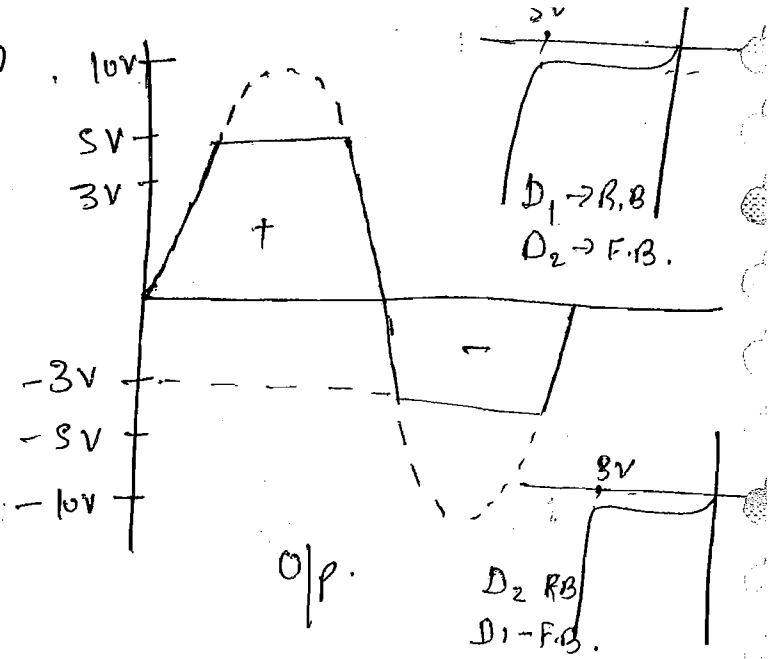
Q. Draw the o/p waveform ?



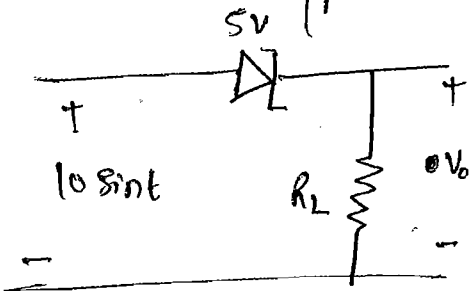


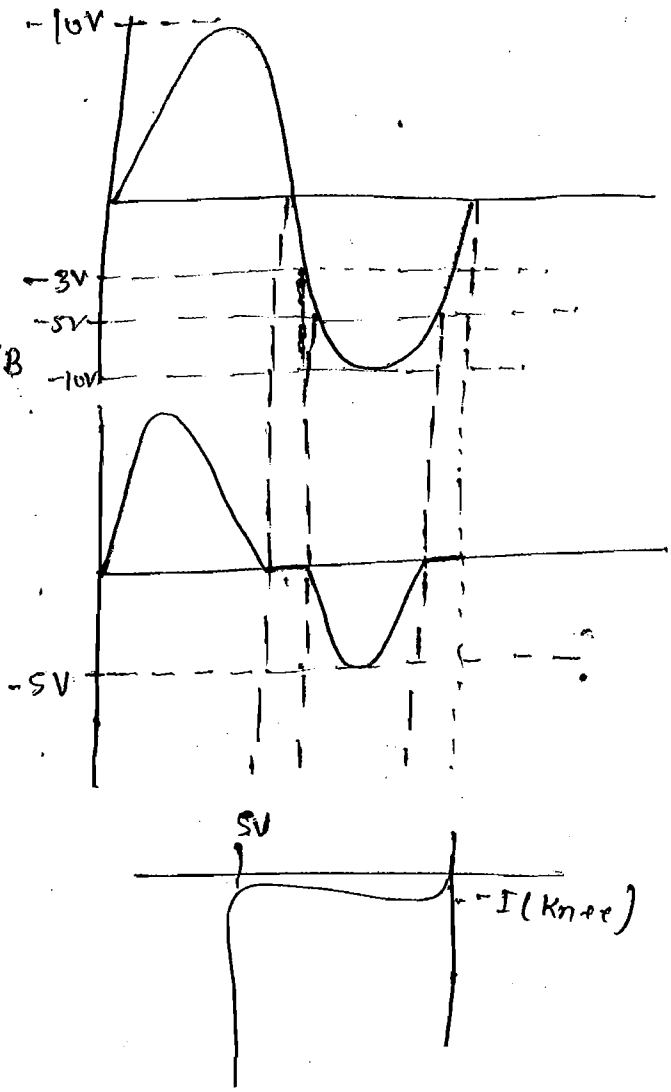
Q. Draw the o/p waveform





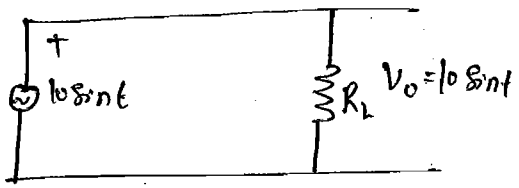
Q. Draw the o/p waveform





for +ve half cycle

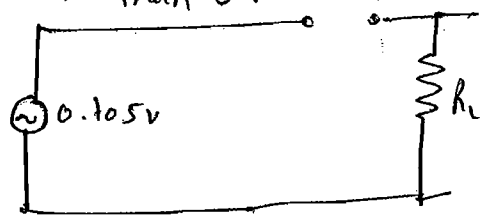
Diode is FB



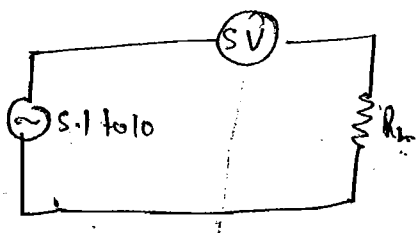
for -ve half cycle :-

Diode is RB

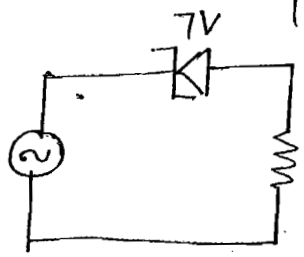
less than 5V



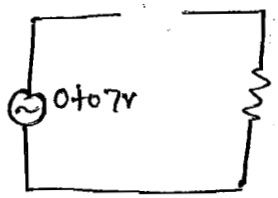
greater than 5V



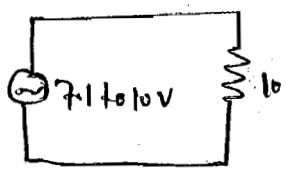
Q. Draw the o/p waveform

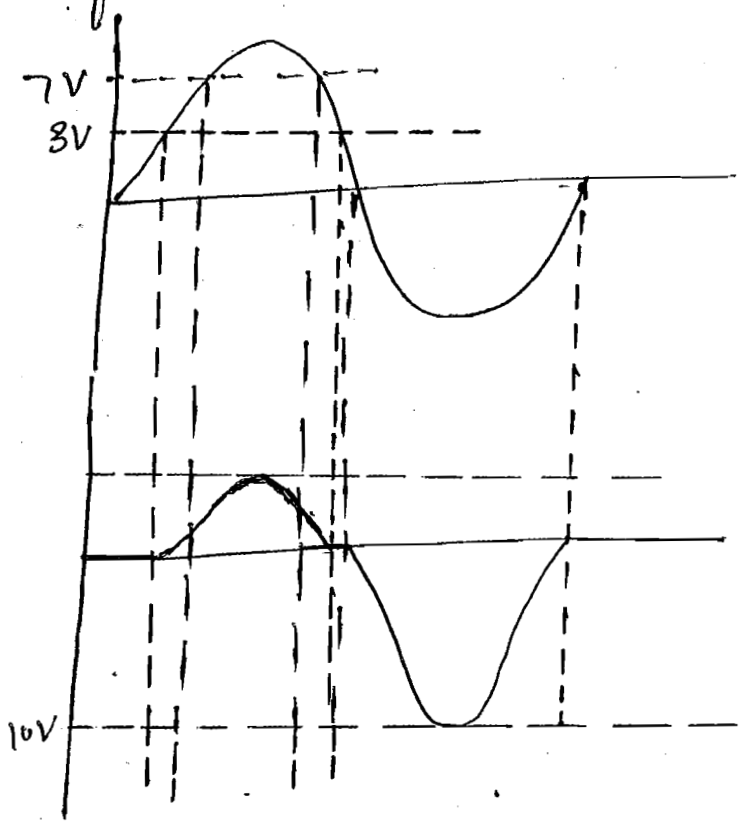


for +ve

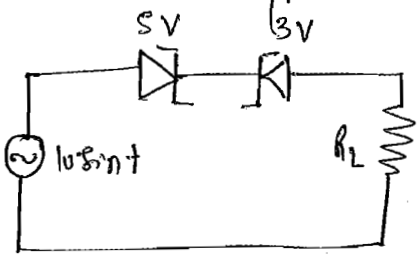


for -ve

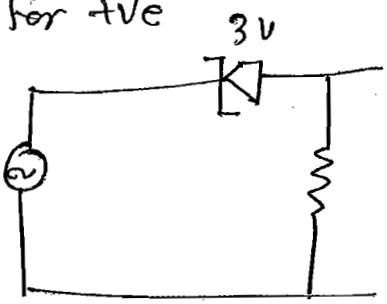




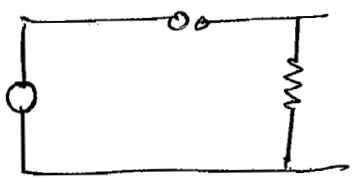
Q. Draw the o/p waveform



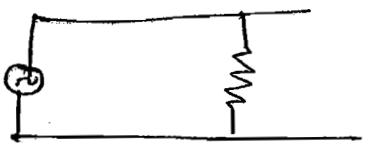
for +ve

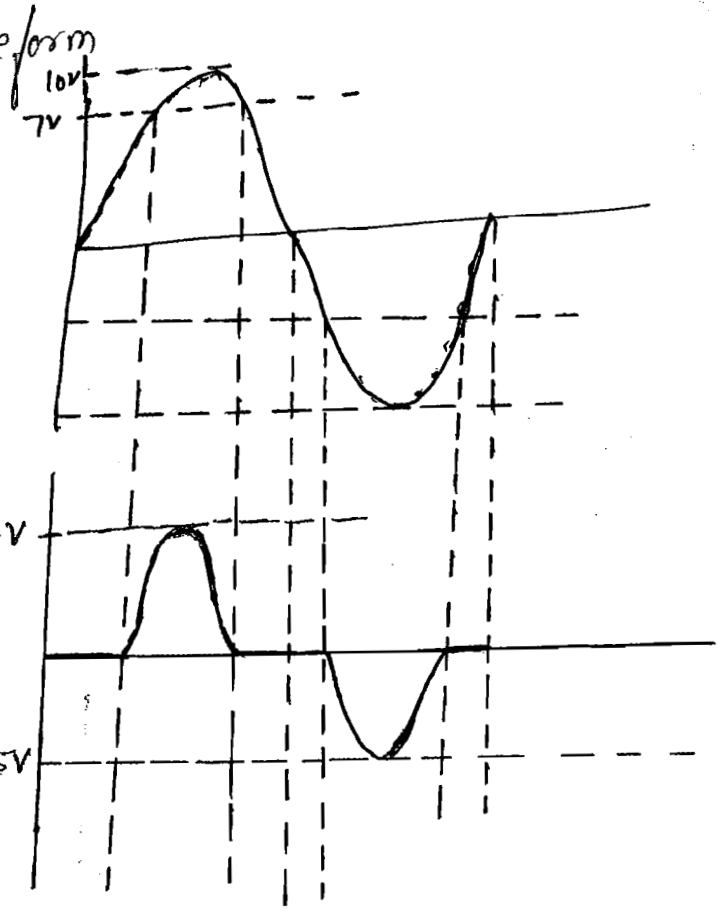


below 3V

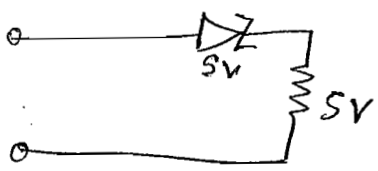


above 3V

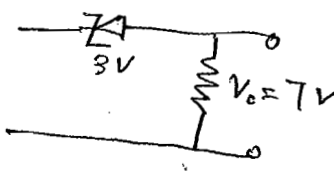




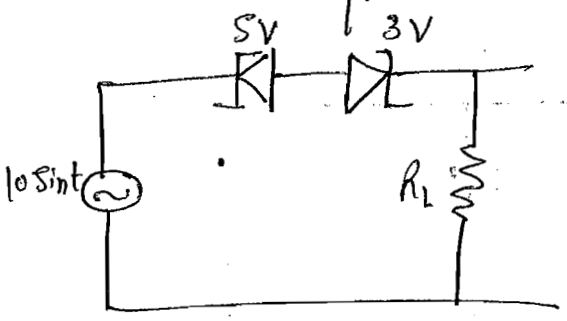
for -ve

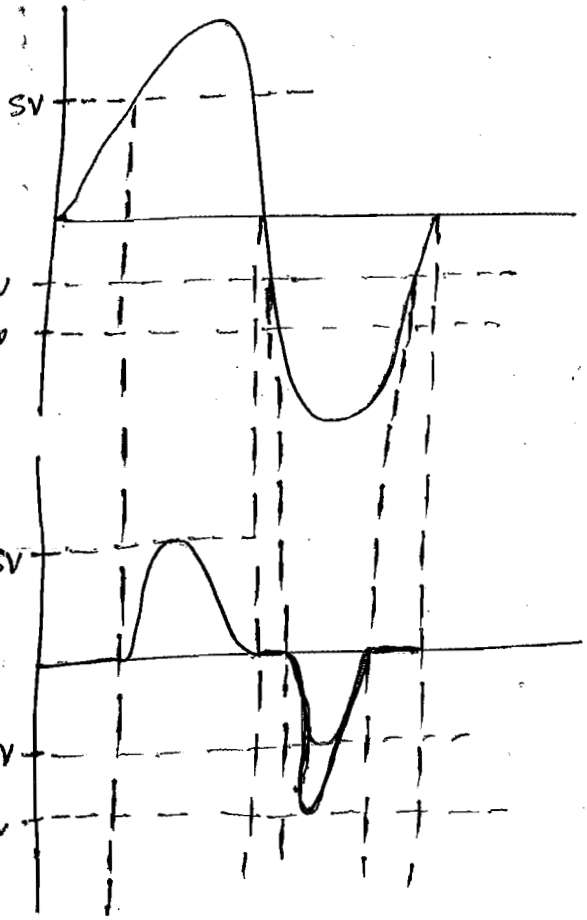


for +ve

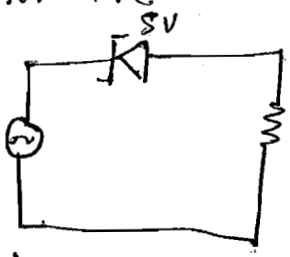


Q. Draw the o/p waveform

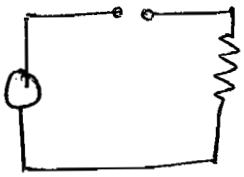




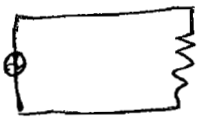
for +ve



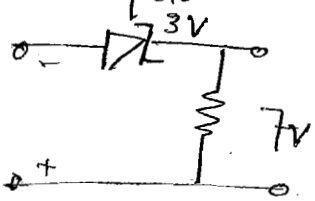
below 5 V



above 5V



for -ve half cycle

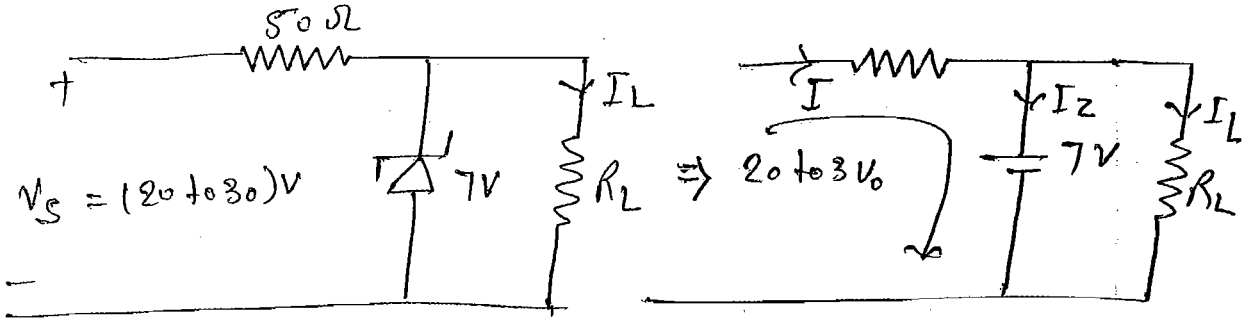


Pg-18

Q.96 Two identical Zener diodes are placed back to back in series and are connected to a variable DC power supply. The best representation of the I-V characteristics of the circuit is ?

(c).

Q.4 For the given circuit diagram shown in figure a zener diode having a breakdown voltage of 7V connected in parallel across load. If variation in the supply is 20 to 30V Calculate the maximum and minimum load current so that a knee current across the zener diode is 5m.A.



$$I = I_Z + I_L$$

$$\boxed{I_L = I - I_Z}$$

$$I_L = I - 5mA$$

$$(I_L)_{max} = (I)_{max} - 5mA \quad \text{—— (i)}$$

$$(I_L)_{min} = (I)_{min} - 5mA \quad \text{—— (ii)}$$

By K.C.L :-

$$-V_S + I.50 + 7 = 0$$

$$I = \frac{V_S - 7}{50}$$

$$I_{max} = \frac{30-7}{50} = \frac{23}{50} = 0.46\,A = 460mA$$

$$I_{min} = \frac{20-7}{50} = \frac{13}{50} = 0.26\,A = 260\,mA.$$

So from (i)

$$(I_L)_{max} = (460 - 5)\,mA = 455\,m.A$$

$$(I_L)_{min} = (260 - 5)\,mA = 255\,m.A.$$

Ans

* Maximum Power Dissipation across Zener Diode

$\because$ Power = Voltage × Current

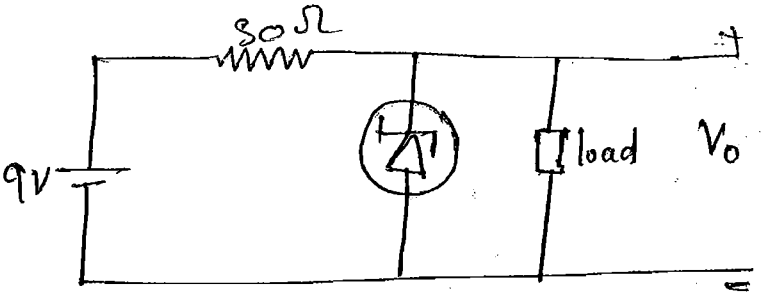
So $P_Z = V_Z I_Z$

↳ fix

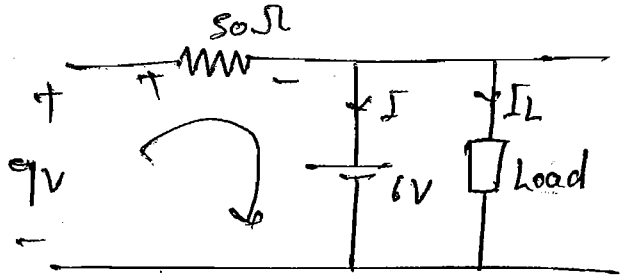
So $\boxed{(P_Z)_{max} = V_Z (I_Z)_{max}}$

Pg. 1

Q.4 A zener-diode shown in figure has a knee current of 5mA and a maximum allowed power



Soln



$-9 + I.50\,\Omega + 6 = 0$

$$I = \frac{9-6}{50} = \frac{3}{50} = 0.6\,A = 60\,mA.$$

$$I = I_Z + I_L$$

$$I_L = I - I_Z$$

$$I_L = 60\,mA - I_Z$$

$$(I_L)_{max} = 60 - I_{Z\,min} = 60 - 5$$

$$= 55\,m.A.$$

$(I_L)_{min} = (I_Z)_{min} = 60\,mA - (I_Z)_{max} = 60 - 50$

$\boxed{(I_Z)_{min} = 10\,mA.}$

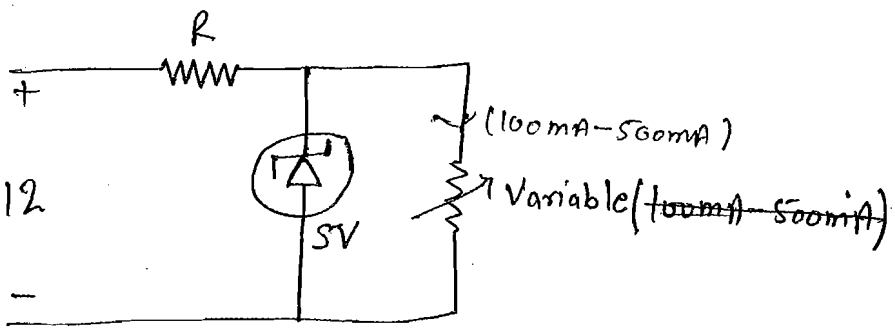
$P_Z = V_Z I_Z$

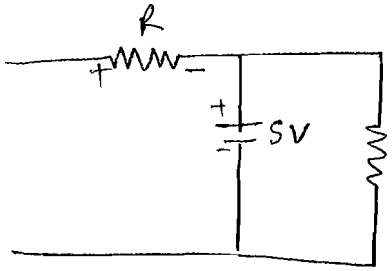
$300mW = 6\, I_{Z\,max}$

$\boxed{I_Z = 50mA}$

Pg-2
Q.7

Sol^n





$-12 + IR + 5 = 0$

$R = \frac{12-5}{I} = \frac{7}{I}$

$\boxed{R = \frac{7}{I}}$ — (9)

$\because \quad I = I_Z + I_L$

$(I)_{max} = 500\,mA$

$(I)_{min} = 100\,mA$

$R_{max} = \frac{7}{I_{max}} = \frac{7}{500mA} = 14\,\Omega$

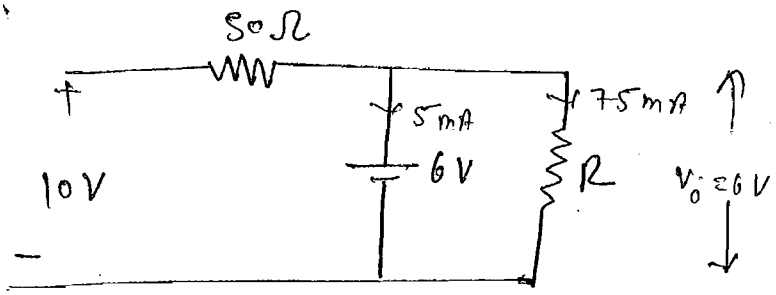
$R_{min} = \frac{7}{I_{min}} = \frac{7}{100mA} = 70\,\Omega$

So

$\boxed{R = \frac{70}{3}\,\Omega}$ Ans

(9)

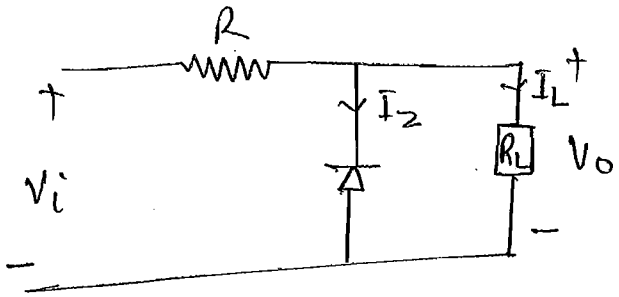
Soln



$$-10 + I \cdot 50 + 6 = 0$$

$$I = \frac{4}{50} = 80\,m.A$$

(11)



$$-V + I \cdot R + 10 = 0$$

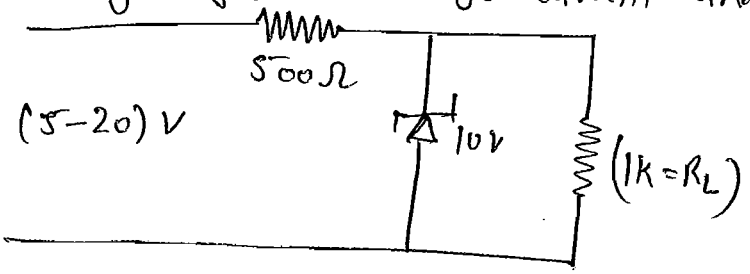
$$\boxed{R = \frac{V - 10}{I}}$$

$$I = I_2 + I_L$$
$$= 1 + 10$$
$$I = 11\,mA$$

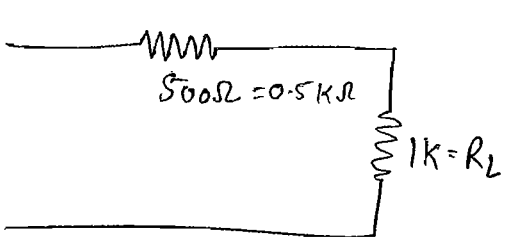
$$R = \frac{(V - 10)}{11\,m.A} = (R)_{max} = \frac{50 - 10}{11} = \frac{40}{11} = 3.6\,k\Omega$$

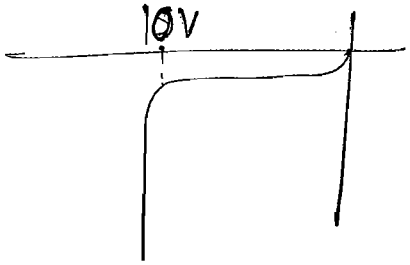
$$(R)_{min} = \frac{30 - 10}{11} = \frac{20}{11} = 1.8\,k\Omega$$

Q. For the given circuit shown calculate the Ratio of maximum and minimum power at the load. If zener diode is having negligible leakage current and breakdown voltage = 10V



Case I : $V_1 = 5V$





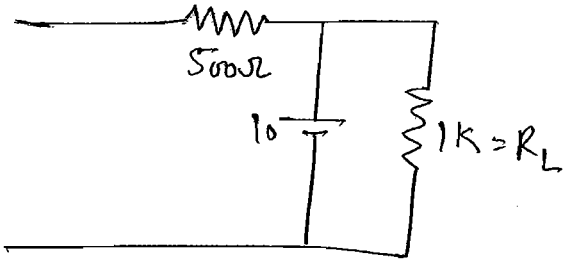
$$V_{RL} = \frac{5 \times 1K}{0.5K} = \frac{50}{15} = 3.33\,V$$

$$\boxed{V_{RL} = 3.33\,V}$$

$$P_L = \frac{V^2}{R} = \frac{(3.33)^2}{1} =$$

$$\boxed{(P_L)_{min} = 11\,mW}$$

Case II : $V = 20V$

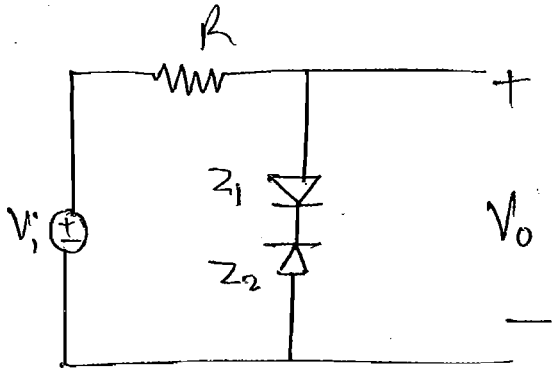


$$V_i = 20V$$

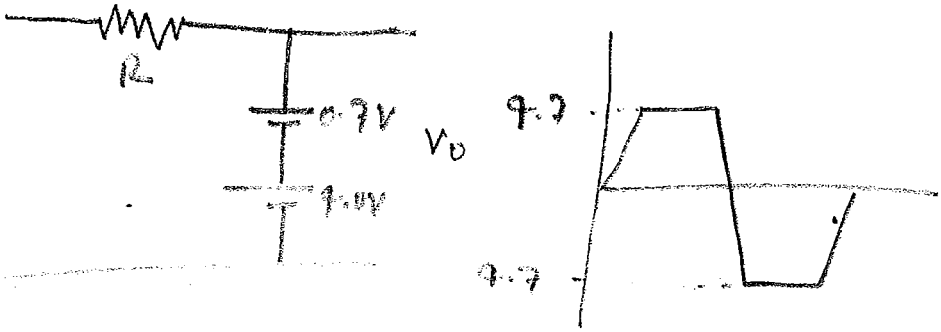
$$P = \frac{10^2}{1K} = 100\,mW$$

$$\frac{P_{max}}{P_{min}} = \frac{100mw}{11mw} = 9.09$$

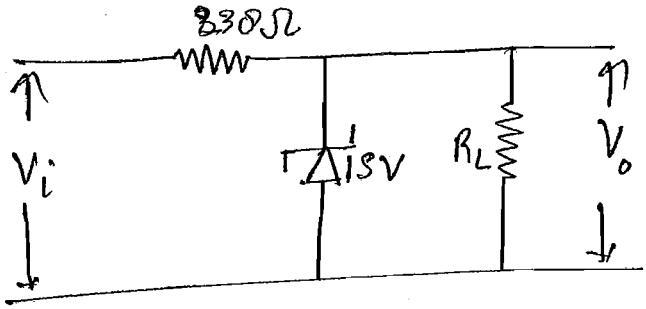
Q.5

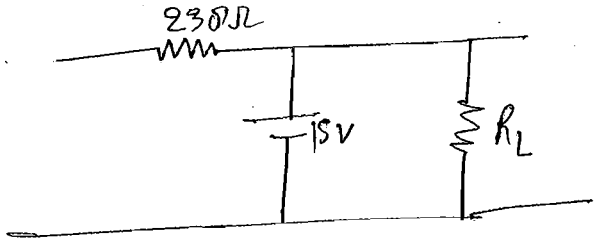


for +ve half cycle



Q.6





$$-V_i + I.230 + 15 = 0$$

$$V_i = I.230 + 15 \quad \text{— (a)}$$

$I = I_Z + I_L$

Power $(P_L) = V_L I_L \Rightarrow I_L = \frac{P_L}{V_L} = \frac{150}{15} = 10mA$

$\boxed{(I_L)_{max} = 10\,mA}$

$P_Z = V_Z I_Z$

$I_Z = \frac{P_Z}{V_Z} = \frac{200}{15} = 13.33\,mA$

$(I_Z)_{max} = 13.33\,m.A.$

$I_{max} = (I_Z)_{max} + (I_L)_{max} = 13.33 + 10$

$\boxed{I_{max} = 23.33\,m.A}$

$V_i = 230 \times 23.33\,m.A + 15$

$((V_i)_{max} = 20.5)$

$\because \quad I = I_Z + I_L$

$I = 0 + 10$

$\boxed{I = 10\,mA}$

$V_i = 2.300 + 15$

$\boxed{V_i = 17.4}$

So Range of V_i = 17.5 V to 20.5 V Ans

NUMBER SYSTEM

Base or Radix of Number system:-
no. of digits used in any number system. It represents

Number System	No. of digits
Binary (2)	0 — 1
Septal (7)	0 — 6
Octal (8)	0 — 7
Decimal (10)	0 — 9
Hexadecimal (16)	0 — 15 (F).

* Decimal to other Conversion
other to decimal Conversion
other to other Conversion
Arithmetic & logic operation among diff no. sys
Complement of a no. System.

* Desimal to other Conversion:-

$(25)_{10} \longrightarrow (11001)_2$

$(25)_{10} \longrightarrow (31)_8$ $\quad 8\,|\,25\,|\,1 \uparrow \;\; 3$

$(25)_{10} \longrightarrow (34)_7$ $\quad 7\,|\,25\,|\,4 \uparrow \;\; 3$

$(25)_{10} \longrightarrow (31)_8 \longrightarrow (34)_7$

"Base of the number system is inversely proportional to number inside the argument". or (bracket).

Q. Identify the values of R_1 and R_2 ?

$(235)_{R_1} = (565)_{10} = (1065)_{R_2}$?

(a) 12, 8 (b) 16, 8 (c) 8, 12 (d) 8, 16

Sol"

16 | 565 — 5
16 | 35 — 3
2

$(565)_{10} \longrightarrow (235)_{16}$

Q. Identify x ?

$(123)_x = (12x)_3$

If we have 3 so we can't have 3 in argument

x is not considered so

(a) 3 (b) −4 (c) 5 (d) None ✓

for 5 in second 5 is not consider

Q. $(25.625)_{10} \longrightarrow (\ ?\ )_2$

Sol"

$(25)_{10} \longrightarrow (11001)_2$

0.625 × 2 = 1.250 — 1 out

0.25 × 2 = 0.50 — 0 out

0.50 × 2 = 1.00 — 1 out

So $(25.625)_{10} \longrightarrow (11001.101)_2$

Q. $(25.625)_{10} \longrightarrow (\ ?\ )_2$

$(25)_{10} \longrightarrow (31)_8$

$$\begin{array}{r} 0.625 \\ \times\ 8 \\ \hline 5.000 \end{array}$$

So $(25.625)_{10} \longrightarrow (31.5)_8$

* Other to decimal Conversion :-

Q. $(11001)_2 \longrightarrow (\quad)_{10}$

MSB ↑ LSB

4 3 2 1 0

$1 \times 2^0 + 0 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4$

$= 1 + 8 + 16 = 25$

$(11001)_2 \longrightarrow (25)_{10}$ Ans

Q. $(11001.101)_2 \longrightarrow (\quad)_{10}$

4 3 2 1 0 −1 −2 −3

$1 \times 2^0 + 0 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3}$

$= 1 + 8 + 16 + \frac{1}{2} + \frac{1}{8}$

$25 + \frac{5}{8} = 25 + 0.625$

$= 25.625$

$(11001.101)_2 \longrightarrow (25.625)_{10}$ Ans

Q. $(31)_8 \longrightarrow (\quad)_{10}$

Soln $1 \times 8^0 + 3 \times 8^1$

$1 + 24 = 25$

$(31)_8 \longrightarrow (25)_{10}$

Q. $(31.5)_8 \longrightarrow (\quad)_{10}$

Soln $1 \times 8^0 + 3 \times 8^1 + 5 \times 8^{-1}$

$25 + \frac{5}{8} = 25.625$

$(31.5)_8 \longrightarrow (25.625)_{10}$

Imp Q. $(123)_n = (124)_3$

$\Rightarrow 3 \times n^0 + 2 \times n^1 + 1 \times n^2 = 4 \times 3^0 + 2 \times 3^1 + 1 \times 3^2$

$3 + 2n + n^2 = 4 + 6 + 9$

$n^2 + n - 12 = 0$

$n = \frac{-1 \pm \sqrt{1^2 - 4 \times -12}}{2 \times 1}$

$n = \frac{-1 \pm 7}{2} = 3, -4.$

$n = 3, -4$ It is not satisfies so option is none of these.

* **Octal Number System :-**

Octal numbers can be represented in range of 3-bit binary since the ranges are satisfied.

000 → 0
001 → 1
010 → 2
011 → 3
100 → 4
101 → 5
110 → 6
111 → 7

* **Hexadecimal Number System :-**

Hexadecimal can be represented in terms of 4-bit binary.

0000
0001
0010
0011
0100
0101
0110
0111
1000
1001 — 9

1010 — 9+1 = A
1011 — 9+2 = B
1100 — 9+3 = C
1101 — 9+4 = D
1110 — 9+5 = E
1111 — 9+6 = F

Q. Perform the conversion $(123.73)_8 \longrightarrow (\quad)_{16}$

Soln

$(123.73)_8 \longrightarrow (053.FC)_{16}$

001 010 011 . 111 011

0 5 3 . E C

Q. Find the minimum decimal equivalent of $(11C.0)_{13}$

(a) 194 (b) 283 (c) 384 (d) 333

$C \times 16^0 + 1 \times 16^1 + 1 \times 16^2$

∵ we find minimum decimal equivalent

So $(11C.0)_{13|14|15|16}^{12}$ so for minimum we have base = 13

$12 \times 13^0 + 1 \times 13^1 + 1 \times 13^2 = 12 + 13 + \ldots = 194$ Ans

Q. Perform the addition $(127)_8 + (172)_8$

Soln

$$\begin{array}{r} {\scriptstyle 1\ 1} \\ 127 \\ 172 \\ \hline 321 \end{array}$$

$8 \mid 9 \quad 1$ (1)

$8 \mid 10 \quad 2$ (1)

So $= (321)_8$ Ans

Q. The addition of two numbers are given as $12.3 + 13.0 = (32.0)$ Then perform the substraction ?

$322 - 133$

Soln

$$\begin{array}{r} {\scriptstyle 1} \\ 12.3 \\ +\ 13.0 \\ \hline 32.0 \end{array}$$

$4 \mid 4 \quad 0$ (1) $= 10$

4

$(322)_4$

$-\ (133)_4$

$(123)_4$ Ans

Q. Perform the multiplication $(1111)_2 \times (1111)_2$

Soln

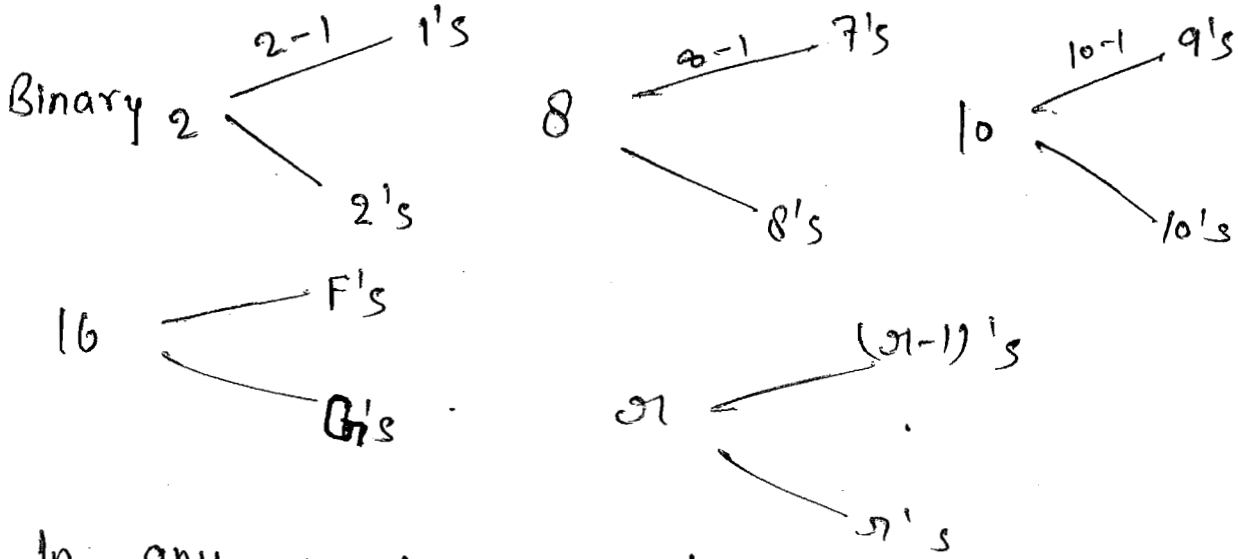
$$\begin{array}{r} 1111 \\ \times\ 1111 \\ \hline 1111 \\ 1111\times \\ 1111\times\times \\ 1111\times\times\times \\ \hline 11100001 \end{array}$$

$$\begin{array}{r} 10 \\ 10 \\ \hline 100 \end{array} \qquad \begin{array}{r} {\scriptstyle 1} \\ 11 \\ 11 \\ \hline 110 \end{array} \qquad \begin{array}{r} 11 \\ 10 \\ \hline 101 \end{array}$$

* Compliment of Number System :-

In modern computer system Two's (2's) Compliment representation is mainly used for performing arithmetic operations.

It reduces the hardware requirement.



In any number system in general base r then there exist two types of Compliment -

(1) (r-1)'s Compliment

(2) r's Compliment.

Example Sol^{n} 1010, Calculate 1's Compliment?

```
  1 1 1 1   <-- largest no. of this no. system.
  1 0 1 0
  | | | |
  0 1 0 1
```

and sub. it find 1's Compliment

Imp. * "To calculate (r-1)'s compliment select maximum digit of that no. system subtract each and every bit with that maximum value. the result is (r-1)'s compliment."

(8493) 10 ← 10's

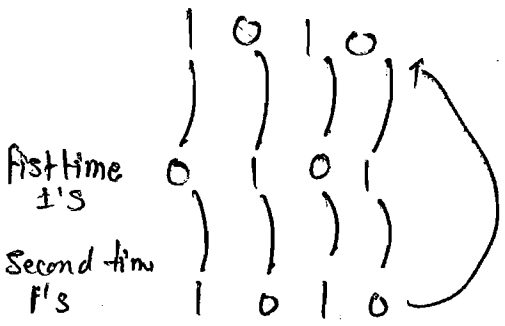
9999
−8493
1206 ← 9's Compliment.

Q. Find the F's Compliment of (3,2,C,A) ?

Soln

FFFF
3 2 C A
C D 3 5 ← F's Compliment.

* "To Calculate r's Compliment from (r-1)'s Complimen add 1 at Least significant Bit (LSB)."



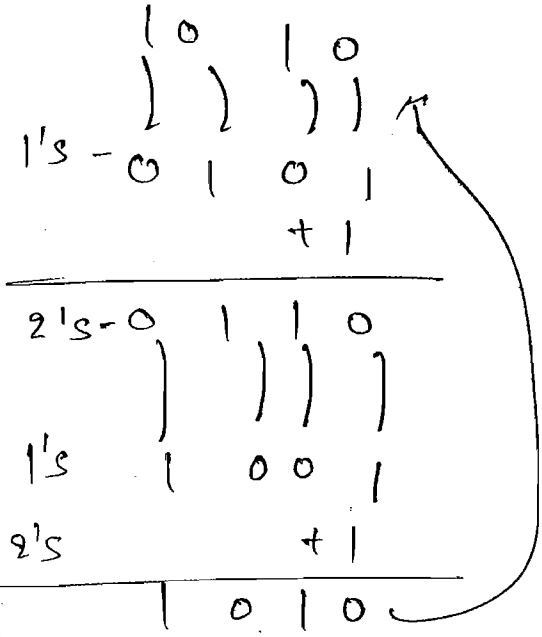
9999
6798
3201 → 9's Comp. first time.

9's

10

9999
3201
6798 — 9's Comp. Secon

In any number system two times (r-1)'s Compliment produces same result.

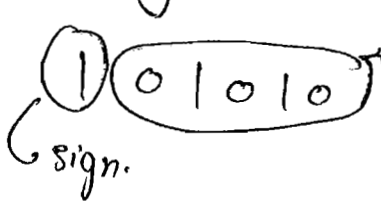


9999
3202
1's 6797
+1
2's 6798

9999
6798
3201
+1
3202

"In any no. system in general two times either (r-1)'s Complemunt or r's Compliment produces same result."

* Signed Magnitude Representation :-



MSB = 1 = Neg -ve
MSB = 0 = No's = +ve

In an n-bit binary representation M.S.B. will give sign. If MSB = 1 ⇒ No = -ve
MSB = 0 ⇒ No = +ve.
Rest (n-1) bit will give the magnitude of the number.

3-bit binary	Sign magnitude	Compliment 1's	Compliment 2's
0 0 0	+ 0	+0 (No change)	+0
0 0 1	+ 1	+1	+1
0 1 0	+ 2	+2	+2
0 1 1	+ 3	+3	+3
1 0 0	- 0	+3	-4
1 0 1	- 1	-2	-3
1 1 0	- 2	-1	-2
1 1 1	- 3	-0	-1
	Rang -3 to +3	rang -3 to +3	increas range (-4 to +4)

The disadvantage of sign magnitude is separate representation of +0, -0 require excess (large) memory space. Hence hardware requirement increases.

Note :- Compliment of any number system are only calculated for -ve nubers.

* ~~2's Compliment~~ The advantage of 2's Compliment is -0 removed.
Range of representation also increases.

* Range of Representation of sign magnitude and 1's Compliment :-

Range :- -3 to $+3$

$$-[2^{(3-1)}-1] \text{ to } +[2^{(3-1)}-1]$$

for n bit

$$\boxed{-[2^{(n-1)}-1] \text{ to } +[2^{n-1}-1]}$$

* Range of Rep. of ~~Sng~~ 2's Compliment :-

$$\boxed{-[2^{(n-1)}] \text{ to } +[2^{(n-1)}-1]}$$

Q. Find the 2's Compliment of $(-17)_{10}$.

```
      1 1 1 1 1
      1 0 0 0 1
    ---------------
1's   0 1 1 1 0
          + 1
    ---------------
2's   0 1 1 1 1
```

2	17	1
2	8	0
2	4	0
2	2	0
	1	

For sign (for -ve sign use 1

So $(-17)_{10} = (10111)$ ← 2's Comp.

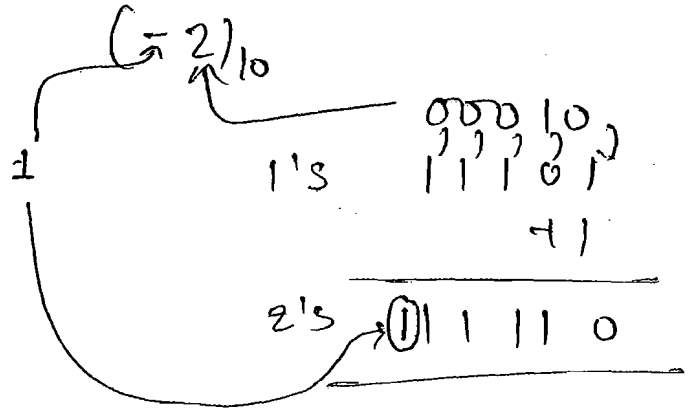
Q. Find the 2's Comp. of $(-2)_{10}$

```
  10
  01
  +1
  --
  10
```

So $(-2)_{10} \longrightarrow (110)$ ← 2's Comp.

Q. Repeate the previous ques for 6-bit comp.

Soln



since in previous ques $(-2)_{10} = 110$

So

111	110
	110

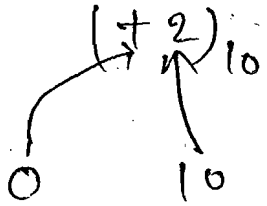
↑ Sign bit

Note:-

⇒ "Whenever it is required to represent the compliment of any no. system by using additional bits Copy sign bit to the additional places."

Q. Find the 2's Compliment of $(+2)_{10}$

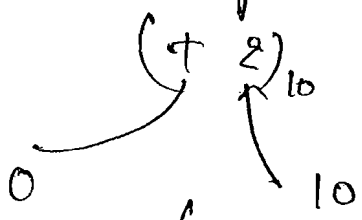
Soln



So (010) Ans

Q. Repeate the previous ques use 6-bit representation.

Soln



for 6-bit 00010

So

0 00010	
	0 10

↑ Sign bit.

So (000010) Ans

* Weighted and Unweighted Code :-

Weighted Code :-

In the number system representati each and every bit is assigned by using significant ~~point~~ positions. Such code representati is called Weighted Code.

If the codes are represented in the arbitrary manner in which each and every bit ~~doe~~ does not have significant bit are called as Unweighted Code.

Ex-

Weighted	Unweighted
B C D code	Gray
Decimal code.	Excess - 3
8 4 2 1	
2 4 2 1	
5 2 1 1	
3 3 2 1	

* B.C.D Code :-

Self Complimentary

8 4 2 1	5 2 1 1	2 4 2 1
0 - 0 0 0 0	0 0 0 0 - 0	0 0 0 0 - 0
1 - 0 0 0 1	0 0 0 1 - 1	0 0 0 1 - 1
2 - 0 0 1 0	0 0 1 1 - 2	0 0 1 0 - 2
3 - 0 0 1 1	1 1 0 1 - 3	0 0 1 1 - 3
4 - 0 1 0 0	0 1 1 1 - 4	0 1 0 0 - 4
5 - 0 1 0 1	1 0 0 0 - 5	0 0 1 1 - 5
6 - 0 1 1 0	1 0 1 0 - 6	1 1 0 0 - 6
7 - 0 1 1 1	1 1 0 0 - 7	1 1 0 1 - 7
8 - 1 0 0 0	1 1 1 0 - 8	1 1 1 0 - 8
9 - 1 0 0 1	1 1 1 1 - 9	1 1 1 1 - 9

By Calculation of 9's Compliment the resultent also gives 1's Comp. Such codes are also called as self Complementary Codes.

forex- 5211, 3221, 2421

8421 is non-self Complementary Code.

* Excess-3 Code :-

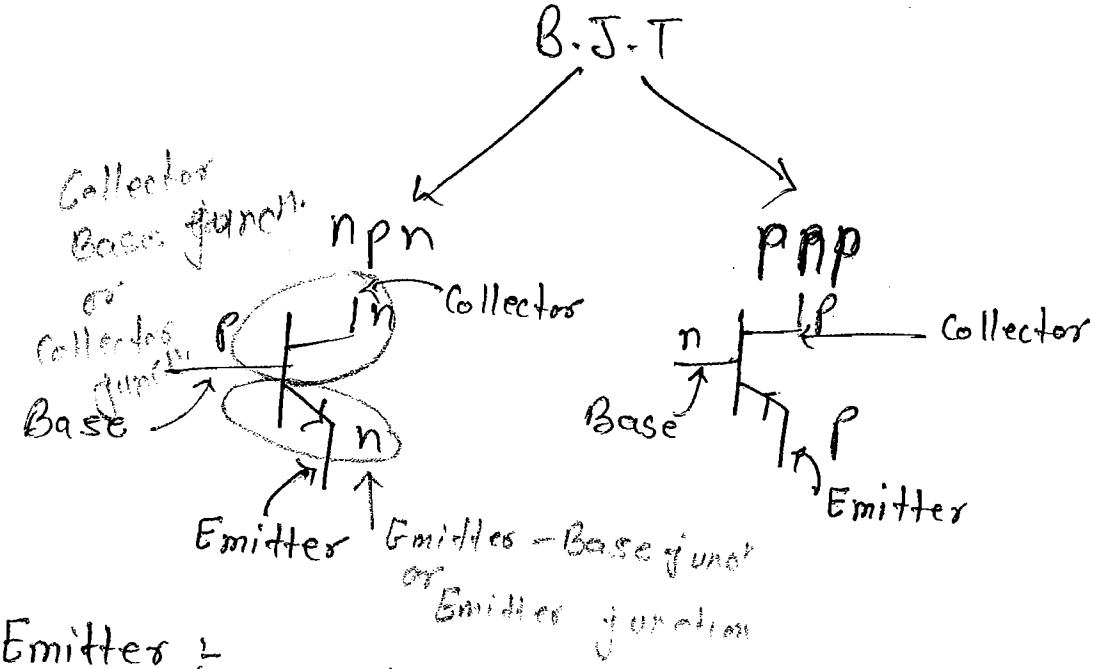
Excess-3 represents values from 0 to 9 but by adding 3 [0 to 9)+3] to each value.

8421	Excess-3
0 0 0 0	0 0 1 1
0 0 0 1	0 1 0 0
0 0 1 0	0 1 0 1
0 0 1 1	0 1 1 0
0 1 0 0	0 1 1 1
0 1 0 1	1 0 0 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 1 0
1 0 0 0	1 0 1 1
1 0 0 1	1 1 0 0

self Complementary

Some thing leakage.

* B.J.T :- (Bipolar junction transistor) :-



* Emitter :-
The function of emitter is to supply majority carriers. Doping of emmiter must be very high.

* Collector :-
The collecter is used to collect all the majority carrier supplied by emitter. The doping of collecter must be comparitivily less w.r. to emitter.

* Base :-
Base is also called as transit region through which majority carriers reaches to collector. Widths of the base must be as smaller as possible. Base will be having least doping.

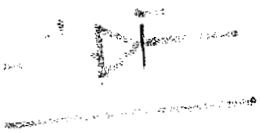
In any transistor there exist. two junctions.

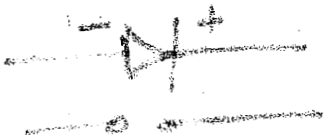
1. J_{EB} / J_E (2) J_{CB} / J_C

The main purpose of transistor is to operate as amplifier.

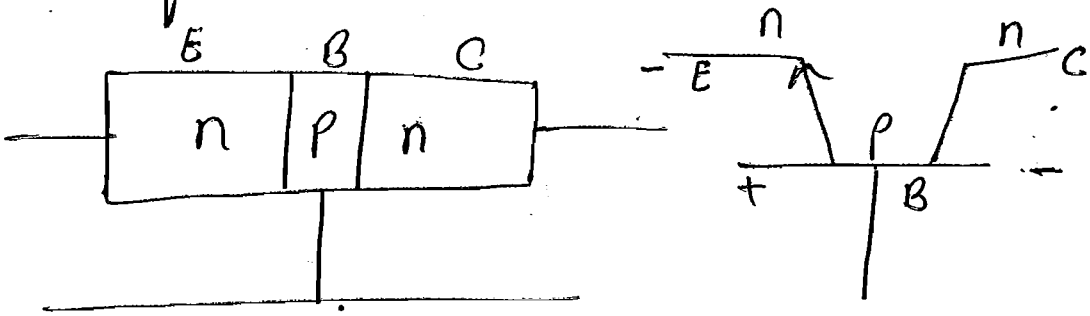
becoz transistor is costly so it is used as amp.
Diode is less cost so it is use as a switch

Region	J_{EB}/J_E	J_{CB}/J_C	Application
Active	F.B.	R.B.	Amplifier
Saturation	F.B.	F.B.	ON · Switch.
Cut off	R.B.	R.B.	Off · Switch
Inverse Active	R.B.	F.B	Attenuation



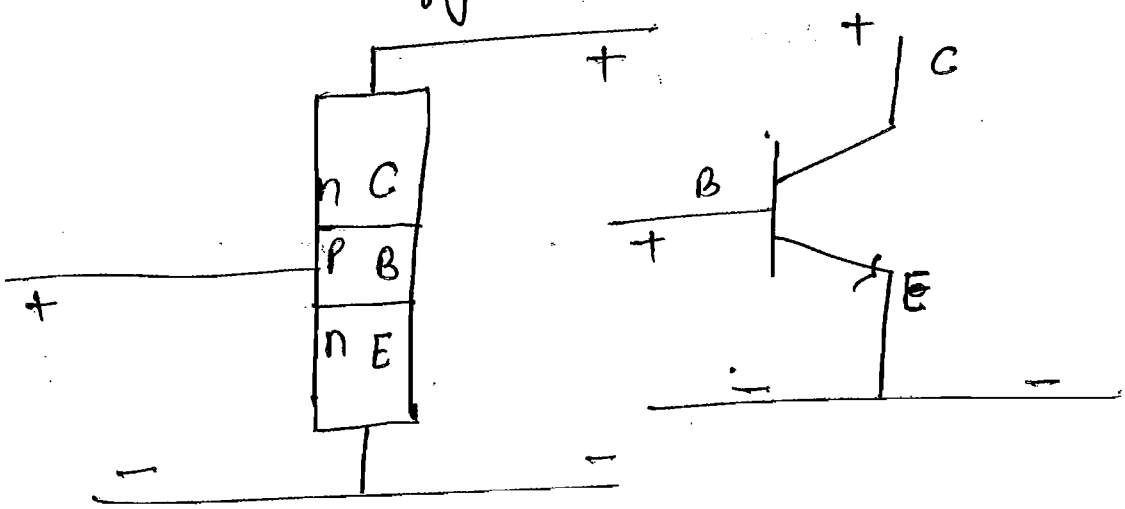


* Configuration Of Transistor :-



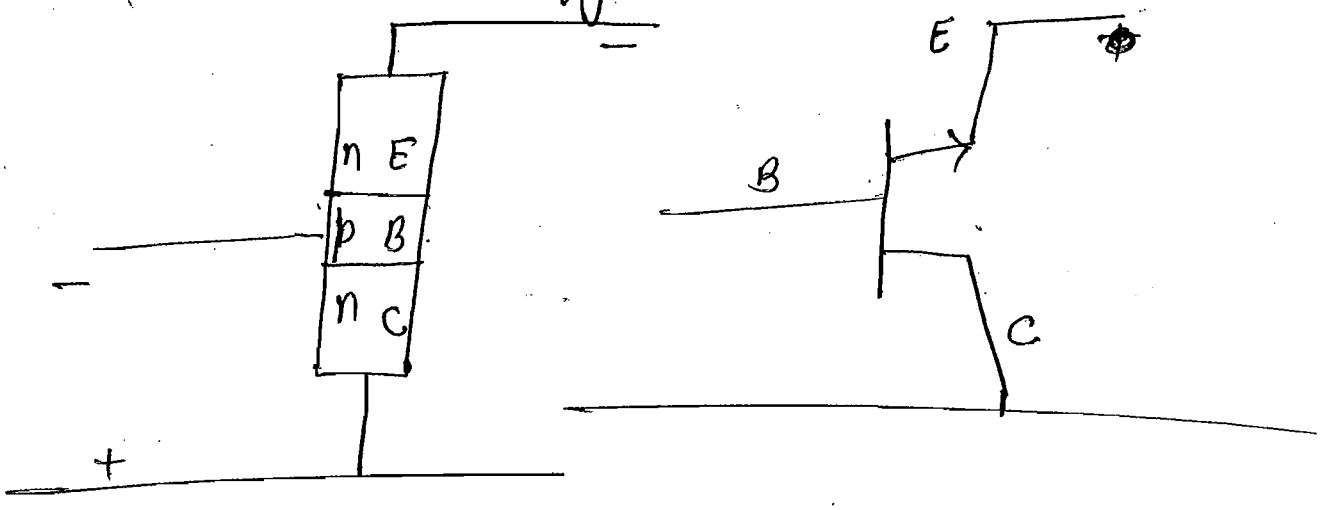
Comon Base Configuratim.

* Common Emitter Configuration :-



Common Emitter Configuration

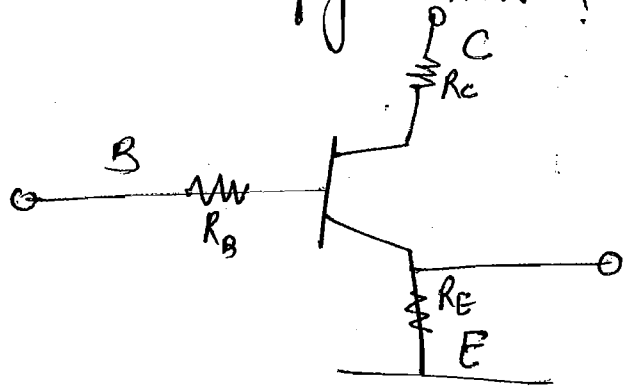
* Common Collector Configuration :-



Common Collector Configuratia

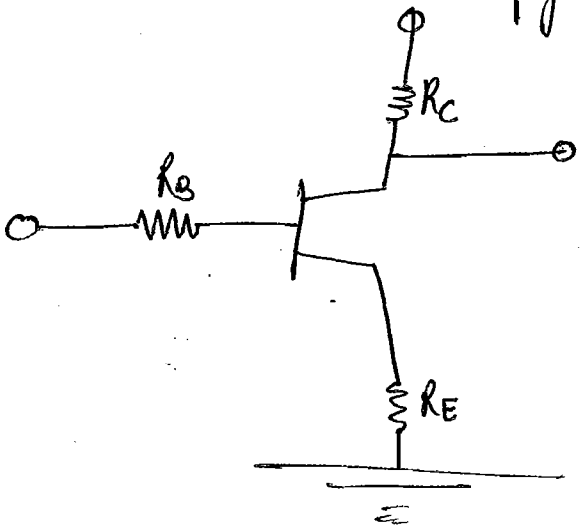
Q. Identify the Configuration ?

(i)



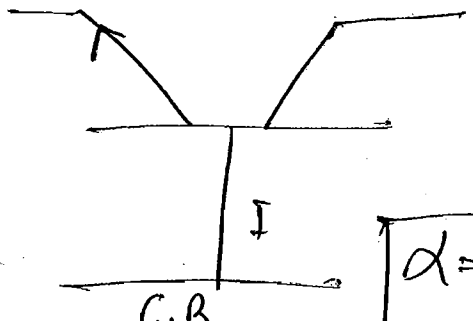
Common Collector Configuration

(ii)

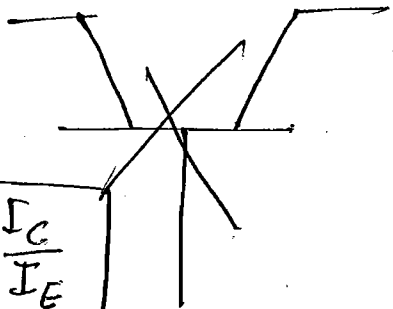


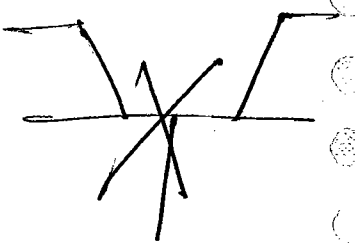
Common Collector Configuration.

Q.

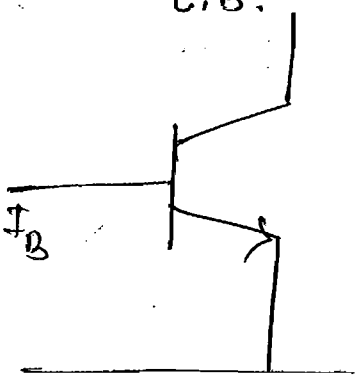


$$\alpha = \frac{I_C}{I_E}$$

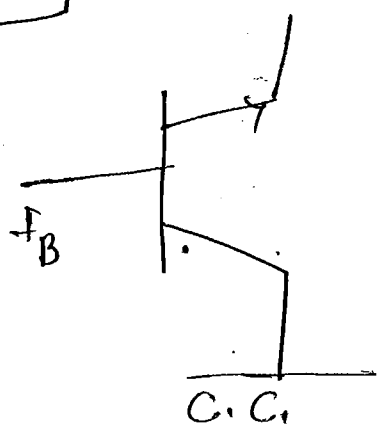




Here γ, β, γ are Current gain.

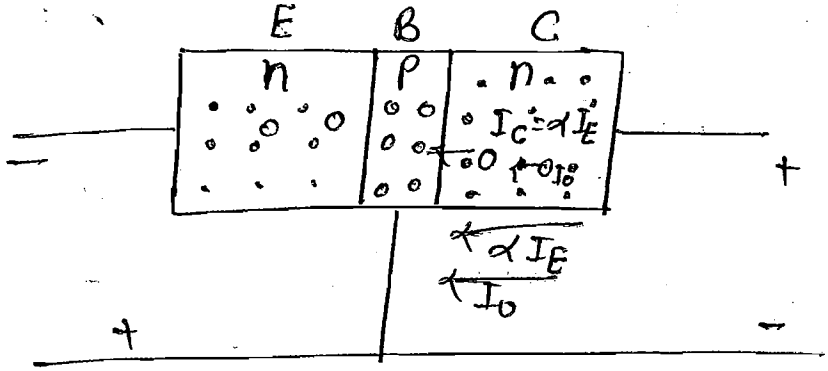


$$\beta = \frac{I_C}{I_B}$$



$$\gamma = \frac{I_E}{I_B}$$

⇒

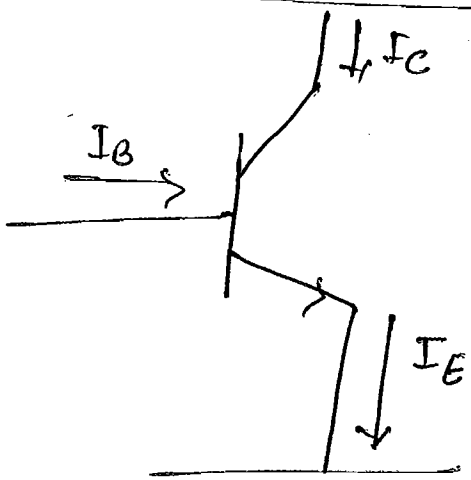


I_o = leakage Current.

$$I_C = \alpha I_E + I_o$$

$$I_C = I_{CO} = I_{CBO} = \alpha I_E + I_o$$

⇒



$$I_E = I_B + I_C \quad \text{— (1)}$$

eqn (1) divide by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\beta = \alpha(1+\beta) = \alpha + \alpha\beta$$

$$\beta - \alpha\beta = \alpha$$

$$\beta(1-\alpha) = \alpha$$

$$\beta = \frac{\alpha}{1-\alpha}$$

⇒ C.B.

$$I_o = \alpha I_E + I_{CO}$$

$$I_C = \alpha(I_B + I_C) + I_{CO}$$

$$(I_C + \alpha I_C) = \alpha I_B + I_C$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{(1-\alpha)} I_B + \frac{I_{CO}}{(1-\alpha)}$$

$$\boxed{I_C = \frac{\alpha}{(1-\alpha)} I_B + (1+\beta) I_{CO}}$$

$\alpha = \beta/1+\beta$

$\frac{\alpha}{\beta} = \frac{1}{1+\beta}$

$\frac{\alpha}{\frac{\alpha}{1+\alpha}} = \frac{1}{1+\beta}$

$1-\alpha = \frac{1}{1+\beta}$

"Common Emitter Configuration is having comparatively more ~~current~~ leakage current w.r. to Common base configuration by $(1+\beta)$ times."

$\underbrace{(1+\beta) I_{CO}}$

$\uparrow$

I_{CBO}

(i) $I_E = I_B + I_C$

(ii) $\alpha = \frac{\beta}{1+\beta}$

(iii)$_{CB}$ $I_C = \alpha I_E + I_O$

(iv)$_{C.C.}$ $I_C = \beta I_B + (1+\beta) I_O$

Q. A Transistor is exited by emmiter current of 10m.A., $\beta = 99$ leakage current $I_{CO} = 10\mu A$ find all other currents.

Soln

$I_C = \alpha I_E + I_{CO}$ $\quad \alpha = \frac{\beta}{1+\beta} = \frac{99}{1+99} = \frac{99}{100}$

$\boxed{\alpha = 0.99}$

So $I_C = 0.99 \times 10mA + 10\mu A$

$= 9.9 mA + 0.01 m.A$

$\boxed{I_C = 9.91 m.A.}$

$\therefore I_E = I_B + I_C$

$\therefore I_B = I_E - I_C$

$= 10\ m.A - 9.91\ m.A$

$$\boxed{I_B = 0.09\ m.A.}$$

Q. A transister is exited by Base current of 20 μ.A. , $\alpha = 0.99$ find all other currents?

Soln Note :- "If Configuration is not mension then assu Commen emitter Configuration."

Soln

$$\beta = \frac{0.99}{1-0.99} = \frac{0.99}{0.01} = 99$$

$$\boxed{\beta = 99}$$

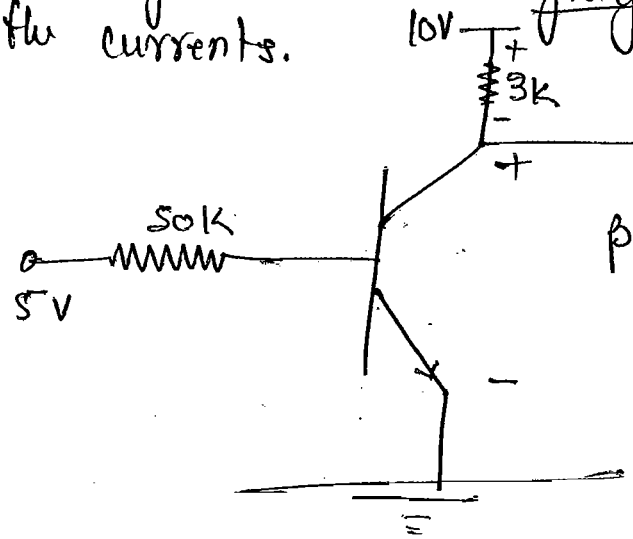
$$I_C = \beta I_B = 99 \times 0.01\ mA$$

$$\boxed{I_C = 1.98\ mA.}$$

$$I_E = I_B + I_C = 20 \times 10^{-3}\ m.A + 1.98\ m.A = 2.\ m.A.$$

$$\boxed{I_E = 2\ m.A.}$$

Q. For the given circuit ~~diag~~ diagram calculate all the currents.



∴ Here leakage current is not given so assum ideally it is 0.

So $I_C = \beta I_B$

$$\boxed{I_C = 100\ I_B} \quad \text{—— (1)}$$

Apply loop current :-

$$-5 + I_B \times 50k + 0.7 = 0$$

$$I_B \times 50k = 5 - 0.7$$

$$I_B = \frac{5 - 0.7}{50}$$

$$\boxed{I_B = 0.086 \text{ mA}}$$

$$I_C = 100 \times 0.08 = 8.6 \text{ m.A.}$$

$$\boxed{I_C = 8.6 \text{ m.A}}$$

$$I_E = I_B + I_C$$

$$= 0.086 + 8.6$$

$$\boxed{I_E = 8.686 \text{ m.A}}$$

Apply loop :-

$$-10 + I_C \times 3k + V_0 = 0$$

$$V_0 = 10 - I_C \times 3k$$

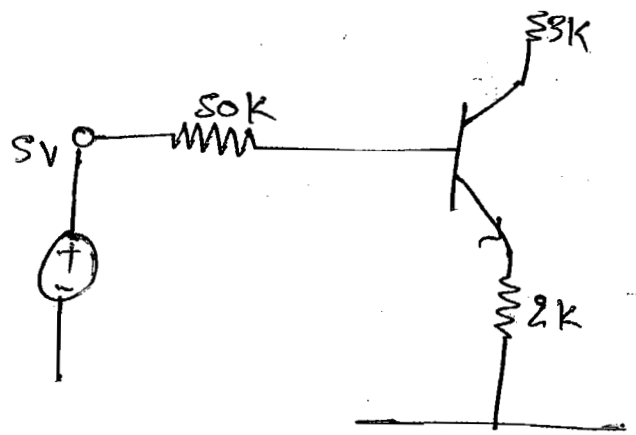
$$= 10 - 8.6 \times 3$$

$$= 10 - 25.8$$

$$\boxed{V_0 = -15.8 \text{ V}}$$

Q. Repeate the previous Ques by replacing emitter by 2kΩ.

Sol:



$I_C = \beta I_B + (1+\beta) I_{C0}$

$\because I_{C0} = 0$

$\therefore \boxed{I_C = \beta I_B}$

$\boxed{I_C = 100 I_B}$

$\because$ eqn fails so apply loop

$-5 + I_B \times 50k + 0.7 + I_E \times 2k = 0$

$I_B \times 50k + (I_B + I_C) \times 2k = 4.3$

$I_B \times 50 + 2I_B + 2 \times 100 I_B = 4.3 \Rightarrow I_B (50 + 2 + 200)$

$I_B = \frac{4.3}{252} = 17.1 \times 10^{-6}$

$\boxed{I_B = 0.017 mA}$

$\because I_C = 100 \times I_B = 100 \times 0.017$

$\boxed{I_C = 1.7 m.A}$

$\because I_E = I_B + I_C$

$I_E = 0.017 + 1.7 = 1.717$

$\boxed{I_E = 1.717 . m.A.}$

Apply loop for V_o :-

$-10 + I_C \times 3 + V_o = 0$

$V_o = 10 - I_C \times 3 = 10 - 1.7 \times 3 = (0 - 5.1)$

$\boxed{V_o = 4.9V}$

$$-10 + I_C \times 3K + V_{CB} + I_E \times 2 = 0$$

$$V_{CE} = 10 + 1.7 \times 3 - 1.717 \times 2$$

$$V_{CE} = 10 + 5.1 - 3.434$$

$$= ~~15.10~~ \; 10 - 8.554$$

$$\boxed{V_{CE} = 1.97V}$$

$V_{CE} - V_{BE} - V_{CB} = 0$

$V_{CB} = V_{CE} - V_{BE}$

$V_{CB} = 1.97 - 0.7$

$\boxed{V_{CB} = 0.77}$

Another loop :-

$V_0 = V_{CE} + I_E \times 2$

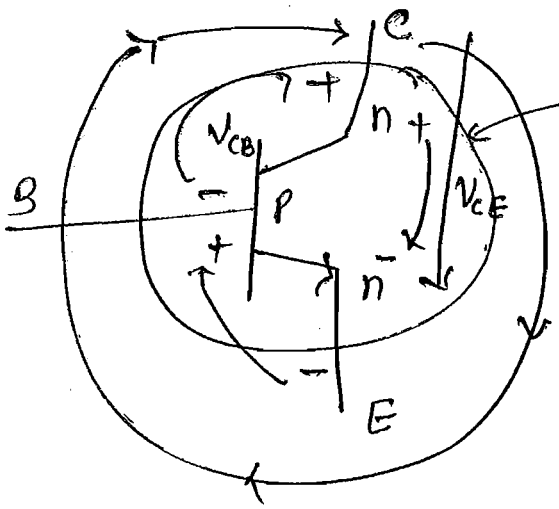
$= 1.4 + 1.717 \times 2$

$= 1.4 + 3.434$

$V_0 = 4.834 \approx 4.9$

$\boxed{V_0 = 4.9 \text{ V}}$

*



Significance of circle around transistor.

$\boxed{+V_{CE} - V_{BE} - V_{CB} = 0}$ Kirchoff's Voltage law.

Q.27

$\alpha = 0.995$, $I_{EB} = 10\,mA.$, $I_{CBO} = 0.5\,mA.$

$I_{CEO} = ?$ $\because I_{CEO} = (1+\beta) I_{CO}$

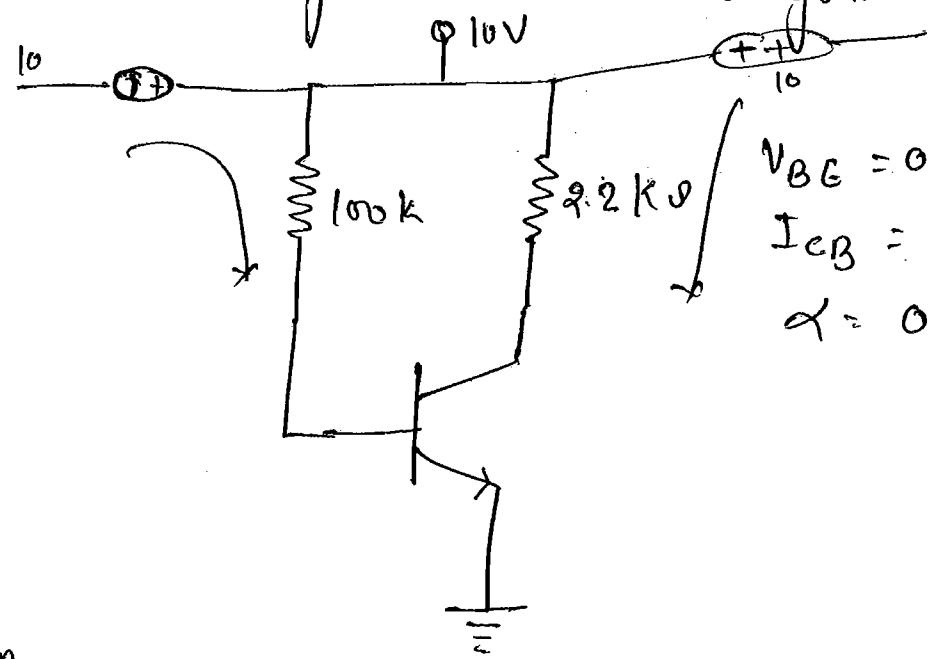
$$\beta = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{0.995}{1-.995} = \frac{0.995}{} = 199$$

$$I_{CEO} = (1+199) I_{CO} = 200 \times 0.5 = 100\,mA$$

$I_{CEO} = 100\,mA$

Q.61 For the given circuit diagram.



Soln

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-96} = \frac{0.96}{0.04} = 24$$

$I_C = \beta I_B + (1+\beta) I_{CBO}$

Applying loop -

$$-10 + I_B \times 100 + V_{BE} = 0$$

$$I_B = \frac{10 - 0.3}{100} = \frac{9.7}{100} = 0.097 \text{ m.A}$$

$$\boxed{I_B = 0.097 \text{ m.A.}}$$

$$I_c = 24 \times 0.097 + 25 \times 0.2$$

$$\boxed{I_C = 2.8 \text{ m.A}}$$

Apply loop by V_c :-

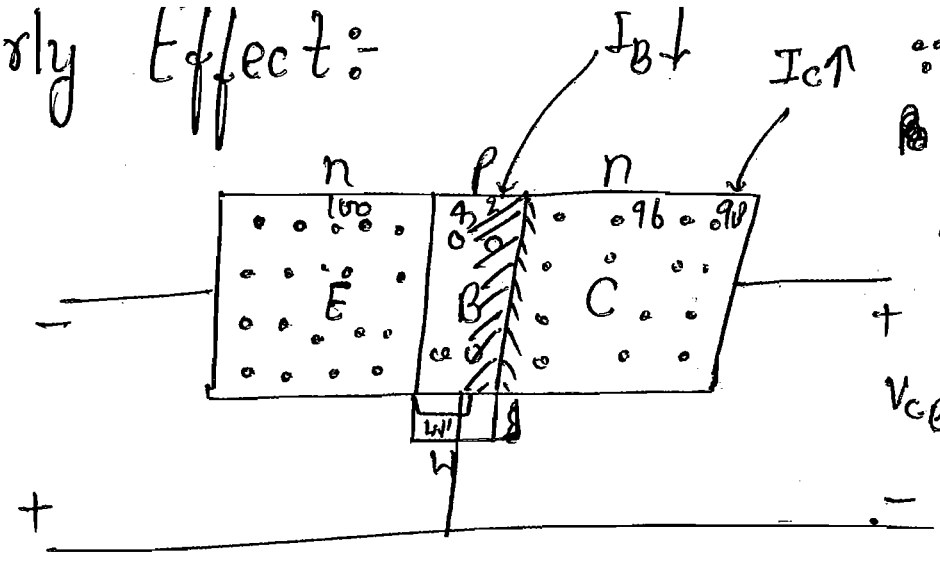
$$-10 + I_c \times 2.2 + V_c = 0$$

$$V_c = 10 - 2.8 \times 2.2$$

$$= 10 - 6.16$$

$$\boxed{V_c = 3.84 \text{ Volt.}}$$

* Early Effect :-



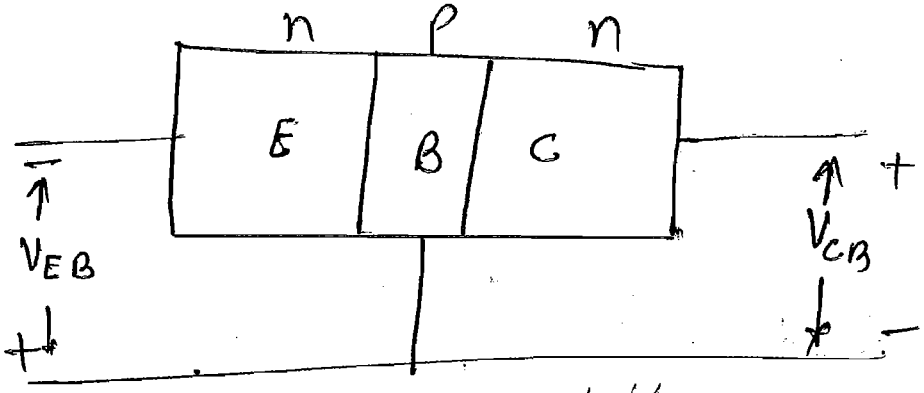
$\because I_C \propto I_E$
So I_E↑

Width of depletion layer is increase when V_{CB} is reverse brase. width is increa more in low doping side.

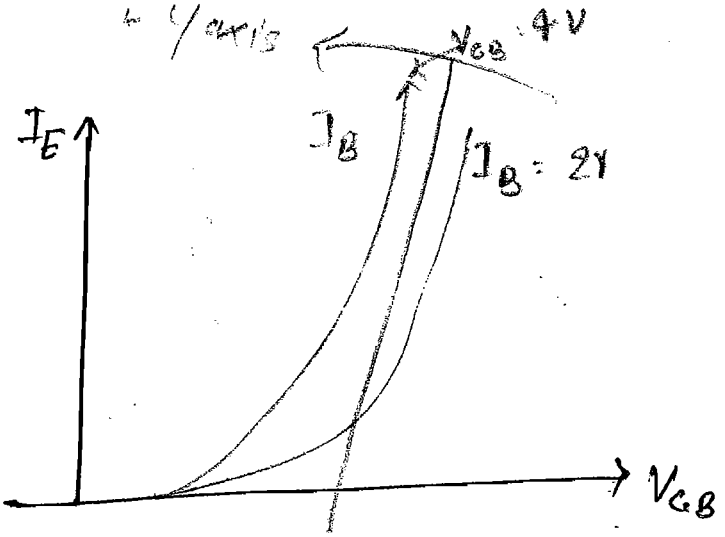
As collector to base voltage varries, effective base width varies is called Base width modulati

As collector to base voltage Changes, ~~dic~~ width of the base decrease so Base Crrent decre So I_C and I_E increases.

* Common Base Configuration :-

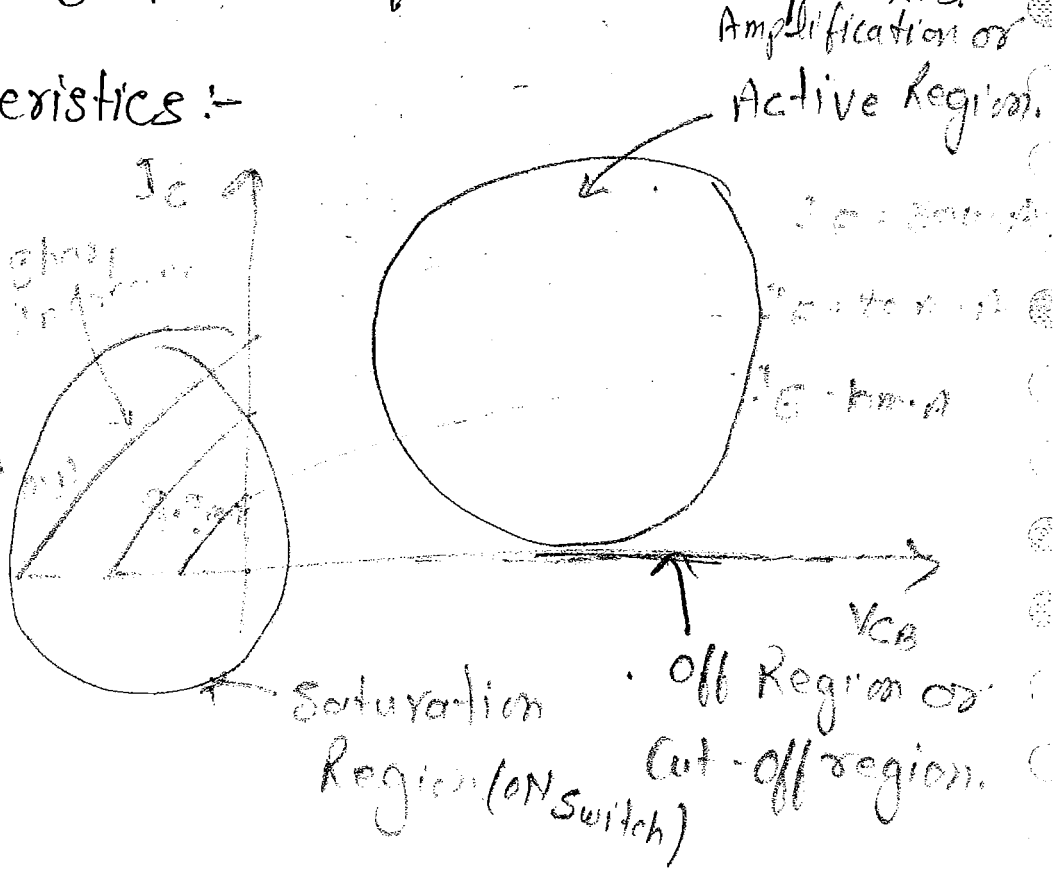


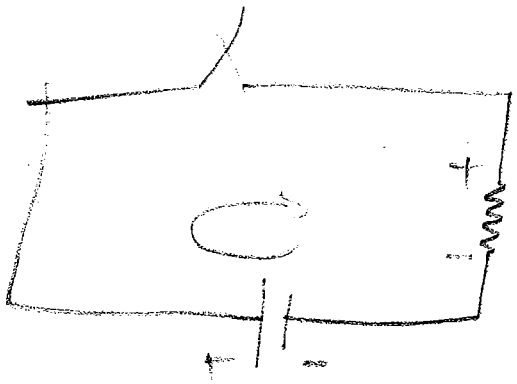
Input Characteristics :-

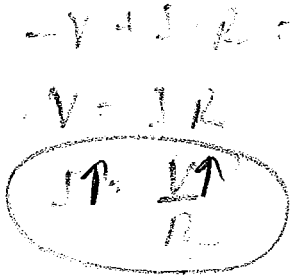


"As V_{CB} increases I_E increas as per Early Effect hence graph shift towards Y-axis."

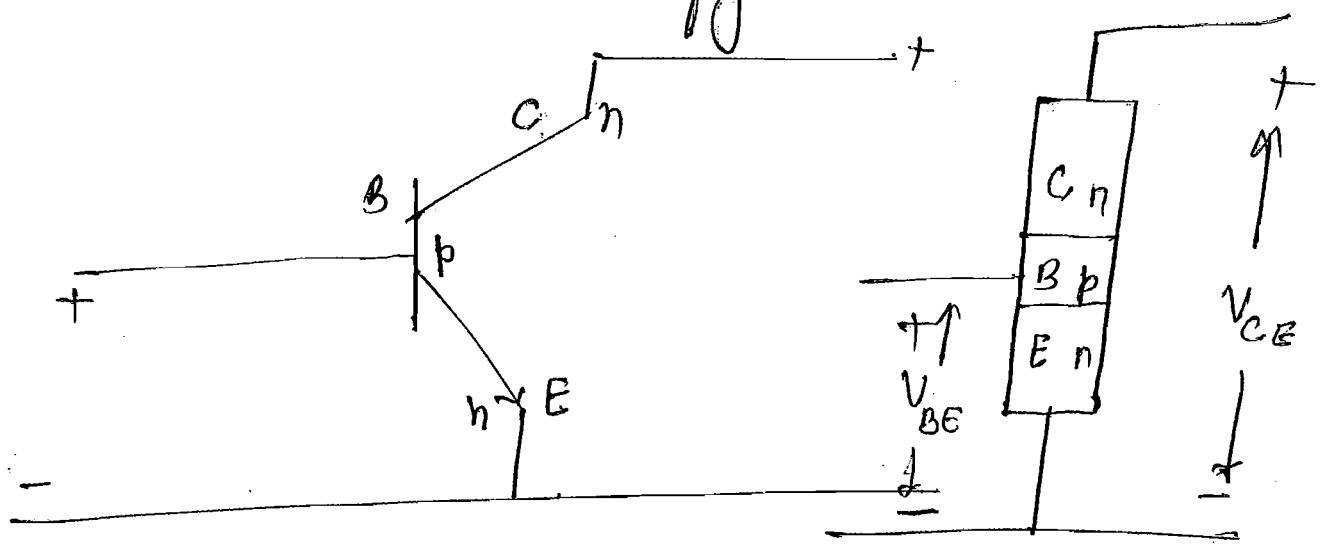
Output Characteristics :-







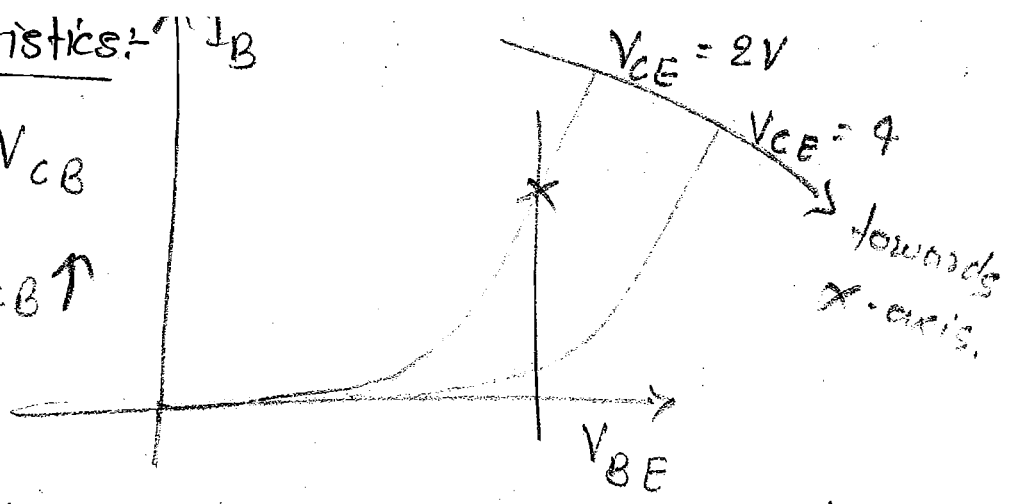
* Common ~~Emitter~~ Emitter Configuration :-



* Input Characteristics :-

$V_{CE} - V_{BE} = V_{CB}$

$V_{CE}\uparrow - 0.7 = V_{CB}\uparrow$



Input characteristics is similar to forward Characteristics of of pn-junction Diode as V_{CB} increases graph shift towards x-axis.

* Output Characteristics :-

$I_C = \beta I_B + (1+\beta) I_{CO}$

Ideally $I_{CO} : 0$

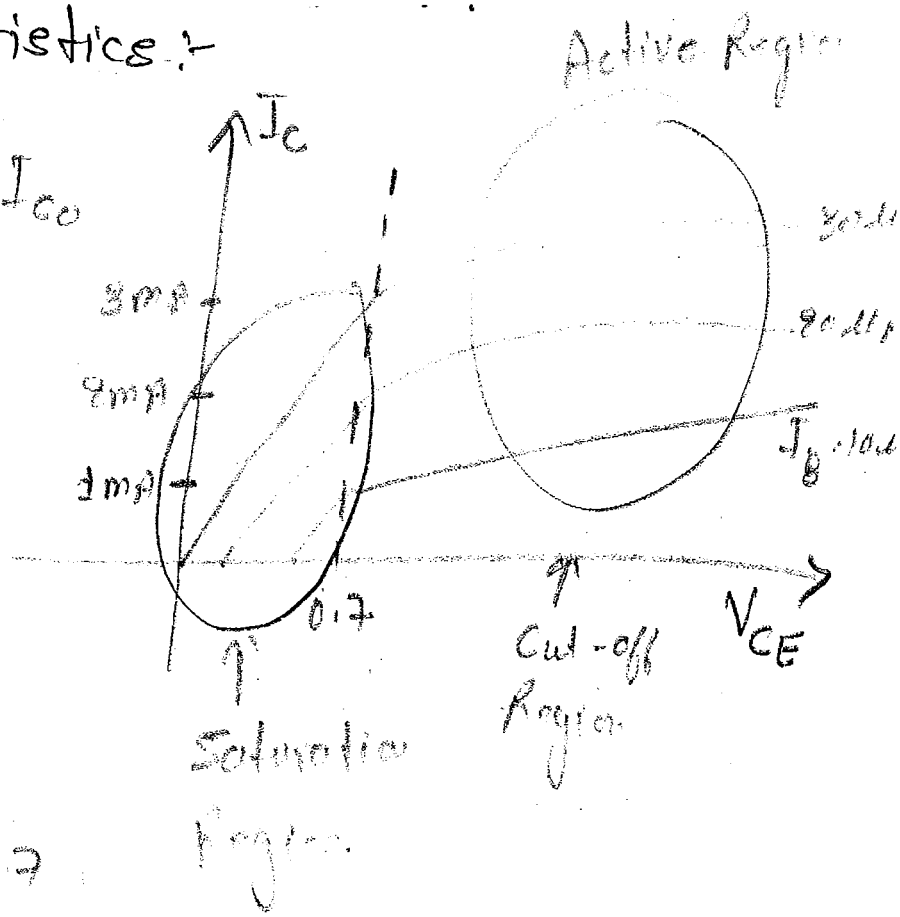
$\beta : 100$

$I_B : 10\mu A$

$I_C : 1mA$

$V_{CE} - 0.7 = V_{CB}$

$\uparrow V_{CE} = \uparrow V_{CB} + 0.7$



$\Rightarrow$ $I_C = \beta I_B$ Relation only applicable for active Region.

* Steps for Determination of Region of Operation :-

Step I :- Assume transistor is operating in Saturation region.

Saturation Voltage	Si	Ge
$V_{BE,sat}$	0.8V	0.3 V
$V_{CE,sat}$.	0.2V	0.1

Step II :- Calculate $I_{B\,sat}$. and $I_{c\,sat}$ Use only loop Analysis { Don't use $I_c = \beta I_B$ }

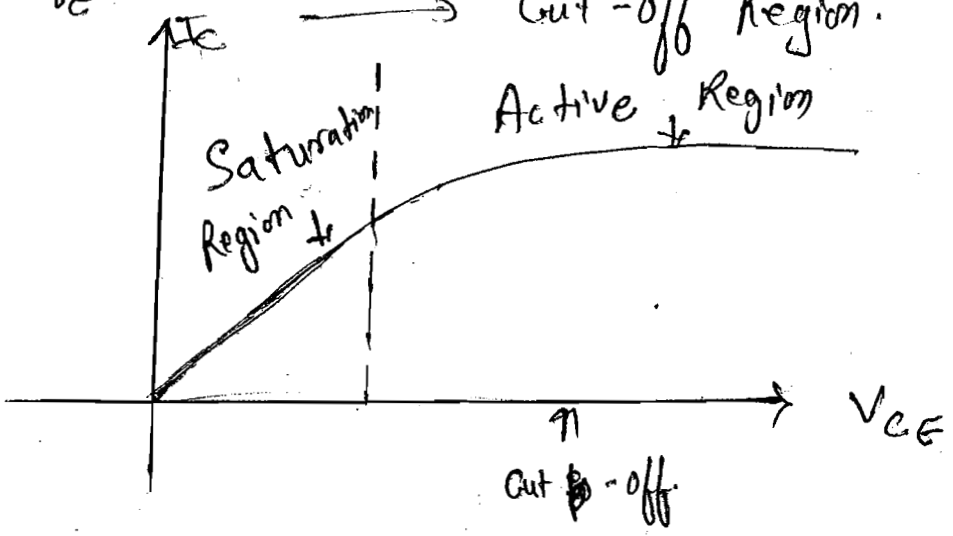
Step III :- Calculate $I_{B,min} = \frac{I_{c\,sat}}{\beta}$

↑ Current in Active Region.

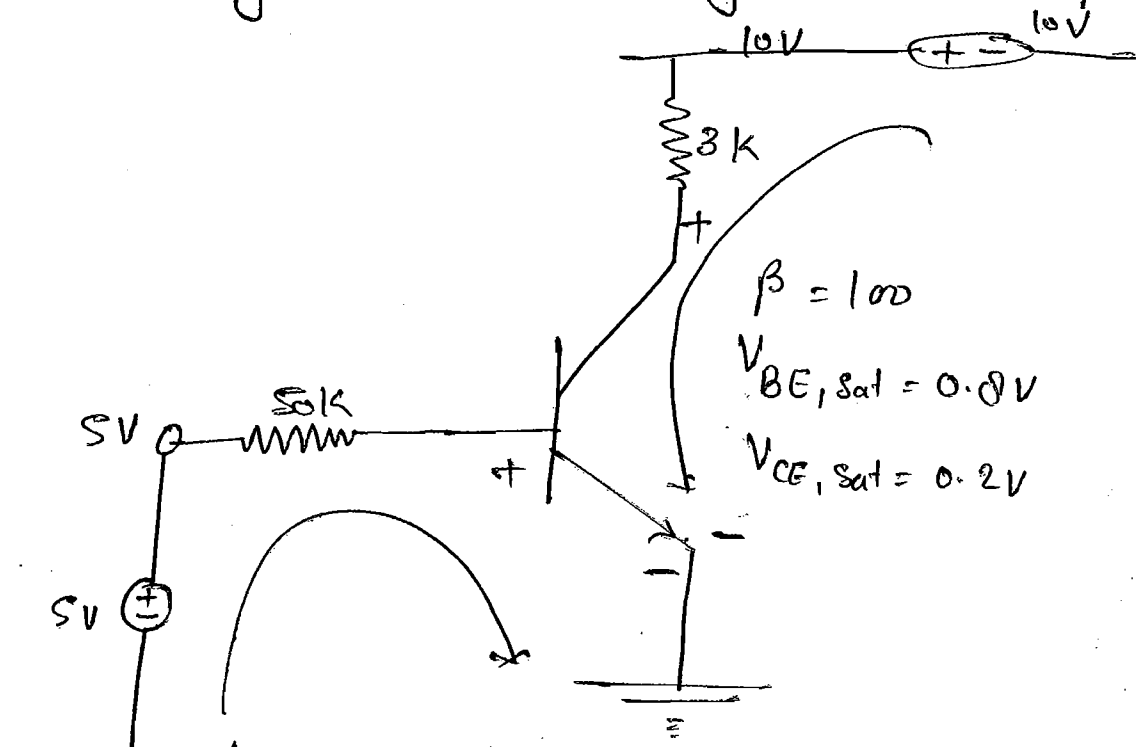
$I_{B,sat} > I_{B,min} \longrightarrow$ Saturation Region

$I_{B,sat} < I_{B,min} \longrightarrow$ Active Region

$I_{B,sat} = -Ve \longrightarrow$ Cut-off Region.



Q. For the given circuit diagram identify the region



Apply loop Analysis :-

$$-5V + I_{B,sat} \times 50k + V_{BE,sat} = 0$$

$$I_{B,sat} \times 50k = 5 - 0.8$$

$$I_{B,sat} = \frac{4.2}{50k} = 0.084mA$$

In Another loop :-

$$-10 + I_{C,sat} \times 3K + V_{CE,sat} = 0$$

$$I_{C,sat} = \frac{9.8}{3}$$

$$= 3.26 m.A.$$

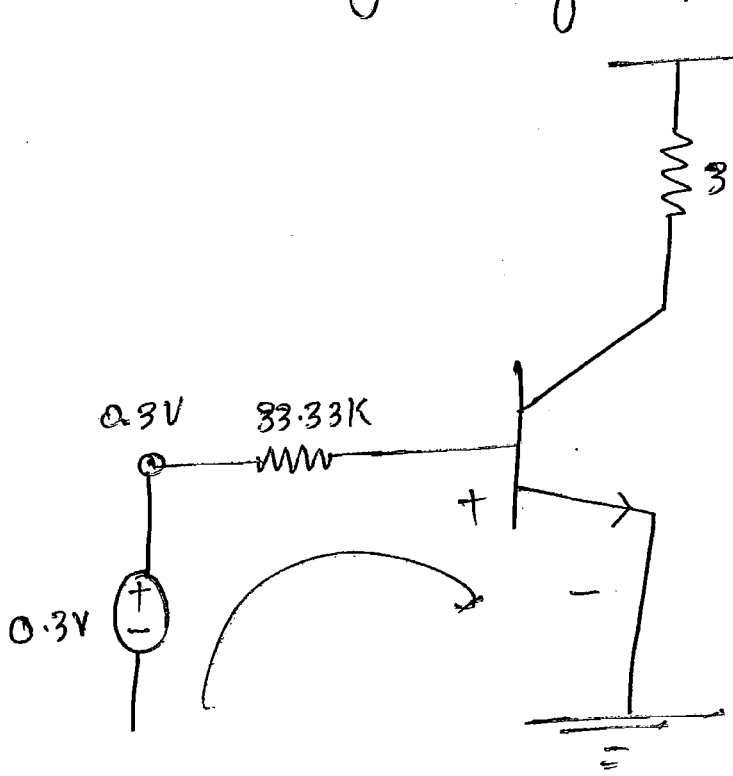
$$I_{\beta,min} = \frac{I_{C,sat}}{\beta} = \frac{3.26m.A}{100}$$

$$I_{\beta min} = 0.0326mA.$$

$$I_{\beta,sat} > I_{\beta min}$$

$0.08 > 0.03$ So it is in saturation Region.

Q. Find the region of operation of given transistor.



$V_{BE,sat} = 0.8V$

$V_{CE\,sat} = 0.2V$

$\beta = 100$

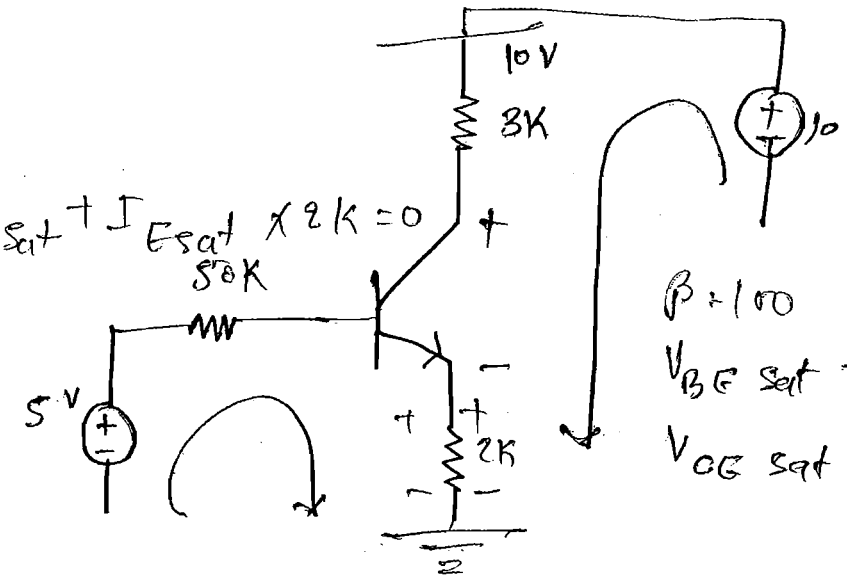
$$-0.3V + I_{B,sat} \times 33.33 + V_{BE,sat} = 0$$

$$I_B \times 33.33 = -0.8 + 0.3\,V$$

$$I_B = \frac{-0.5}{33.33} = -0.015001S$$

I_B = -ve So cut-off Region.

Q. for the given circuit diagram determine region.



$-5 + V_{Bsat} \times 50 + V_{BE\,sat} + I_{E\,sat} \times 2K = 0$

$\beta = 100$

$V_{BE\,sat} = 0.8V$

$V_{CE\,sat} = 0.2V$

$$-5 + I_{B\,sat} \times 50K + 0.8 + [I_{B\,sat} + I_{C\,sat}]\,2K = 0$$

$$-5 + I_{B\,sat} \times 50K + 0.8 + [I_{sat} + I_{C\,sat}]\,2K = 0 \quad \text{(II)}$$

$$I_{B\,sat} \times 52K + I_{C\,sat} \times 2K = 4.2 \quad \text{(I)} \times 5$$

$$-10 + I_{C\,sat} \times 3K + V_{CE\,sat} + I_{E\,sat} \times 2K = 0$$

$$-10 + I_{C\,sat} \times 3K + 0.2 + [I_{C\,sat} + I_{B\,sat}]\,2K = 0$$

$$I_{B\,sat} \times 2K + I_{E\,sat}\, 5K = 9.8 \quad \text{(II)} \times 2$$

$$I_{B\,sat} \cdot 260K + I_{C\,sat}\, 10K = 21 \quad \text{(III)}$$

$$I_{B\,sat} \times 9K + I_{C\,sat}\, 10K = 19.6 \quad \text{(IV)}$$

$$I_{B\,sat} \times 256K = 9.4$$

$$I_{B\,sat} = \frac{9.4}{256K}$$

$$\boxed{I_{B\,sat} = 0.0093\,mA}$$

~~So $I_{C\,sat}$ =~~

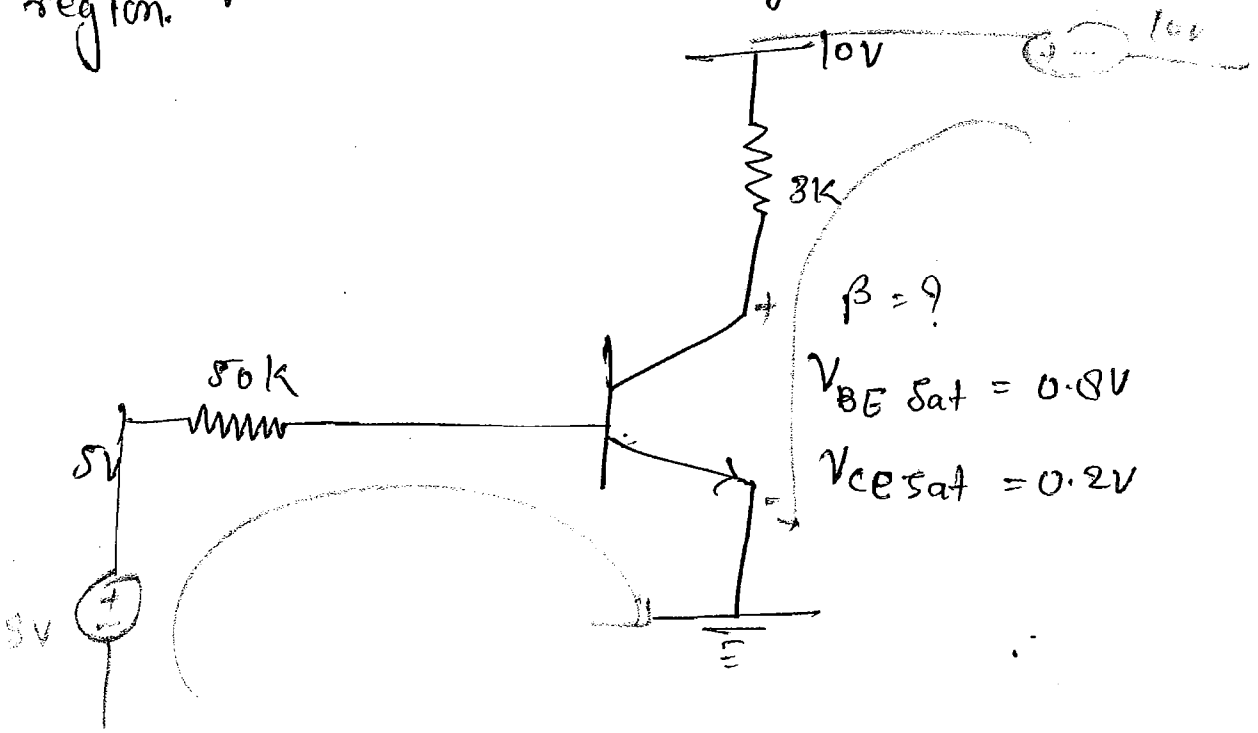
from eqn (III) :-

$$0.0093 \times 260K + I_{C.sat} \times 10K = 21$$

$$I_{C\,sat} = \frac{21 - 2.418}{10} = \frac{18.582}{10}$$

$$\boxed{I_{C\,sat} = 1.8582\,mA}$$

Q. Assume transistor is operating in saturation region find the minimum value of β.? so that circuit produces stable operation in saturation region.



$$I_B = \frac{5 - 0.8}{50K}$$

$$= \frac{4.2}{50K}$$

$$\boxed{I_{B_{sat}} = 0.084\,mA}$$

$$I_{C\,sat} = \frac{10 - 0.2}{3K} = 3.33\,mA$$

$$\boxed{I_{C\,sat} = 3.33\,mA}$$

$$I_{B\,min} = \frac{I_{C\,sat}}{\beta} = \frac{3.33\,mA}{\beta}$$

for 0.084_{mA} $\quad \frac{3.33\,mA}{\beta} \Rightarrow \beta > 39$

$$\boxed{\beta > 40}$$

Q. Repeat the previous Question as $\beta = 100$ Calculate ~~$I_{C\,sat}$~~ ~~$I_{B\,min}$~~ & R_C ?

Soln

$$I_{B,sat} = 0.084\,mA$$

$$-10 + I_{C\,sat} \cdot R_C + 0.2V = 0$$

$$-10 + I_{C\,sat} \times R_C + 0.2V = 0$$

$$-10 + I_{C\,sat} \times R_C + 0.2V = 0$$

$$I_{C\,sat} = \frac{10 - 0.2}{R_C} = \frac{9.8}{R_C}$$

$$I_{C\,sat} = 3.266$$

$$I_{B\,min} = \frac{I_{C\,sat}}{\beta}$$

Condition of saturation -

$$I_{B\,sat} > I_{B\,min}$$

$$0.084\,m.A. > I_{B\,min}$$

$$\because I_{B\,min} = \frac{I_{C\,sat}}{\beta}$$

$$I_{B\,min} = \frac{9.8}{R_C \times 100}$$

$\because$ Condition of saturation

$$I_{B\,sat} > I_{B\,min}$$

$$0.084\,m.A > \frac{9.8}{R_C \times 100}$$

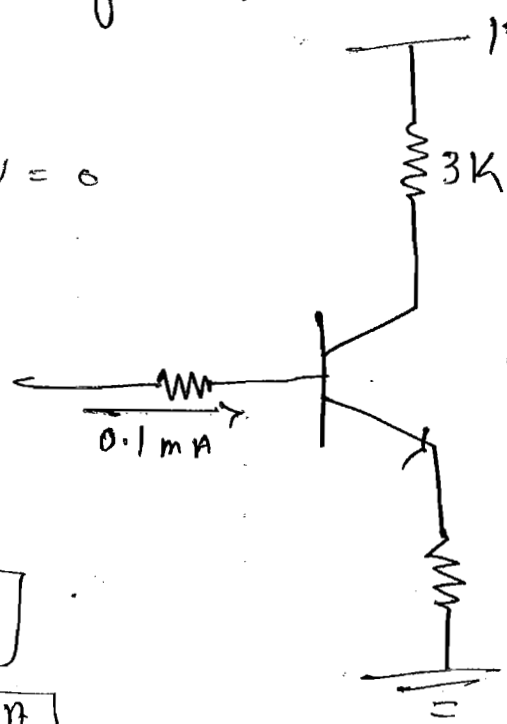
$$R_C > \frac{9.8}{0.084 \times 100}$$

$$R_C > \frac{9.8}{8.4}$$

$$\boxed{R_C > 1.1\,\Omega}$$ Ans

Q. Assume circuit is operating in saturation region determine the value of β for stable operations.

Soln



$$I_{CE\,sat} = 0.2V$$

$$V_{BE\,sat} = 0.8V$$

$\beta = ?$

$$-12 + I_C \times 3K + 0.2V = 0$$

$$I_C = \frac{12 - 0.2}{3}$$

$$= \frac{11.8}{3K}$$

$$\boxed{I_C = 3.93\,m.A}$$

given $\boxed{I_{B\,sat} = 0.1\,m.A}$

$$I_{B\,min} = \frac{I_{C\,sat}}{\beta} = \frac{3.93\,mA}{\beta}$$

Condition of saturation

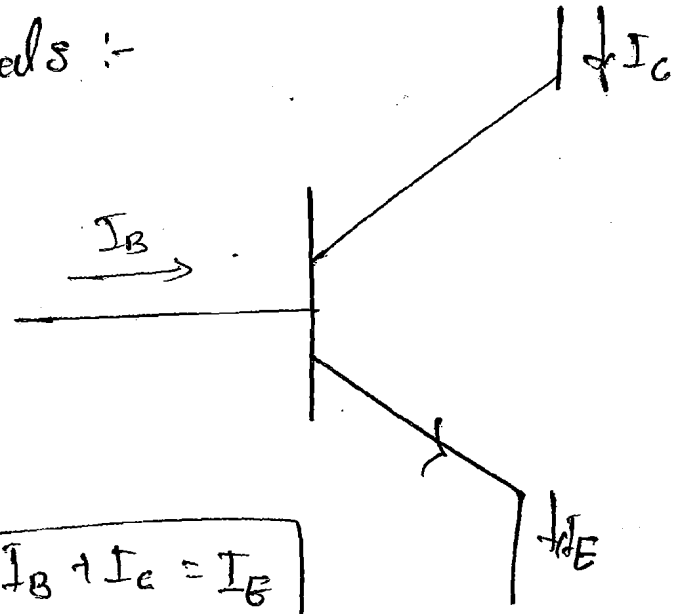
$$I_{B\,sat} > I_{B\,min}$$

$$0.1\ mA > \frac{3.9\ mA}{\beta}$$

$$\boxed{\beta > 39}$$

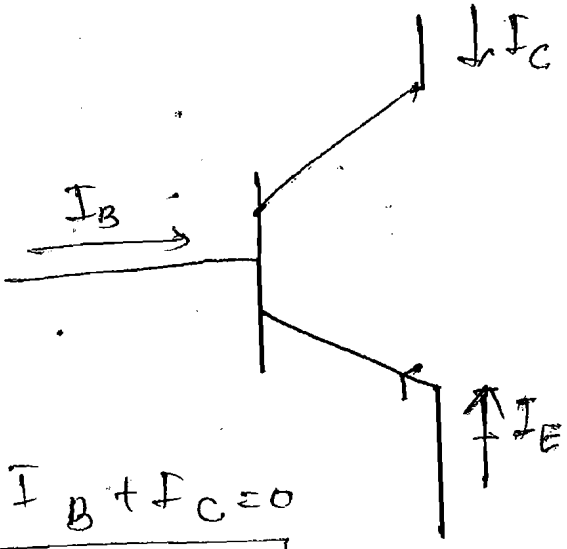
Fundamentals :-

n-p-n



$$\boxed{I_B + I_C = I_E}$$

p-n-p :-

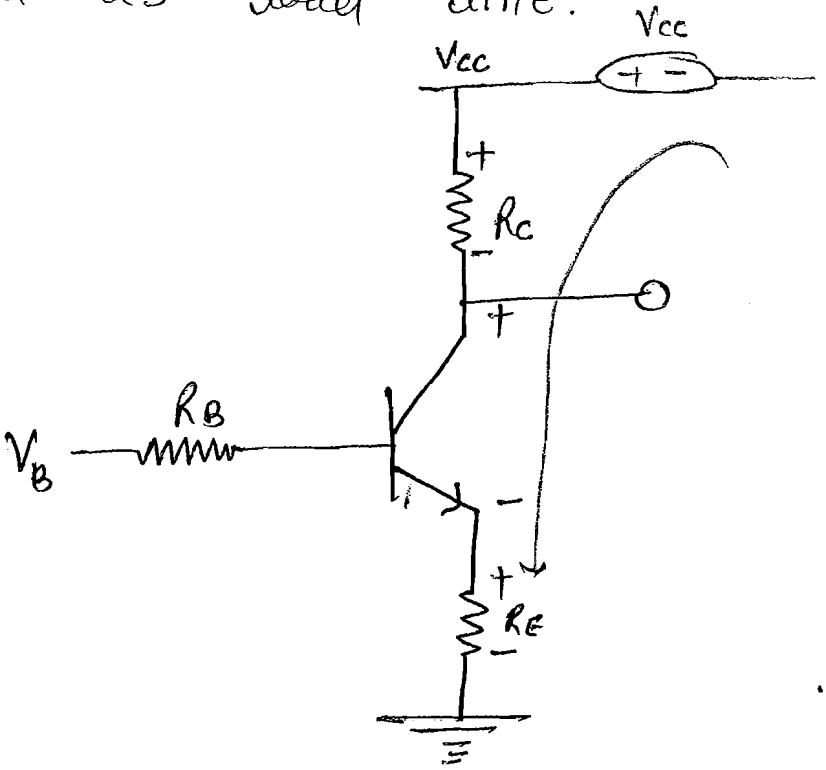


$$I_E + I_B + I_C = 0$$

$$\boxed{I_E = -(I_B + I_C)}$$

Load Line :-

A line drawn on the output characteristics is called as "load line".



Note :-

For Larger value of β, $I_E = I_C$ and $I_B = 0$

$$I_E = I_B + I_C$$

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta}$$

$$I_C = I_c \left[\frac{1}{\beta} + 1\right]$$

$$I_E = I_c \left[1 + 0\right]$$

$$\boxed{I_E = I_C}$$

$\frac{1}{\beta} \approx 0$ when $\beta >>>$ large

So $\boxed{I_C = I_E}$

Applying the loop :-

$$-V_{cc} + I_C R_C + V_{CE} + I_E R_E = 0$$

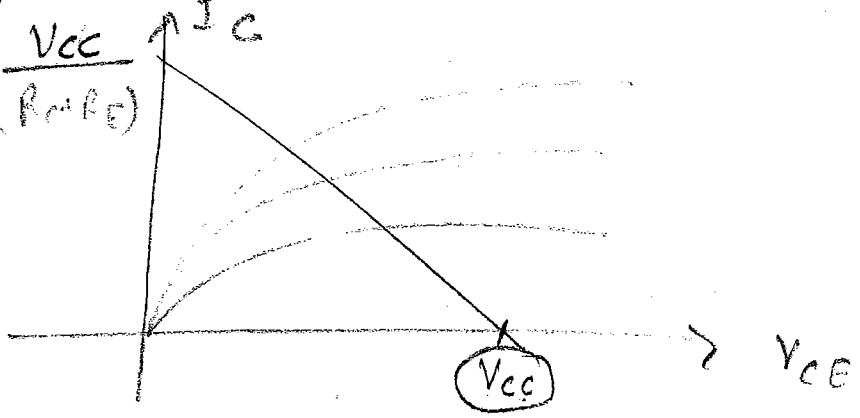
$$-V_{cc} + I_C \times R_C + V_{CE} + I_C \times R_E = 0$$

$$I_C (R_C + R_E) = -V_{CE} + V_{cc}$$

$$\boxed{I_c = \frac{-V_{CE}}{(R_C + R_E)} + \frac{V_{cc}}{(R_C + R_E)}}$$ like $y = mx + c$ eqn of line.

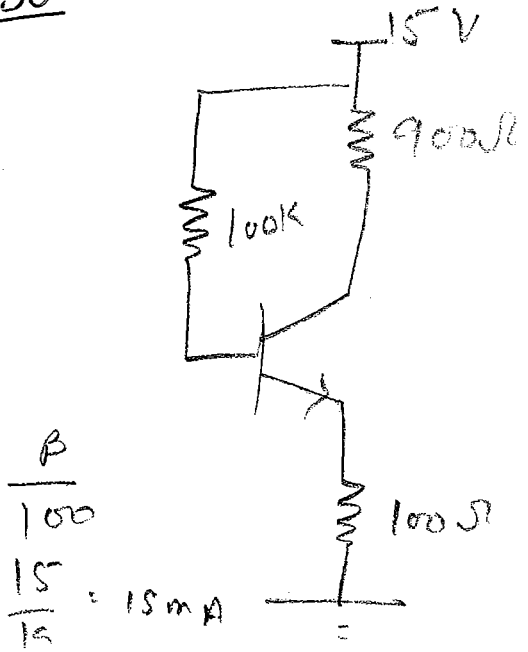
If $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C + R_E}$

modification when $R_E = 0$: $\frac{V_{CC}}{R_C}$ / $\frac{V_{CC}}{(R_C + R_E)}$



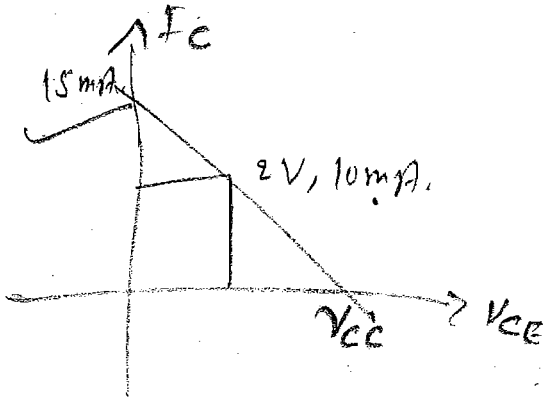
B.A.

Q.38



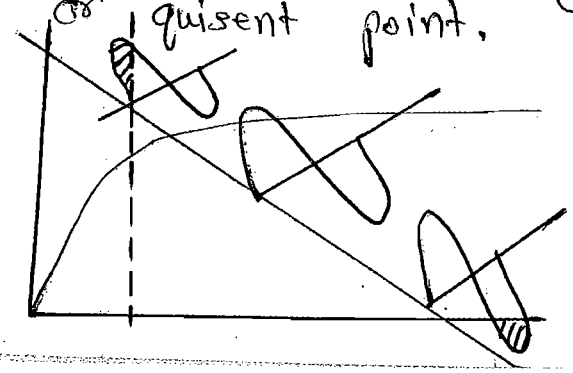
$\frac{\beta}{100}$

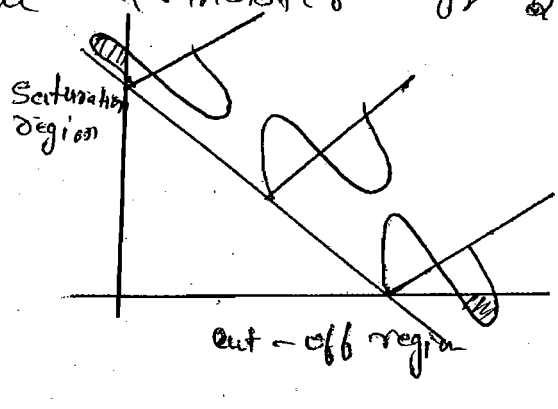
$\frac{15}{I_B} : 15mA$



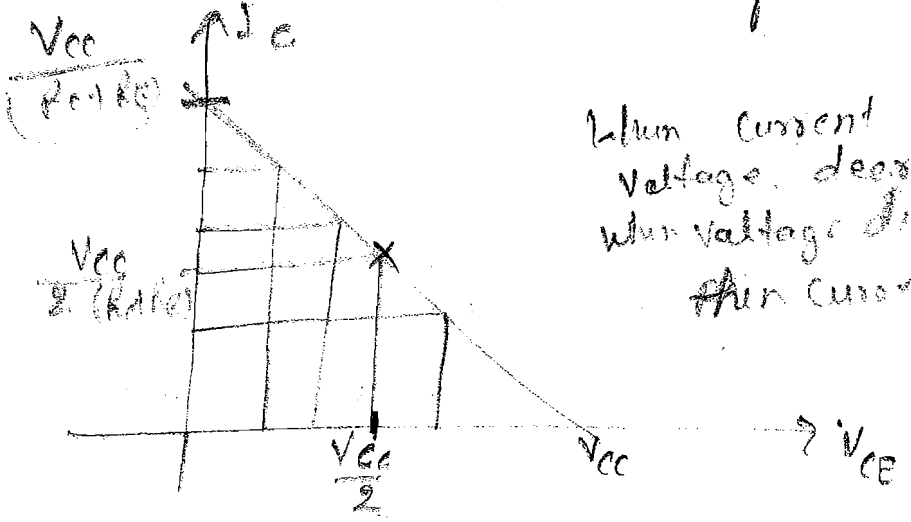
* Q - Poin :-

A point selected on load line corresponding to that a fixed voltage and fixed current at which transistor operates is called as operating point of the transistor or Q-point or quisent point.

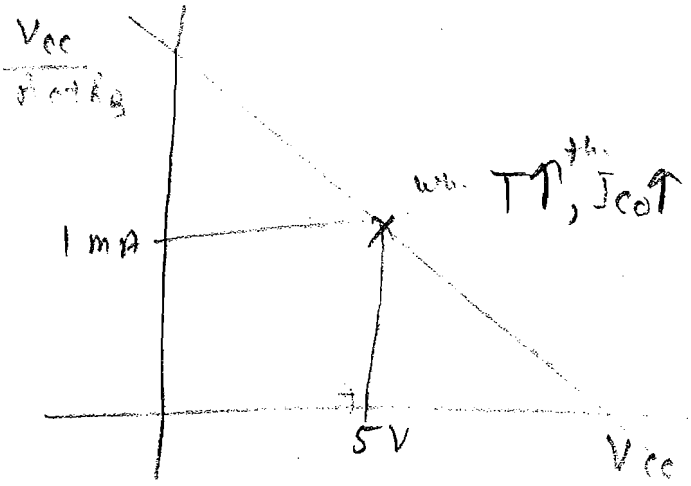




If the operating point selected near saturation region or near cut-off region. then the upper portion of the wave form will be in saturation or cut off where proper amplification is not found. Hence operating point selected approximately mid of the active region.



When current increases - voltage decreases when voltage decreases then current decreases.



$I_C = \beta I_B + (1+\beta) I_{CO}$

with $T°$, I_{CO} with temp increases

$I_C \uparrow = \beta I_B + (1+\beta) I_{CO} \uparrow$

(i) β mismatch

(ii) material mismatch. Ge, Si

(i) Once the operating point selecting at the center it does not gaurantees that it will remain at the center. it can change because of changes in temp (I_{CO} changes) hence I_C changes. given by the expression.

$$\boxed{I_C = \beta I_B + (1+\beta) I_{CO}}$$

(ii) Replacement of transistor :- β mismatch

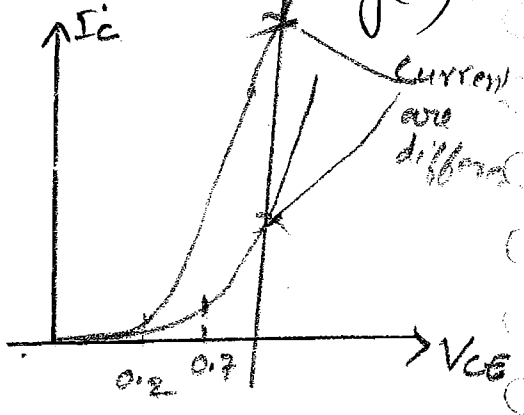
(iii) Replacement of transistor :- Mismatch of material turn cut in voltage changes.

* Stability factor :- It is defined as a factor by how much collector current changes due to change in (I_{CO} , β , Base-Emitter Voltage.).

$$S = S_I = \frac{\Delta I_C}{\Delta I_{CO}} \text{ or } \frac{\partial I_C}{\partial I_{CO}}$$

$$S = S_\beta = \frac{\Delta I_C}{\Delta \beta} \text{ or } \frac{\partial I_C}{\partial \beta}$$

$$S = S_V = \frac{\Delta I_C}{\Delta V_{BE}} \text{ or } \frac{\partial I_C}{\partial V_{BE}}$$



"Ideal value of stability factor must be minimum (≈ 0)."

$$I_C = \beta I_B + (1+\beta) I_{CO} \quad \text{—①}$$

differentiate w.r.to. I_C

$$\frac{\partial I_C}{\partial I_C} = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$(1+\beta) \frac{\partial I_{CO}}{\partial I_C} = 1 - \beta \frac{\partial I_B}{\partial I_C}$$

$$\frac{\partial I_{C0}}{\partial I_C} = \frac{(1-\beta)\frac{\partial+\beta}{\partial I_C}}{(1+\beta)}$$

$$\boxed{\frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{(1-\beta)\frac{\partial I_B}{\partial I_C}}}$$

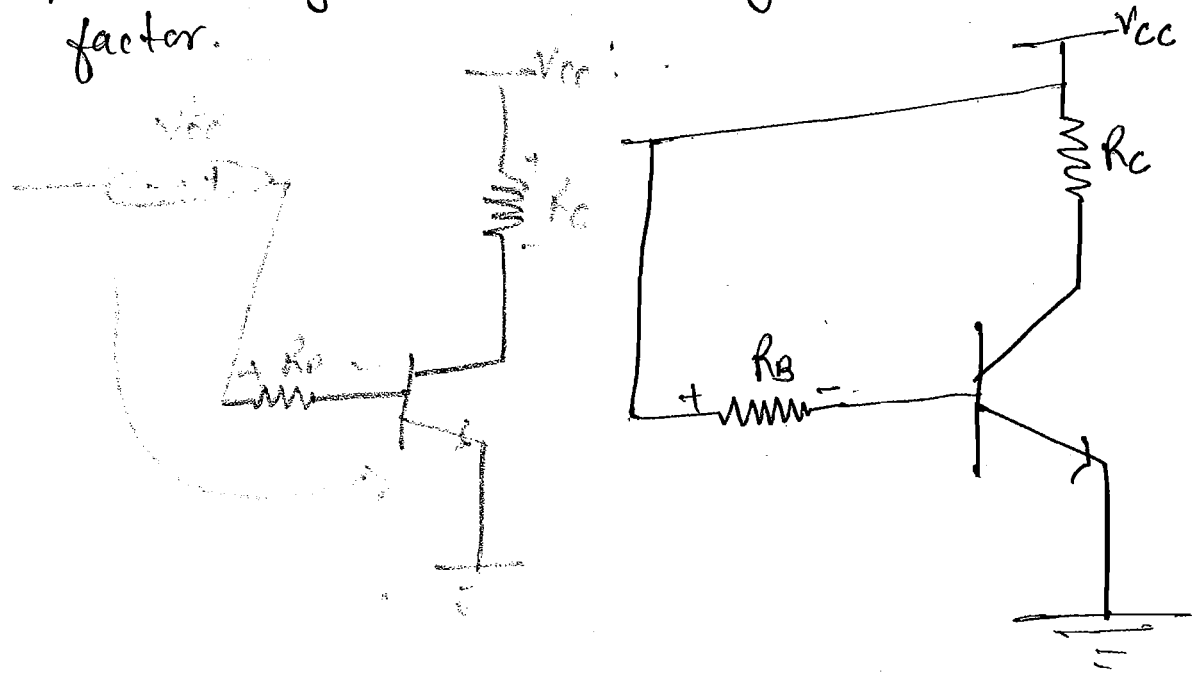
* Steps for calculating stability factor :-

(i) Apply loop including input terminal

(ii) Calculate I_B

(iii) find $\frac{\partial I_B}{\partial I_C}$

Q. For the given circuit diagram determine stability factor.



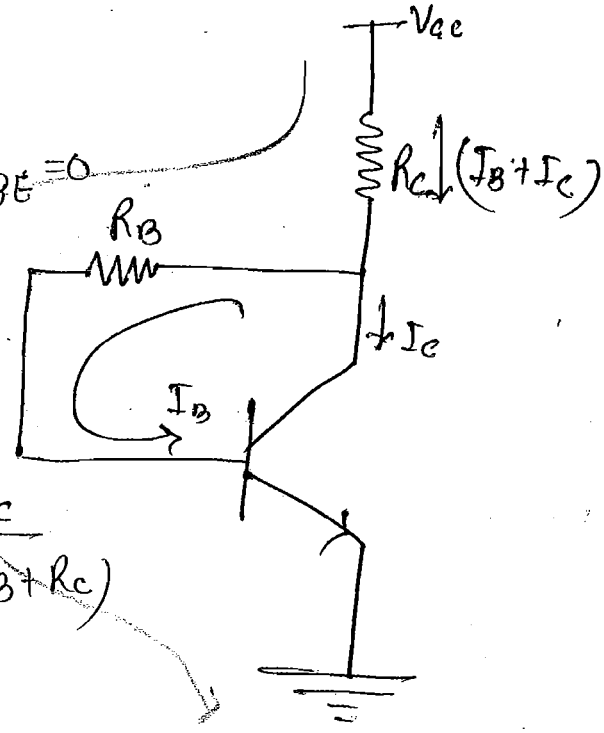
$$-V_{CC} + I_C \times R_C + V_{BE} = 0$$

$$\frac{\partial I_B}{\partial I_C} = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

$$S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}} = 1+\beta$$

Q Determine circuit factor



$$-V_{CC} + (I_C + I_B)R_C + I_B R_B + V_{BE} = 0$$

$$I_B(R_B + R_C) = V_{CC} - V_{BE} - I_C R_C$$

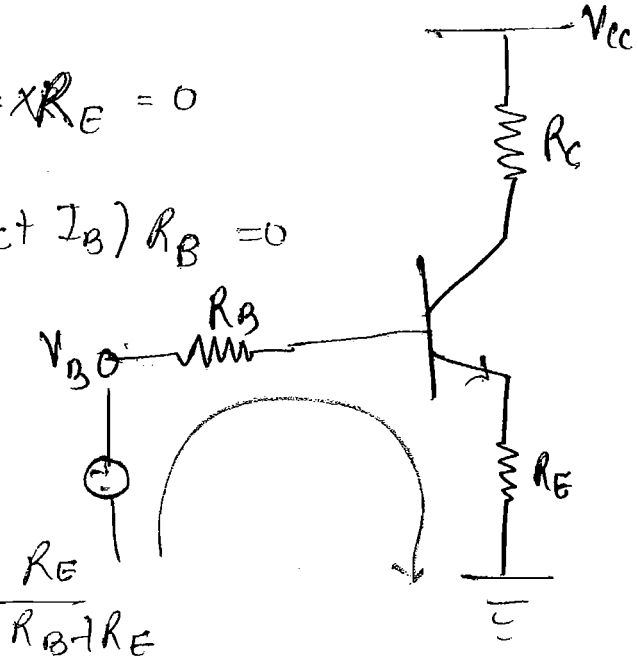
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C} - I_C \times \frac{R_C}{(R_B + R_C)}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C + R_B}$$

$$S = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_C+R_B}\right)}$$

So $$S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}}$$

Q. find stability factor.



$$-V_B + I_B \times R_B + V_{BE} + I_E \times R_E = 0$$

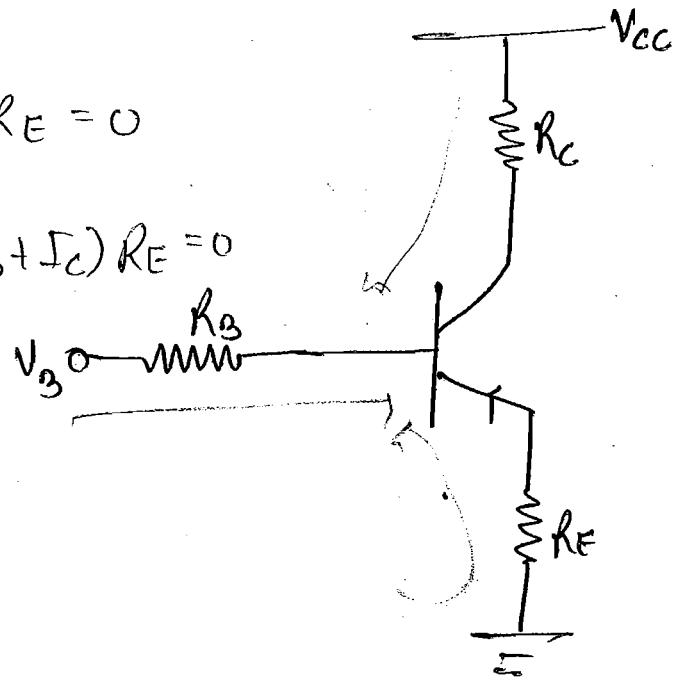
$$-V_B + I_B R_B + V_{BE} + (I_C + I_B)R_B = 0$$

$$I_B(R_B + R_E) = V_B - V_{BE} - I_C R_B$$

$$I_B = \frac{V_B - V_{BE}}{R_B + R_E} - \frac{I_C R_E}{R_B + R_E}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \Rightarrow \boxed{S = \frac{1+\beta}{1+\beta \frac{R_E}{(R_B+R_E)}}}$$

Q.



$$-V_B + I_B R_B + V_{BE} - I_E R_E = 0$$

$$-V_B + I_B R_B + V_{BE} + (I_B + I_C) R_E = 0$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$\boxed{S = \frac{1+\beta}{1+\beta \frac{R_E}{(R_B+R_E)}}}$$

* **Stabilizing Circuit:-** To fix the operating point at the center the circuit used are called as stabilizing circuit.

Stabilizing Circuit

- Compansating circuit (logic)
- Biasing circuit (mathematics)

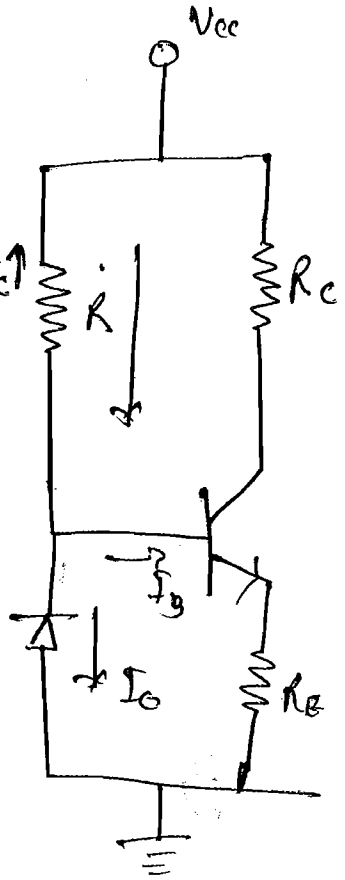
Compansating circuit are operates on logic function.

(2) Baising Circuit :-

Totally baised on mathematical operation.

in PSU's

* DIODE COMPANSATION :-



When temp increases then -

$T\uparrow \; I_{CO}\uparrow \; I_C\uparrow \; = I_C = \beta I_B\downarrow + (1+\beta) I_C\uparrow$

$I = I_B\downarrow + I_C\uparrow$

Increase in I_{CO} and decrease in I_C cancels their effect. Hence I_C stable.

* "Sensistor" / Compansating Circuit :-

$T\uparrow \; R_s\uparrow \; \sigma\downarrow$ (Positive Temp. Coefficient) (like metals)

$T\uparrow \; R_s\downarrow$ (Negative Temperature Coefficient)

$T\uparrow \; I_o \uparrow \; I_e \uparrow$

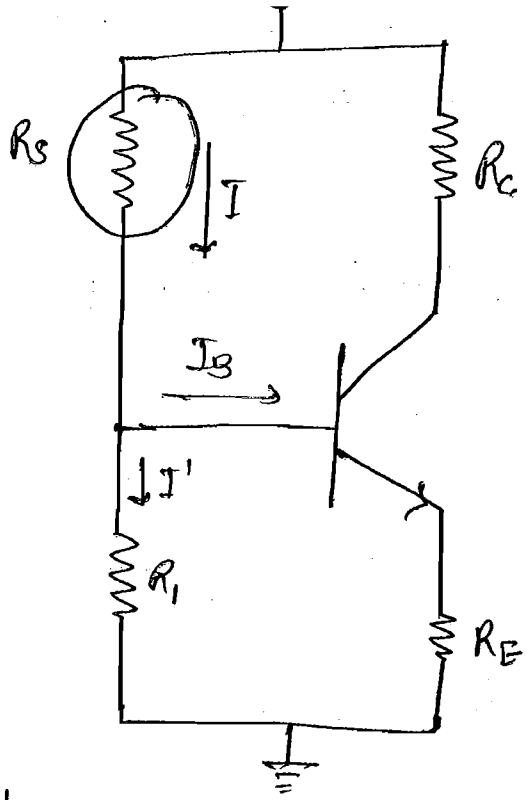
$\Rightarrow I_C = \beta I_B + (1+\beta) I_{CO}$

$I_B = I_B + I'$

Simultaniously

$T\uparrow \; R_S \uparrow \; I_S \downarrow$

$\therefore I_S = I_B + I'$



when I_S decreases, I_B also decreases.

I_{CO} ↑ an I_B ↓ so effect cancel out.

V.Imp.

* Biasing Circuits:-

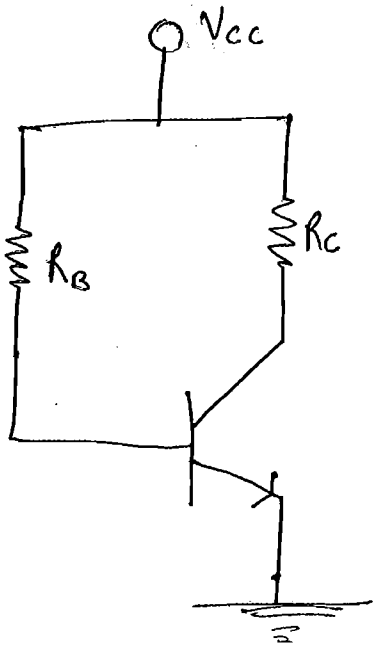
(i) fixed Biased Circuit

(ii) Collector to base bias circuit

(iii) Self Bias / Voltage divider bias / Potential divider bias

(1) fixed Biased Circuit:-

$S = 1+\beta$ → stability factor very high. So non practical circuit



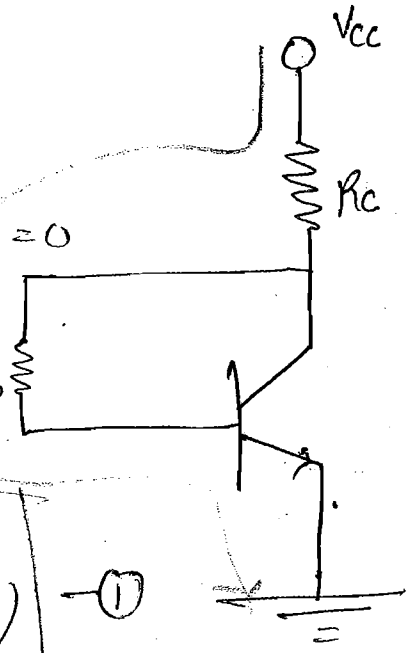
$-V_{CC} + I_B R_B + V_{BE} = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R}$$

$\therefore$ the value of I_B is fixed so it called fixed bias circuit.

There is no provision to decrease I_B, so stability factor is high. So practically not used.

(2) Collector to Base bias Circuit:-



Applying input loop -

$$-V_{CC} + (I_B + I_C)R_C + I_B R_B + V_{BE} = 0$$

$$I_B (I_B + R_C) = V_{CC} - V_{BE} - I_C R_C R_B$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{(I_B + R_C)} - \frac{I_C R_C}{(R_B + R_C)}} \quad \text{--- (1)}$$

(fixed) (fixed)

$$S = \frac{1+\beta}{\left(1+\frac{\beta R_C}{R_B + R_C}\right)}$$

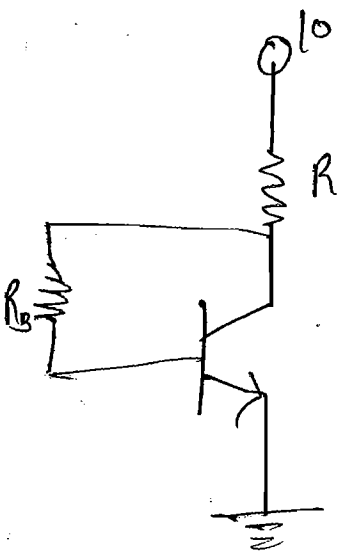
When T ↑, I_{CO} ↑ hence I_C ↑

giving $I_C = \beta I_B + (1+\beta) I_{CO}$

I_B is decreases by eqn (1)

Hence effect cancel out.

Q.



$V_{BE} = 0.7V$

$\beta = 100$

$S = 10$

$R_B = ?$

$$\because S = \frac{1+\beta}{1+\beta\frac{R_C}{R_B + R_C}}$$

$$10 = \frac{1+100}{1+\frac{100 \times 3}{R_B + 3}}$$

$$10 = \frac{101}{(R_B+3)+300}(R_B+3)$$

$$10\{(R_B+3)+300\} = 101(R_B+3)$$

$$10R_B + 30 + 3000 = 101R_B + 303$$

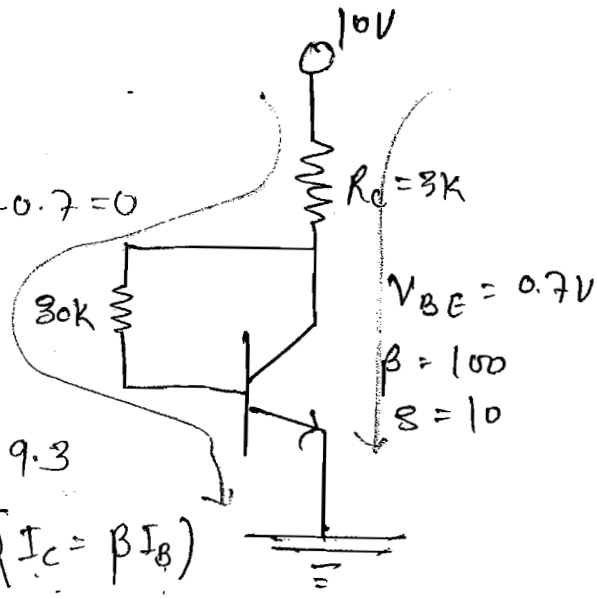
$$101R_B - 10R_B = -303 + 30 + 3000$$

$$R_B(91) = 2727$$

$$R_B = \frac{2727}{91} = 29.967$$

$$\boxed{R_B \approx 30k}$$

Q.



$$-10 + (I_B + I_C)3K + I_B \times 30K + 0.7 = 0$$

$$I_B \times 33K + I_C \times 3K = 9.3$$

$$I_B \times 33K + \beta I_B \times 300K = 9.3$$

$$\{I_C = \beta I_B\}$$

$$I_B = \frac{9.3}{333K} = 0.02$$

$$I_C = \beta \times 0.02$$

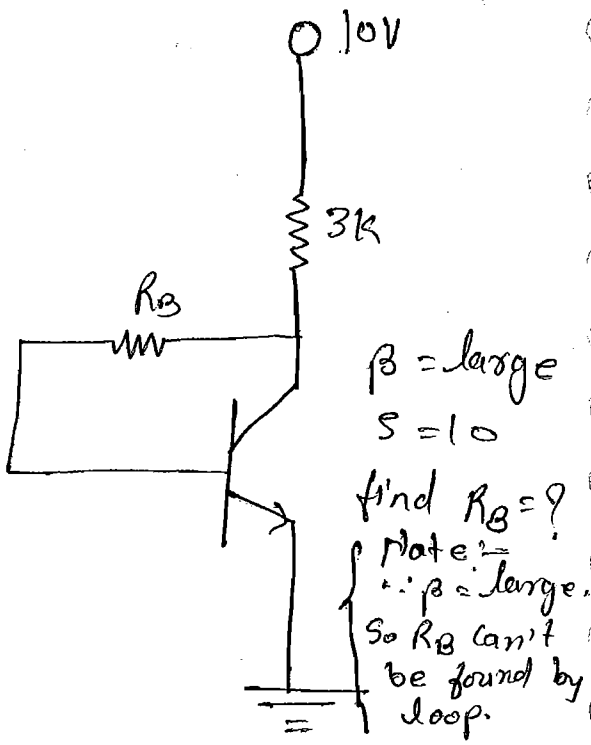
Applying in outward loop :-

$$-10 + I_E \times 3K + V_{CE} = 0$$

$$V_{CE} = 10 - I_E \times 3K$$

$$\boxed{V_{CE} = 3.94V}$$

Q.



$$\therefore S = \frac{1+\beta}{1+\beta \frac{R_C}{R_B+R_C}}$$

$$S = \frac{1+\beta\,(R_B+R_C)}{(R_B+R_C)+\beta R_C}$$

∵ β is very large

So $$S = \frac{\beta\,(R_B+R_C)}{\beta R_C}$$

$$S = \frac{R_B+R_C}{R_C}$$

$$10 = \frac{R_B+3}{3}$$

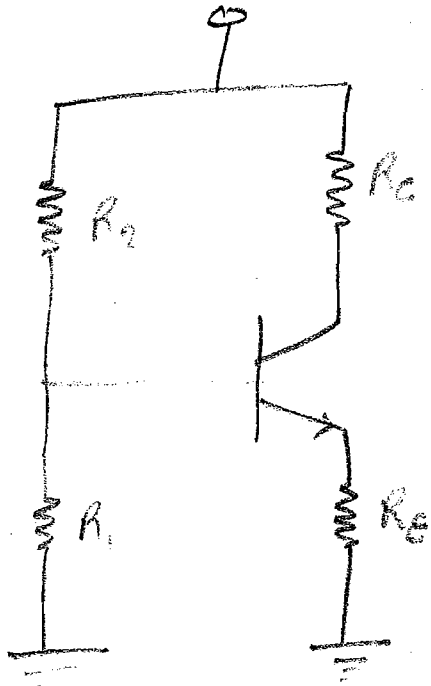
$$30 = R_B + 3$$

$$R_B = 30 - 3$$

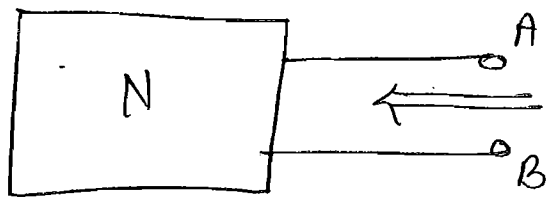
$$\boxed{R_B = 27}$$ Ans

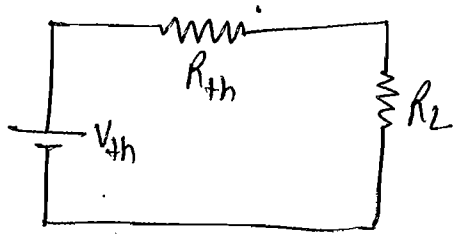
* Self Bias / Voltage Divider Bias / Thevenin Divider Bias :-

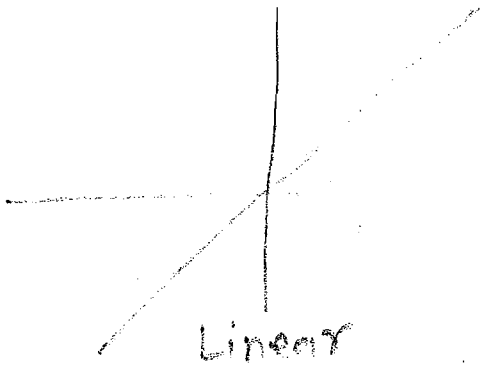
Thevenin's Theorem :-

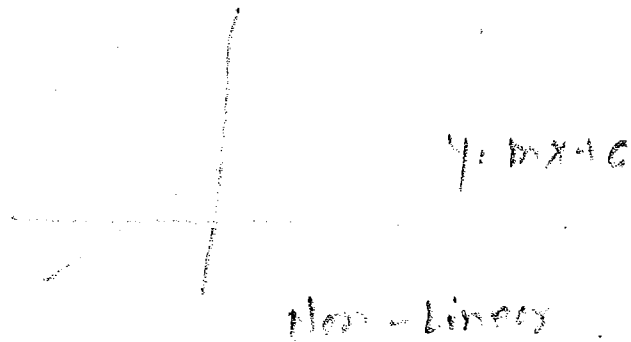


for any linear and bilateral network seen from two terminal A, B the simplified representation a voltage source (V_{th}) and a single Resistance (R_{th}) in series with (V_{th}).







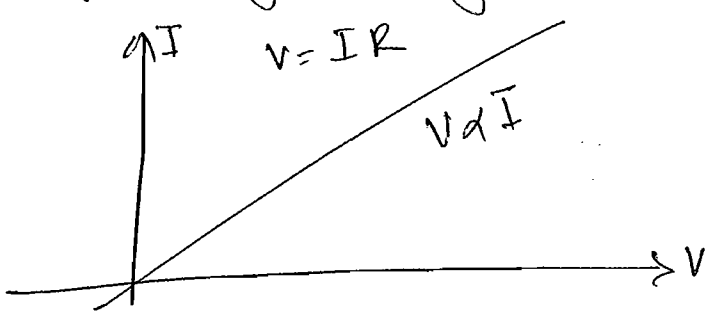


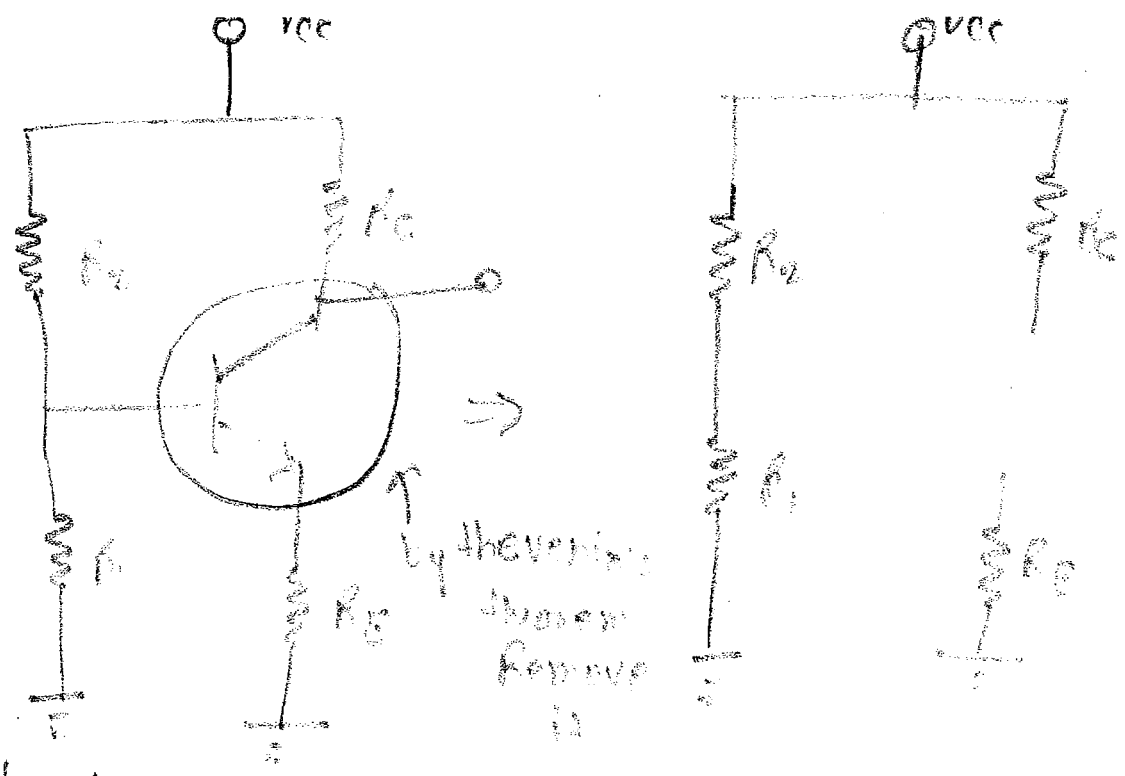
$$3\frac{d^2y}{dx^2} + 4\frac{dy}{dx} + 3y + (2) = 0$$ ← Constant term

So given eqn is non-linear eqn.

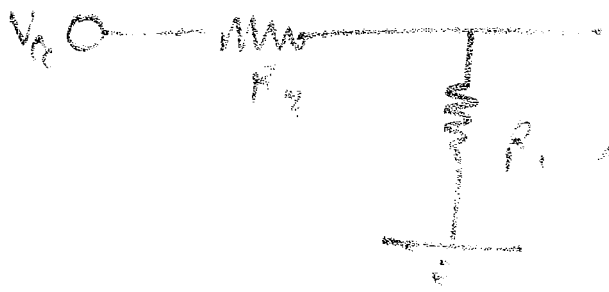
Linear graph must passing through the origin.

Ohm's Law :-



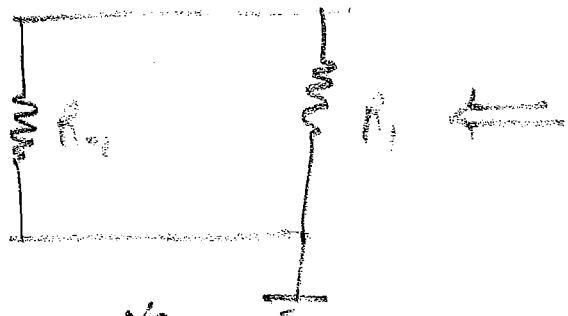


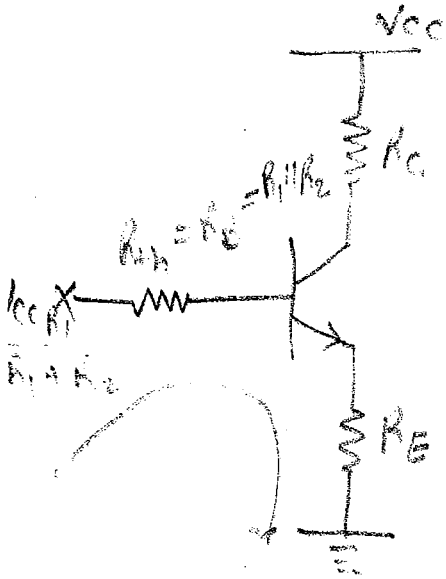
Simplified diagram.



R_1 & R_2 = from voltage divider Rule.

$$V_{th} = \frac{V_{cc} \times R_1}{R_1 + R_2}$$





$$S = \frac{1+\beta}{1+\beta \frac{R_E}{R_C + R_E}}$$

$$-V_{th} + I_B R_B + V_{BE} + I_E R_E = 0$$

$$-V_{th} + I_B R_B + V_{BE} + (I_B + I_E) R_E = 0$$

$$I_B [R_B + R_E] + I_C R_E = V_{th} - V_{BE}$$

$$\therefore \boxed{I_B = \frac{V_{th} - V_{BE}}{R_B + R_E} - \frac{I_C R_E}{R_B + R_E}} \quad \text{(1)}$$

($R_B + R_E$: fixed)

"As temp increases I_{CO} is increases and I_C is also increases given by -

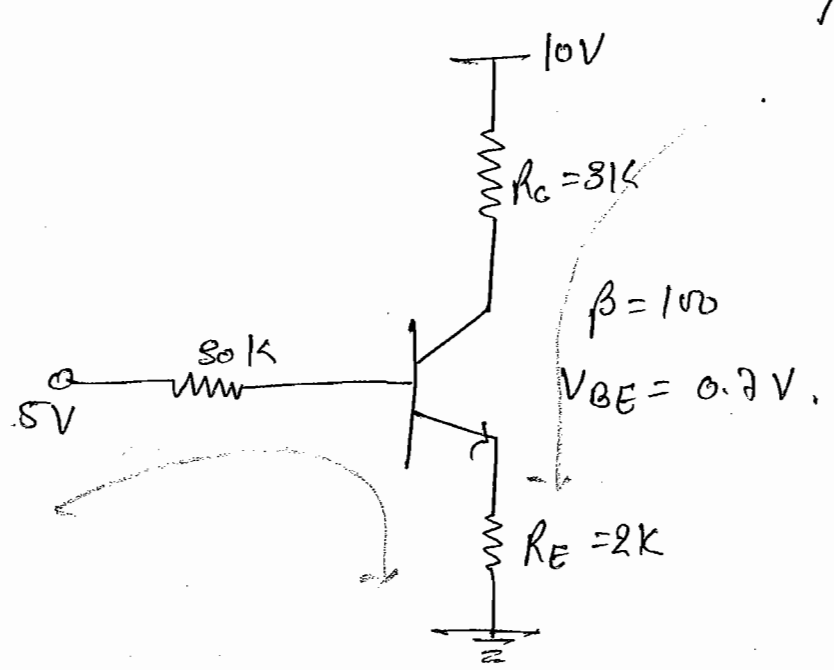
$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

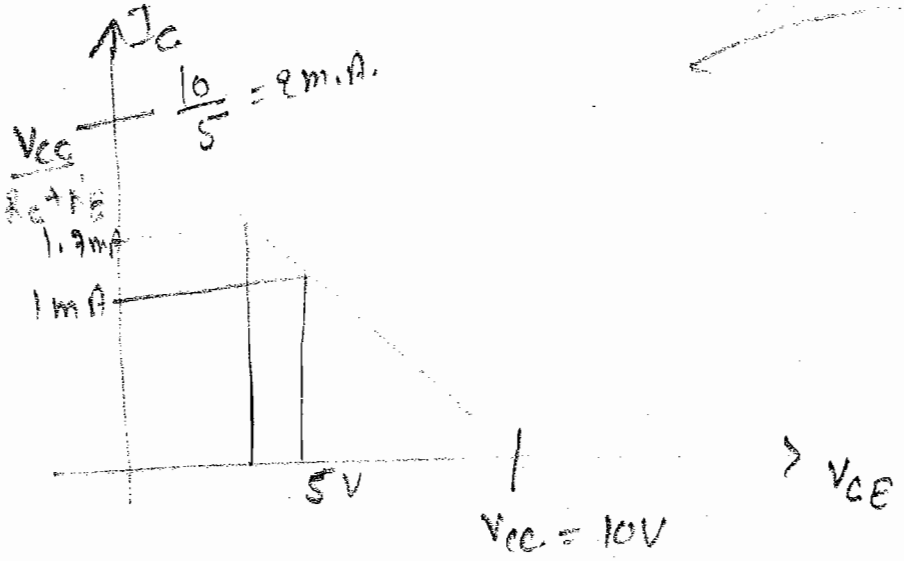
Simultaneously I_B decreases given by eqn (1) Increase in I_{CO} decrease in I_B, the effect cancells out. Hence I_C will be stable."

~~Q. for the given circuit~~

Bias	Stability factor	Approximate analysis (β-range)
fixed	$S = 1 + \beta$	β
C-B bias	$\frac{1+\beta}{1+\beta \frac{R_B}{R_B + R_C}}$	$\frac{1+\beta}{R_C}$
Self Bias	$\frac{1+\beta}{1+\beta \frac{R_B}{R_B + R_E}}$	$\frac{1+\beta}{R_E}$

Q. For the given circuit diagram draw the load line, calculate Q-point, determine the stability factor.





$$-5 + I_B \cdot 50 + 0.7 + I_E \times 2K = 0$$

$$\Rightarrow -5 + I_B \times 50 + 0.7 + (I_B + I_C) \times 2K = 0$$

$$\Rightarrow 52 I_B + 2 I_C = 4.3$$

$$\Rightarrow 52 I_B + 200 I_B = 4.3 \quad \{ I_C = \beta I_B \}$$

$$\Rightarrow I_B \, [252\ K] = 4.3$$

$$I_B = \frac{4.3}{252\ K} = 0.017 \text{ m.A}$$

$$\boxed{I_B = 0.017 \text{ m.A}}$$

$$I_C = \beta I_B$$

$$I_C = 100 \times 0.017 \Rightarrow \boxed{I_C = 1.7 \text{ m.A}}$$

$$-10 + I_C \times 3 + V_{CE} + I_E \times R_E = 0$$

$$\Rightarrow \quad 3I_C + V_{CE} + I_B R_E + I_C R_E = 10$$

$$\Rightarrow \quad 5I_C + 0.017 \times 2 = 10 - V_{CE}$$

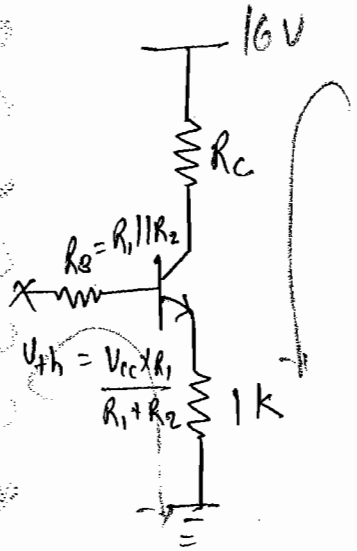
$$\Rightarrow \quad V_{CE} =$$

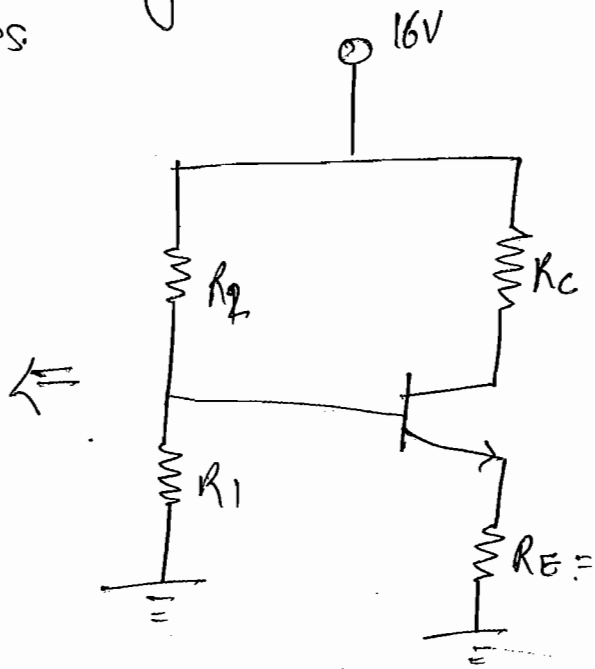
$$S = \frac{1+\beta}{1+\beta \frac{R_E}{R_B + R_E}} = \frac{1+100}{1+100 \times \frac{50}{50+2}}$$

$$= \frac{101}{1+100 \times \frac{50}{52}}$$

$$S = \frac{101 \times 52}{52 + 100 \times 50}$$

Q. For the given circuit diagram determine the resistances





$\beta = 100$

Q [Q m.A, C

$S = 10$

$V_{BE} = 0.7$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad \longrightarrow (I)$$

$$V_{th} = \frac{V_{CC} \times R_1}{R_1 + R_2} \quad \longleftarrow (II)$$

(I)/(II)

$$\frac{R_B}{V_{th}} = \frac{R_1 R_2}{V_{CC} R_1} = \frac{R_2}{V_{CC}}$$

$$\boxed{\frac{R_B}{V_{th}} = \frac{R_2}{V_{CC}}}$$

$$S = \frac{1+\beta}{1+\beta \cdot \frac{R_E}{R_B + R_E}} \Rightarrow \frac{101}{1 + \frac{100}{R_B + 1}} = 10$$

$$= \frac{(101)(R_B + 1)}{R_B + 101} = 10$$

$$\Rightarrow 10R_B + 1010 = 101R_B + 10$$

$$\rightarrow 91 R_B = 1010 - 101$$

$$91 R_B = 909$$

$$R_B = \frac{909}{91}$$

$$= 9.9 \approx 10$$

$$\boxed{R_B = 10k}$$

(2m.A, 0V)

$$I_C = 2m.A, \quad V_{CC} = 0V$$

$$I_B = \frac{I_C}{\beta} = \frac{2}{100} = 0.02 m.A$$

$$I_B = 0.02\ mA$$

$$-V_{th} + I_B \times R_B + V_{BE} + I_E \times R_E = 0$$

$$\Rightarrow \quad I_E = \frac{V_{th} - V_{BE}}{I_B R_B}$$

$$= \frac{V_{th} - 0.7}{0.02 \times 10}$$

$$I_B + I_C = \frac{V_{th} - 0.7}{0.2}$$

$$\Rightarrow \quad V_{th} = 0.2\,(2.02) + 0.7$$

$$V_{th} = 2.9\ V$$

$$\frac{R_B}{V_{th}} = \frac{R_2}{V_{CC}}$$

$$R_2 = \frac{V_{CC} \times R_B}{V_{th}} = \frac{16 \times 10}{2.9}$$

$$R_2 = \frac{160}{2.9}\,k =$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} =$$

Applying loop :-

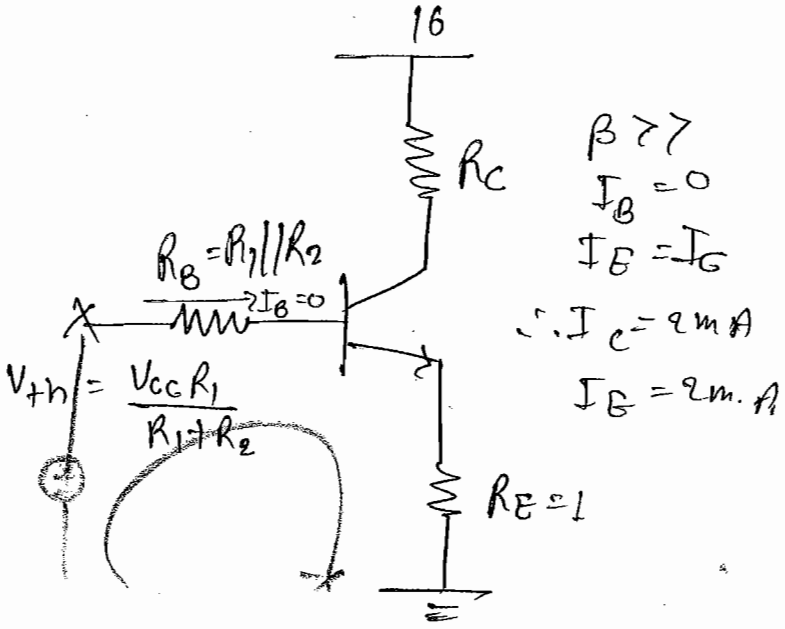
$$-16 + I_C \times R_C + V_{CE} + I_E R_E = 0$$

$$\Rightarrow \quad R_C = \frac{2.02 + 16 - 8}{2} = \frac{-2.02 + 8}{2}$$

$$= \frac{5.98}{2} = 2.98\ V$$

$$R_C = 2.98 \approx 3\ V$$

Q. Repeat the previous Question assuming β is very large.



$\beta \gg 7$
$I_B = 0$
$I_E = I_C$
$\therefore I_C = 2\,mA$
$I_E = 2\,m.A$

$$S = 1 + \frac{R_B}{R_E}$$

$$10 = 1 + \frac{R_B}{R_E}$$

$$9 = \frac{R_B}{1}$$

$$\boxed{R_B = 9K}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad \text{---(1)}$$

$$V_{th} = \frac{V_{CC} \times R_1}{R_1 + R_2} \quad \text{---(11)}$$

$$\frac{R_B}{V_{th}} = \frac{R_2}{V_{CC}} \quad \text{---(3)}$$

Applying loop :-

$$V_{th} + 0.7 + 2 \times 1 = 0$$

$$V_{th} = 0.7 + 2 = 2.7$$

$$\boxed{V_{th} = 2.7\,V}$$

from (14)

$$\frac{9}{2.7} = \frac{R_2}{16}$$

$$R_2 = \frac{16 \times 9}{2.7} = \frac{160}{3} = 53.33$$

$$\boxed{R_2 = 53.33K}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

$$9 = \frac{R_1 \times 53.33}{R_1 + 53.33}$$

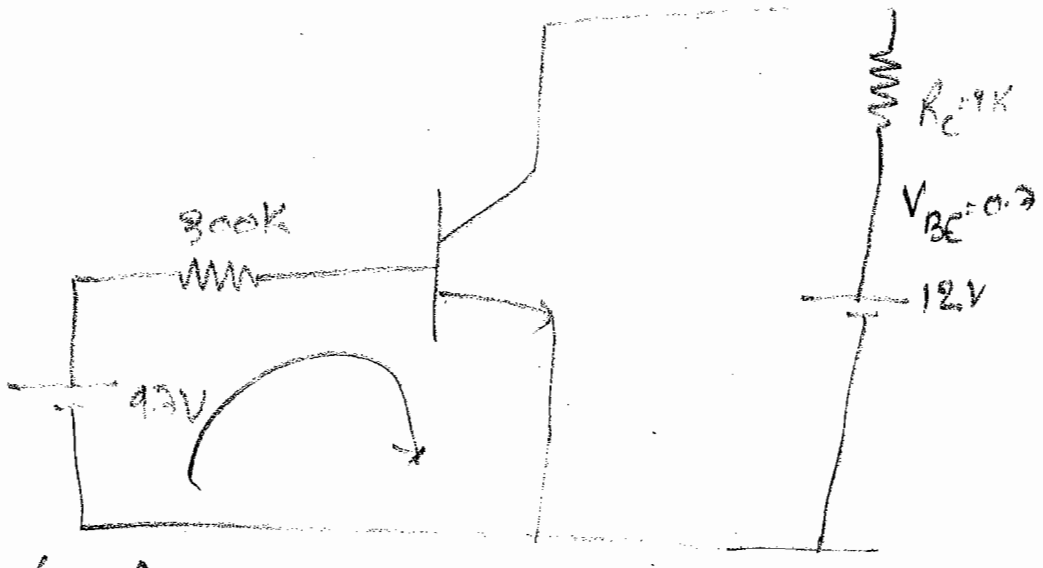
$$9R_1 + 9 \times 53.33 = R_1 \times 53.33$$

$$9 \times 53.33 = R_1 \times 53.33 - 9R_1$$

$$R_1 = \frac{9 \times 53.33}{(53.33 - 9)}$$

$$\boxed{R_1 = 10.827\Omega}$$

Pg.-17
Q. 04



$$\frac{V_{CC}}{R_C} = \frac{12}{2} = 6\,mA$$

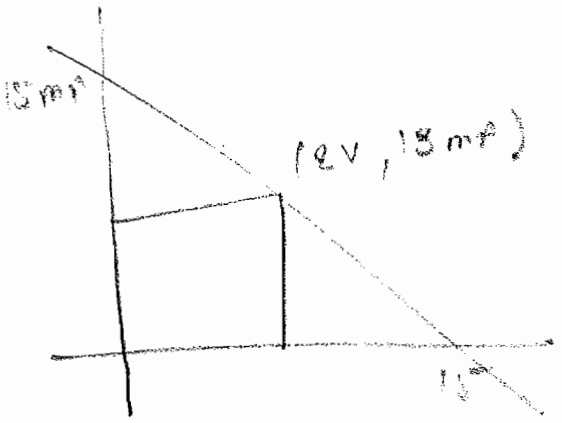
(b) and (c)

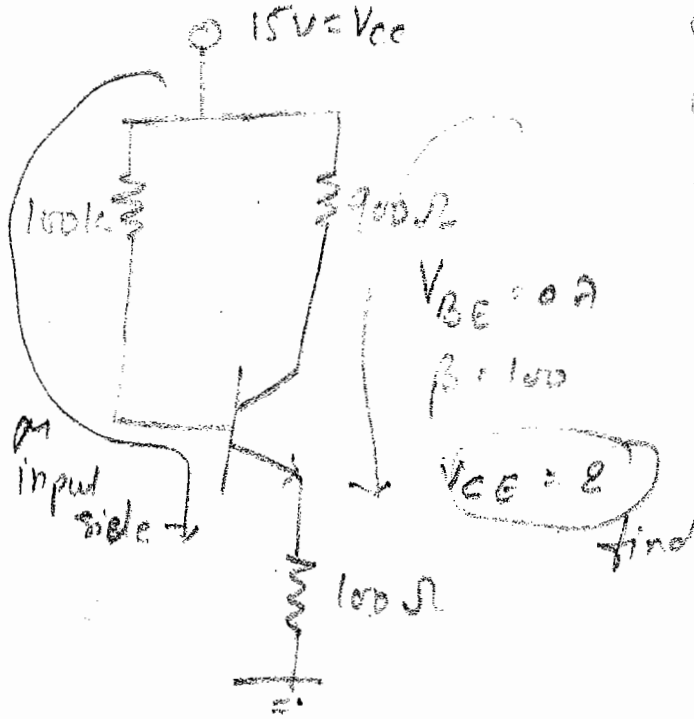
$-9 + I_B \times 2 + 0.7 = 0$

$I_B = 0.03\,mA$

$I_B = 30\,\mu A$

Q.38





$$-15V + I_B \times 100k + 0.7 + (I_B + I_C) \times 100\Omega = 0$$

$$I_B \times 100k + (I_B + I_C)\, 0.1K = 14.3$$

$$I_B \times 100k + (I_B + 100 I_B) \times 0.1k = 14.3$$

$$I_B (100k + 10.1k) = 14.3$$

$$I_B = \frac{14.3}{110.1} m.A$$

$$\boxed{I_B = 0.13 m.A}$$

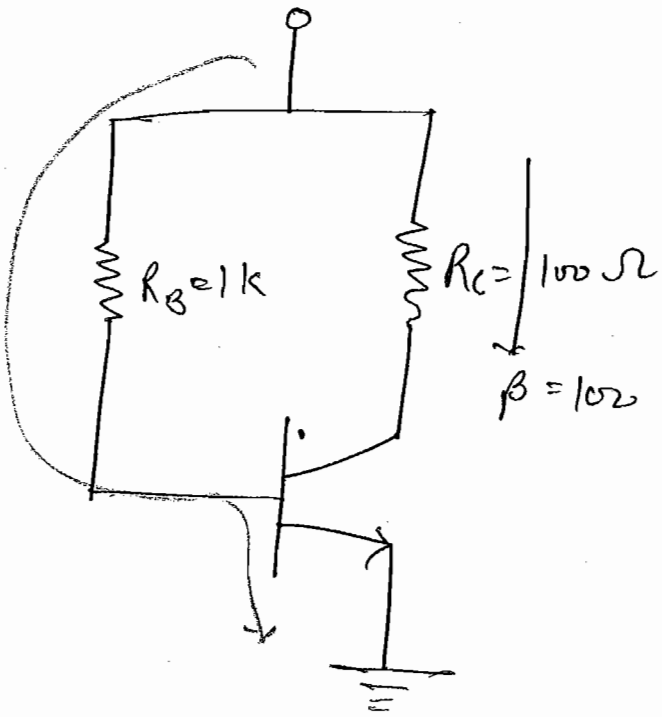
$$I_C = \beta I_B$$

$$I_C = 100 \times 0.13 m.A.$$

$$\boxed{I_C = 13 m.A.}$$

$$-15 + I_C \times 0.9 + V_{CE} + (I_B + I_C)\, 0.1K = 0$$

P.g.11
Q.52



$$-5V + I_B \times 1k + 0.7 = 0$$

$$\Rightarrow \boxed{I_B = 4.3\ m.A.}$$

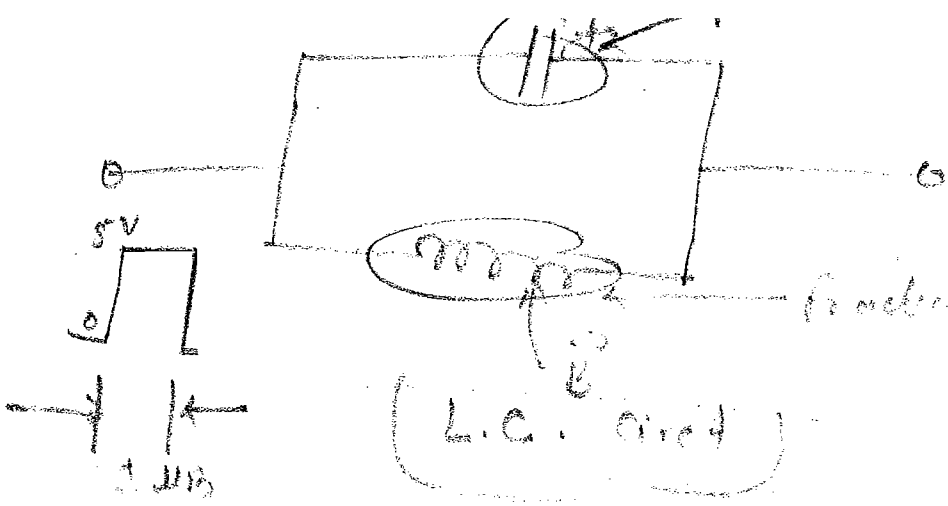
$$I_C = \beta I_B$$

$$I_C = 4.3 \times 100\ m.A.$$

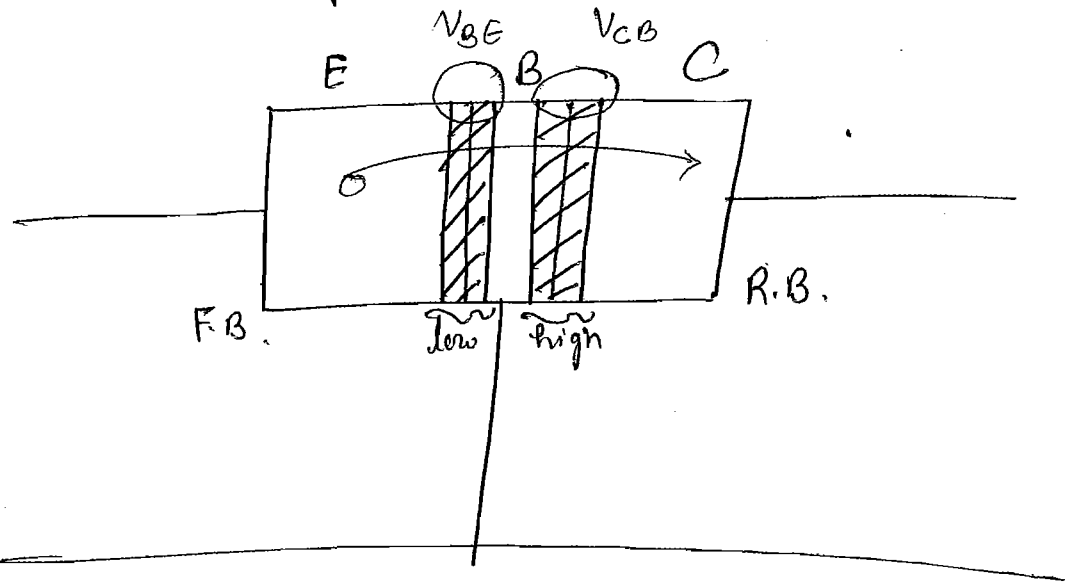
$$= .43 \times 10^{-3} \times 10^{3}\ A$$

$$\boxed{I_C = 0.43\ A}$$

P.g-13
Q.67) Ans (d)



* Power Dissipation in the Transistor :-



Power dissipation in emitter junction.

$$P_E = V_{BE} \times I_E \quad \text{——— (I)}$$

Power add in collector junction

$$P_C = V_{CB} \times I_C \quad \text{——— (II)}$$

Total Power

$$P_t = P_E + P_C$$

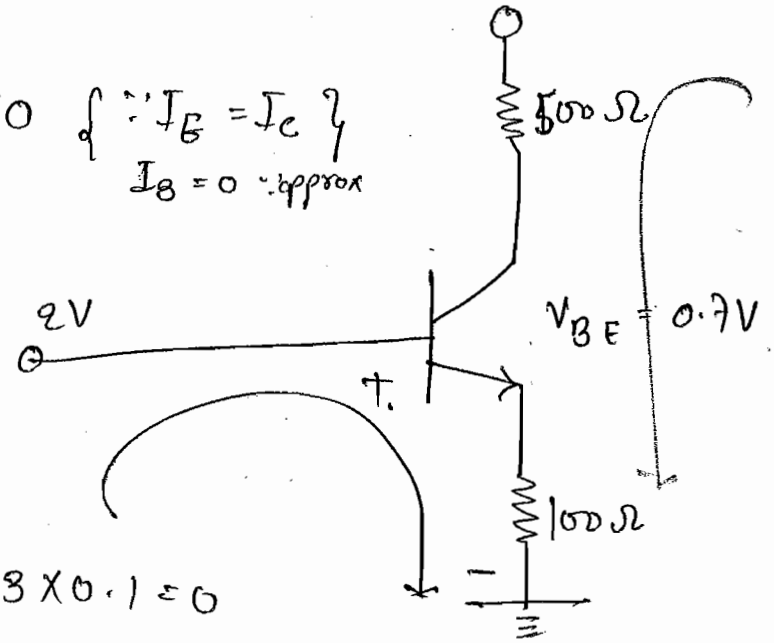
$$= V_{BE} \times I_E + V_{CB} \times I_C$$

$$\boxed{P_t = V_{CB} I_C + V_{BE} I_E} \quad \text{——— (III)}$$

$$P_t = (V_{CB} + V_{BE}) I_C$$

$$\boxed{P_t = V_{CE} I_C}$$

TIFR
P.g 4
Q. 13



$-2 + 0.7 + I_C \times 100 = 10$ $\{ \because I_B = I_C \}$
$I_B = 0$ approx

$$I_C = \frac{1.3}{100}$$

$$\boxed{I_C = 13\ mA}$$

$-15 + 13 \times 0.5 + V_{CE} + 13 \times 0.1 = 0$

$\Rightarrow V_{CE} = 15 + 6.5 + 1.3$

$= 15 - 7.8 = 7.2$

$$\boxed{V_{CE} = 7.2\ V}$$

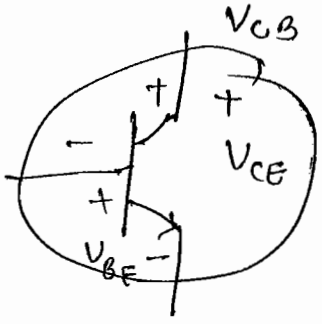
$P = V_{CE} \times I_C$

$= 13 \times 7.2$

$$\boxed{P = 93.6\ m.watt.}$$ Ans

Second Method :-

$-V_{CE}$



Q. For the given circuit diagram calculate power dissipation across the transistor.

From previous qums.

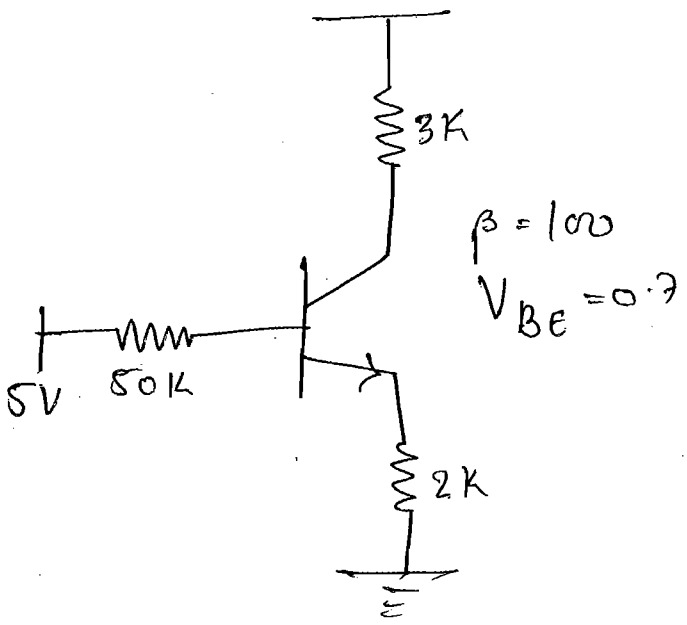
$I_C = 1.7\ mA$

$V_{CE} = 1.4V$

$I_B = 0.017\ mA$

$\therefore P_t = (1.7 \times 1.4)\ mA$

$\boxed{P_t = 2.40\ mW}$



Exact Method :-

$V_{CB} = V_{CE} - V_{BE}$

$= 1.46 - 0.7$

$\boxed{V_{CB} = 0.76V}$

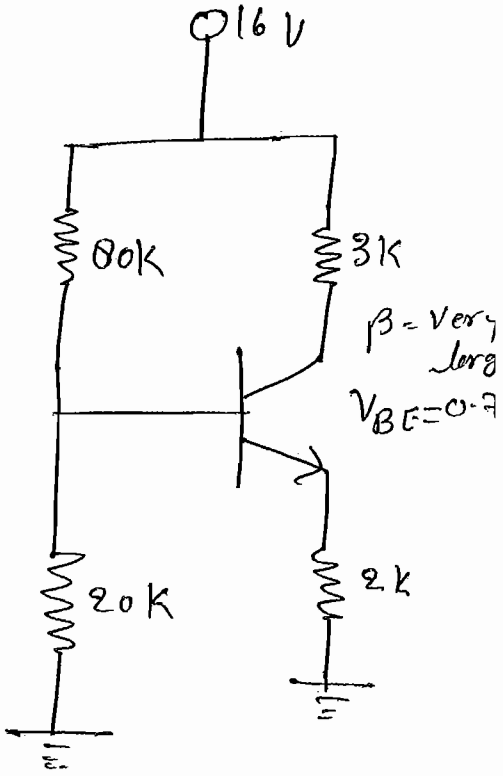
$P_t = V_{BE} \times I_E + V_{CB} \times I_C$

$= 0.7 \times 1.717 + 0.76 \times 1.7$

$= 1.2011 + 1.292$

$\boxed{P_t = 2.49\ mW}$

Q. For the given circuit diagram find power dissipation.


16 V
80K
3K
β = very large
V_{BE} = 0.7
20K
2K

Field Effect Transistor

The divice operating under the influence of electric field. It is a unipolar divice i.e. single type of charge carriers involved in the conduction processe only mefority carriers present & minority carriers negligible hence minority carrier curren also negligible. hence device is independent of temp. Henee thermally stable.

* Construction of Junction field Effect Transistor

Field Effect Transistor

JFET

3-terminal divice

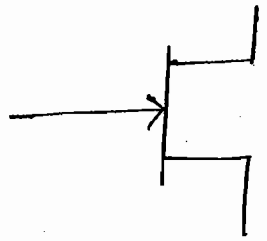
→ Source → Emitter
→ Drain → Collector
→ Gate → Base

n-channel P-channel

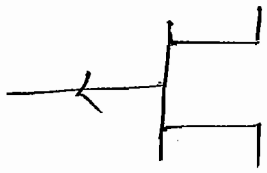
MOSFET

→ IGFET
→ MOST
→ 4-terminal device
→ Source
→ Drain
→ Gate
→ Body

⇒ MOSFET is having very high input resistance as compaired to JFET because Oxide layer is used in MOSFET. ($S_2 + O_2 \xrightarrow{1400}$



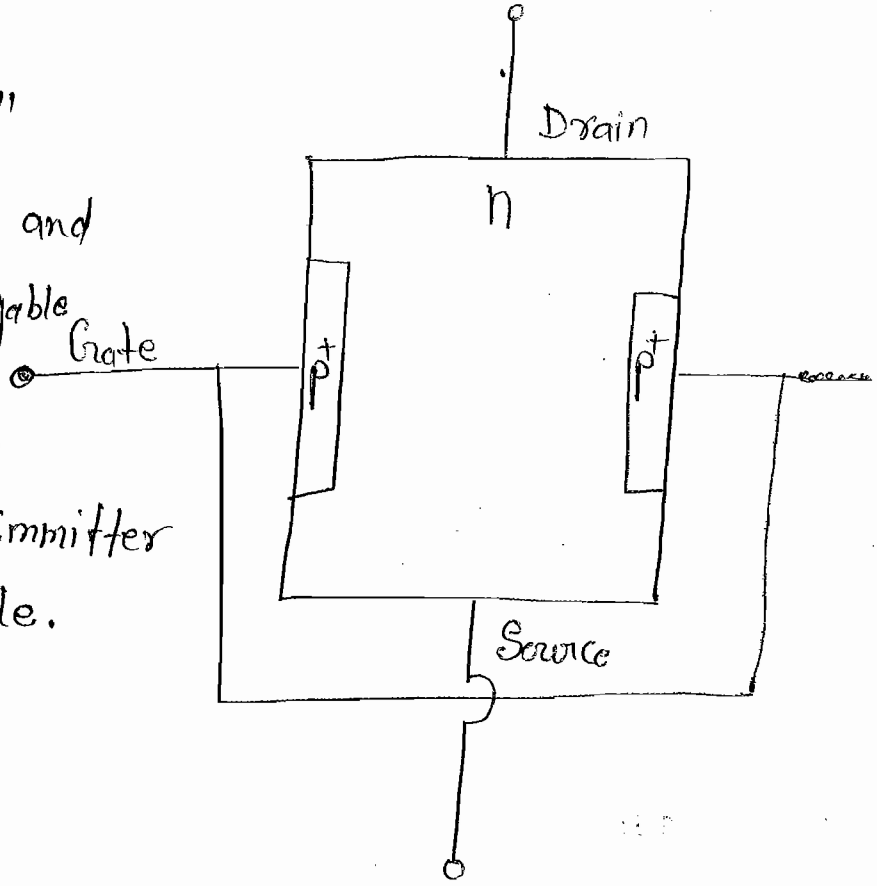
(n-channel)



(p-channel)

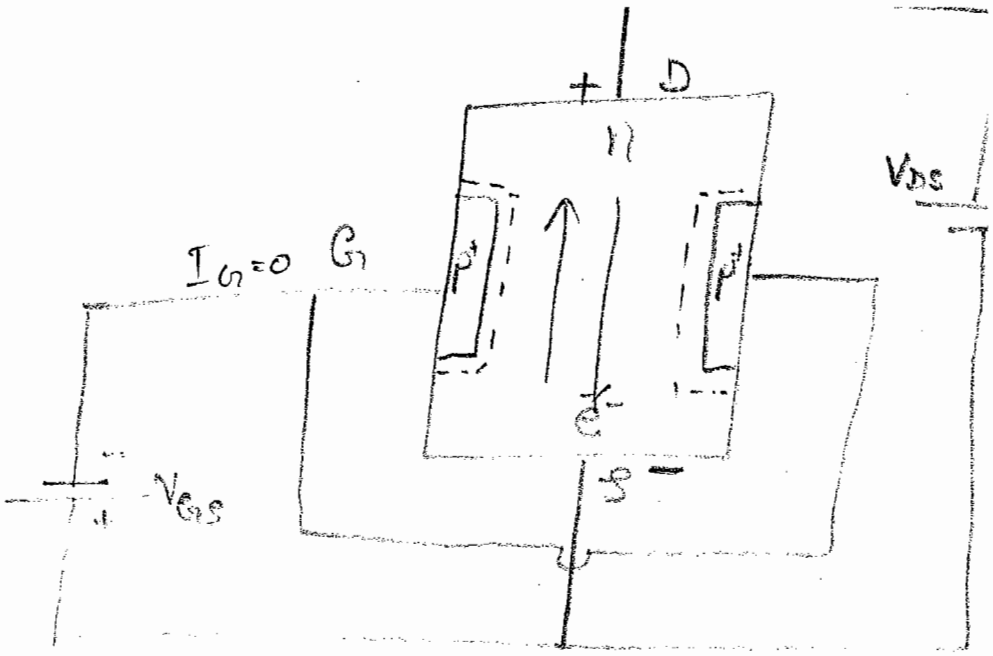
* Construction of n-channel JFET :-

FET is a "symmetrical" device because drain and source are interchangable but B.J.T. is a non-symmetrical device because collector & Emmitter are not interchangeable.



* Biasing of JFET :-

(Biasing means how to apply the voltage to work the device).



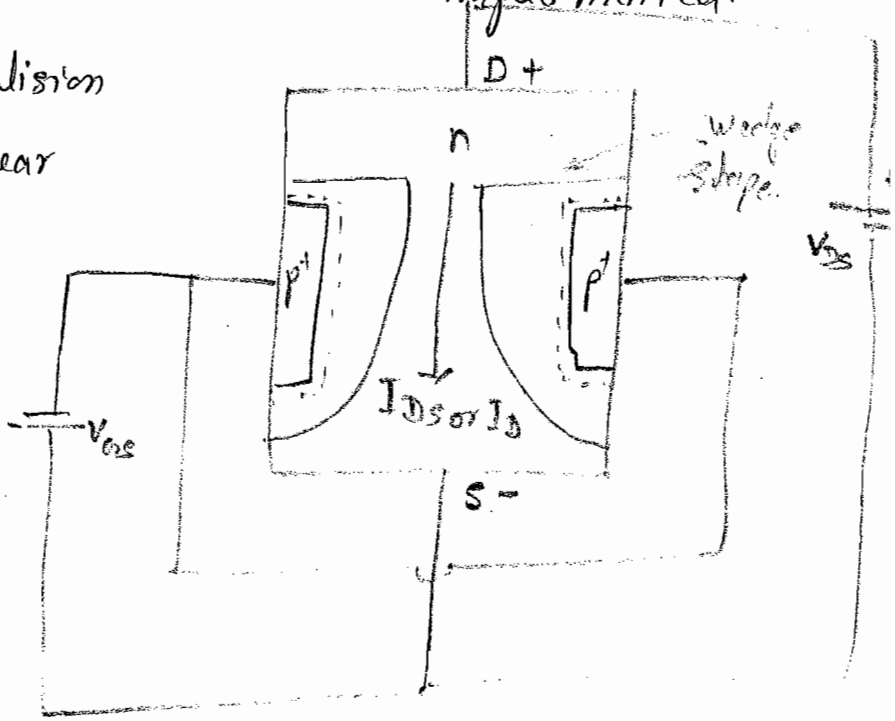
for the analysis of the transistor since gate is Reverse Biased then $I_G = 0$.

* Transfer Characteristic :-

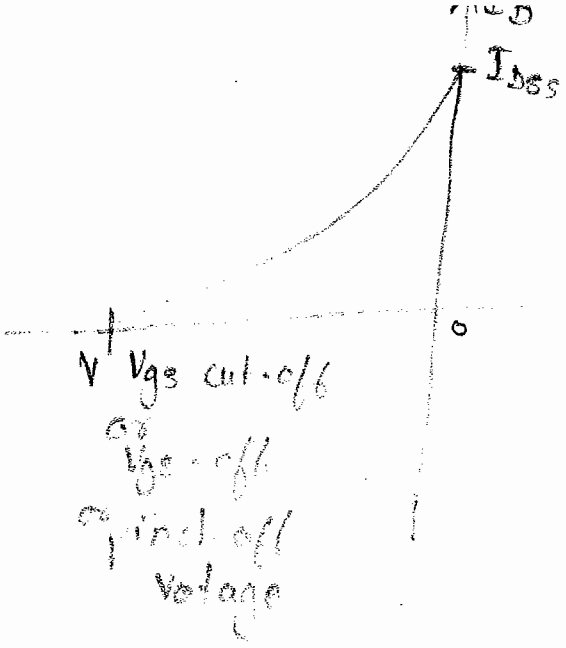
Since input current $I_G = 0$ it is not possible to draw input characteristic Hence transfer characteristics are implemented.

The shape of the depletion region is larger near ~~drain~~ ~~gate~~ Drain and Smaller near source.

The shape of depletion layer is Wedge shape.



When $V_{GS}=0$ the current through the channel is maxm. As V_{GS} increases reverse biase voltage is increases.



The depletion region will move towards each other, the flow of charge carriers reduces. Hence current also decreases.

As V_{GS} increases to such an extent the two depletion region penitrate in each other current through the channel is zero that voltage is called pinch-off voltage (V_{gs} cut off or V_{gs} off).

$$I_D = I_{DSS}\left[1 - \frac{V_{gs}}{V_p}\right]^2$$

→ It is a square law device.

* Transconductance :-

$$\frac{\partial I_D}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}}\left[I_{DSS}\left(1 - \frac{V_{gs}}{V_p}\right)^2\right]$$

$$= I_{DSS}\frac{\partial}{\partial V_{gs}}\left[1 - \frac{V_{gs}}{V_p}\right]^2$$

$$= 2\,I_{DSS}\left[1 - \frac{V_{gs}}{V_p}\right]\left[-\frac{1}{V_p}\right]$$

$$g_m = -\frac{2 I_{DSS}}{V_p}\left[1 - \frac{V_{gs}}{V_p}\right]$$

* Maximum Transconductance :-

$$(g_m)_{max} = \frac{-2 I_{DSS}}{V_p} \qquad (\because V_{gs} = 0)$$

Q. An n-channel junction field effect transistor has $I_{DSS} = 10\,m.A.$, $V_{gs} = -2V$, $V_p = -8V$. Calculate I_D, g_m, $(g_m)_{max}$.

Soln

$$I_D = 10\left[1 - \frac{2}{8}\right]^2$$

$$= 10\left[\frac{03}{04}\right]$$

$$\boxed{I_D = 5.6\ m.A.}$$

$$g_m = \frac{+2 \times 10}{+3}\left[1 - \frac{2}{8}\right]$$

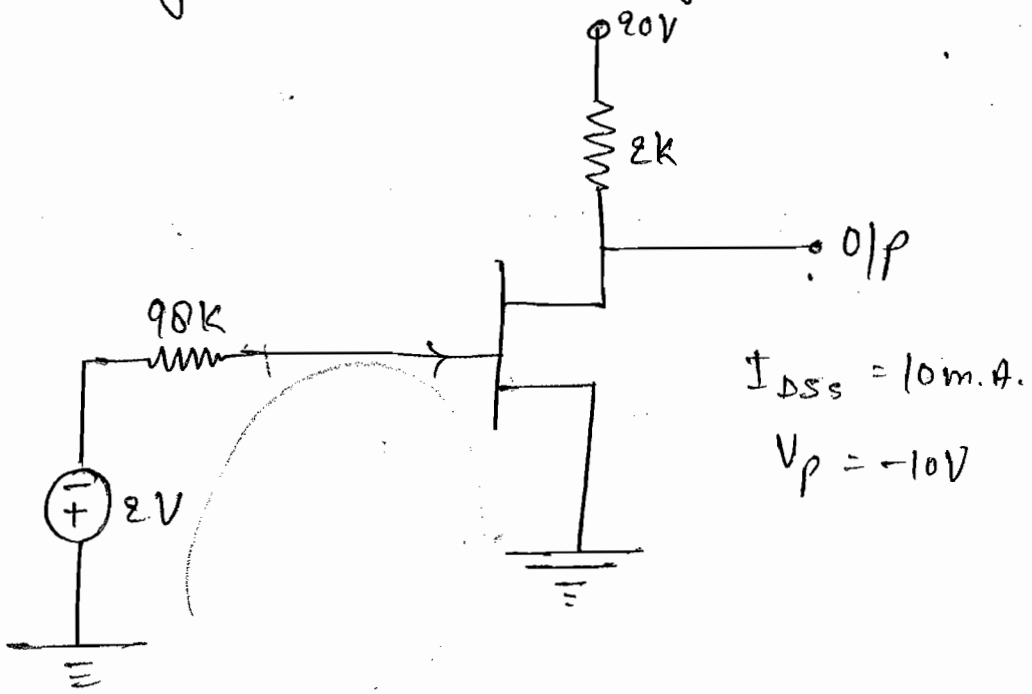
$$= \frac{5}{2}\left(\frac{6^3}{8}\right] = \frac{15}{8}$$

$$\boxed{g_m = 1.8\ \frac{m.\eta}{V}}$$ or $\mho$ or mines.

$$(g_m)_{max} = \frac{-2 \times 10}{-8.4}$$

$$\boxed{(g_m)_{max} = 2.5 \text{ mhos.}}$$

Q. For the given circuit diagram.



$$I_D = I_{DSS}\left[1 - \frac{V_{gs}}{V_p}\right]^2$$

$$+2 + I_g \times 98k + V_{gs} = 0$$

$$\because I_g = 0$$

So $\boxed{V_{gs} = -2V}$

$$I_D = 10\left[1 - \frac{2}{10}\right]^2 = \cancel{10 \times \frac{8}{10}} \times \frac{8}{10}$$

$\boxed{I_D = 6.4\text{m.A.}}$

$$(g_m)_{max} = \frac{+2 \times 10}{+10} = 2$$

$$\boxed{(g_m)_{max} = 2}$$

$$g_m = \frac{-2I_{gs}}{V_p}\left(1 - \frac{V_{gs}}{V_p}\right)$$

$$= \frac{+2 \times 10\,mA}{+10}\left[1 + \frac{2}{10}\right]$$

$$= 2 \times \frac{4}{5} = \frac{8}{5}$$

$$\boxed{g_m = 1.6}$$

Q.88

Soln

Check - (3.16) A_v

$$I_{DSS} = 5\,mA$$

$$V_p = -5$$

$$V_{gs} = -2.5$$

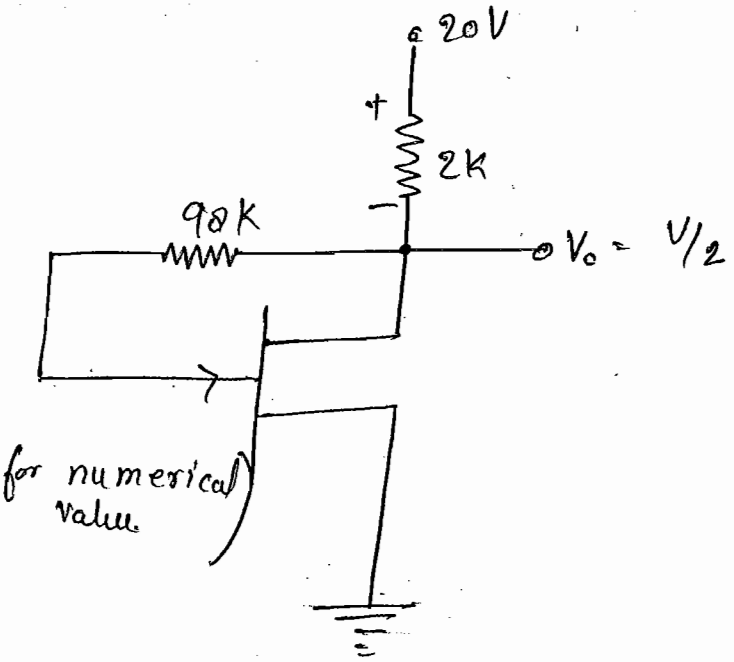
$$I_D = I_{DSS}\left[1 - \frac{V_{gs}}{V_p}\right]^2$$

$$= 5\left[1 - \frac{2.5}{5}\right]^2$$

$$= 5 \times 16$$

$$= 80$$

Q.



Always $I_S = I_D$ (for numerical value)

$$I_D = \frac{20-10}{2} = \frac{10}{2} = 5\ m.A.$$

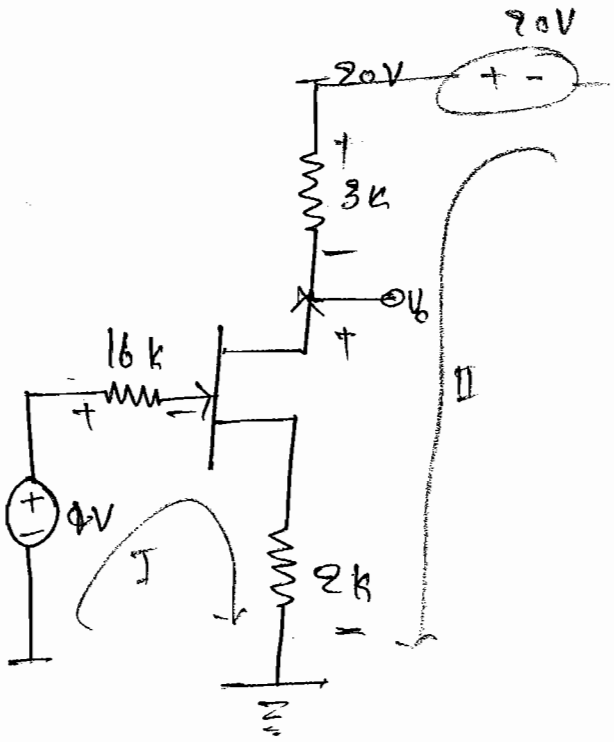
Q. An n-channel JFET having I_D changes from 3 m.A to 3.1 m.A. if V_{gs} changes from (-2 to -1.8) Volt find transconductance

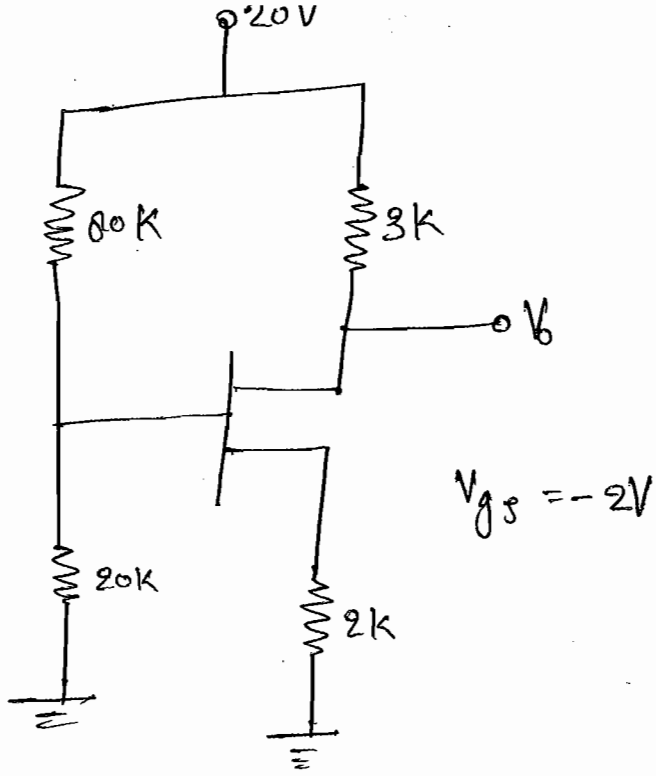
Soln

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{(3.1-3)}{(-1.8-(-2))} = \frac{0.1}{0.2}$$

$$g_m = 0.5 \cdot \frac{m.A}{V}$$

Q. for the given circuit diagram find I_D, I_S, V_o shown in figure.





$V_{gs} = -2V$

equivalent

$$V_g = \frac{20 \times 80}{20+80} = \frac{400}{100} = 4 \text{ Volt.}$$

$$\boxed{V_g = 4 \text{ Volt}}$$

$$-4 + I_g \times 16k + V_{gs} + I_s \times 2k = 0$$

$$-4 + (-2) + I_s \times 2k = 0$$

$$\therefore I_s = \frac{6}{2} = 3 \text{ m.A} = I_D$$

In second loop:-

$$-20 + I_D \times 3 + V_o = 0$$

$$V_o = 20 - I_D \times 3$$

$$= 20 - 3 \times 3$$

$$\boxed{V_o = 11V}$$

Determine the voltage $V_{DS} = ?$

$$-20 + I_D \times 3k + V_{DS} + I_S \times 2K = 0$$

$$-20 + 3mA \times 3K + V_{DS} + 3mA \times 2K = 0$$

$$V_{DS} = 20 - 9 - 6$$

$$\boxed{V_{DS} = 5\,V}$$

Second method :-

$$V_0 = +V_{DS} + I_S \times 2K$$

So $V_{DS} = V_0 - I_S \times 2K$

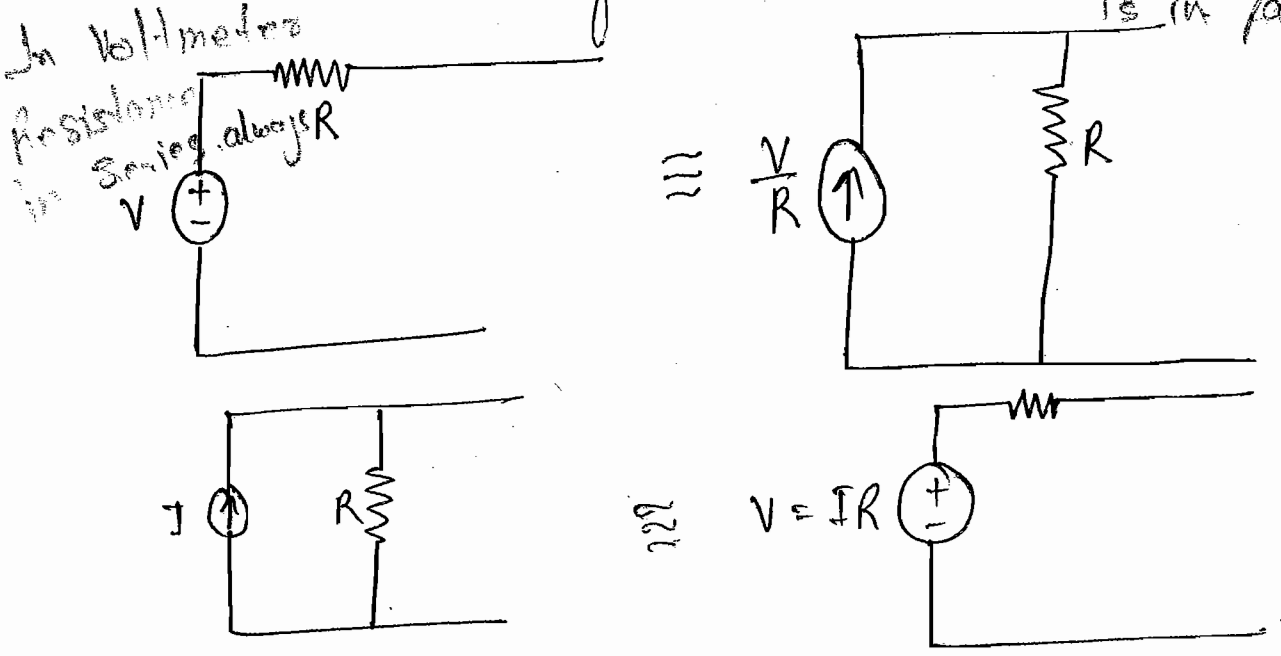
$= 11 - 3 \times 2$

$= 11 - 6$

$$\boxed{V_{DS} = 5\,V}$$

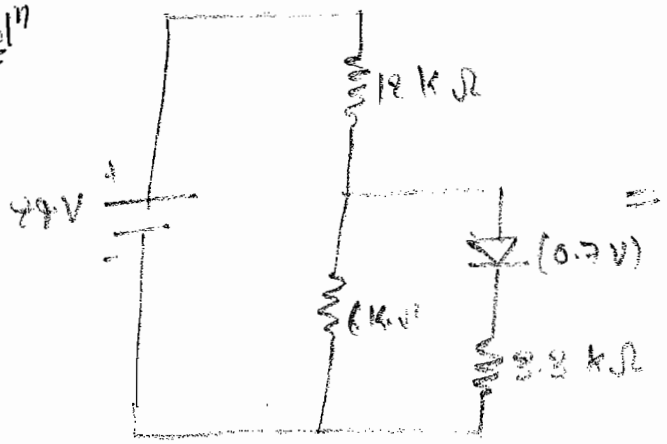
* Source Transformation :- In ameter Resistance always is in parallel

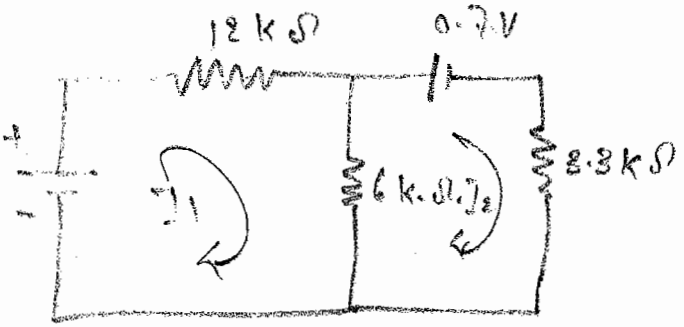
In Voltmeter resistance always in series



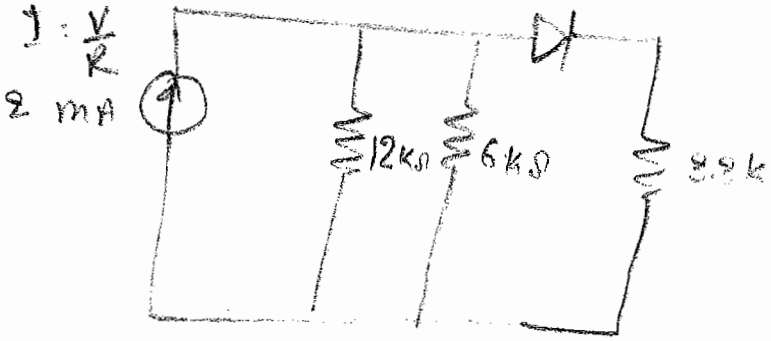
Q.35

Soln

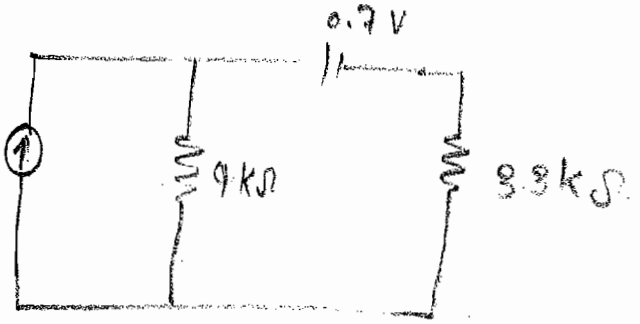


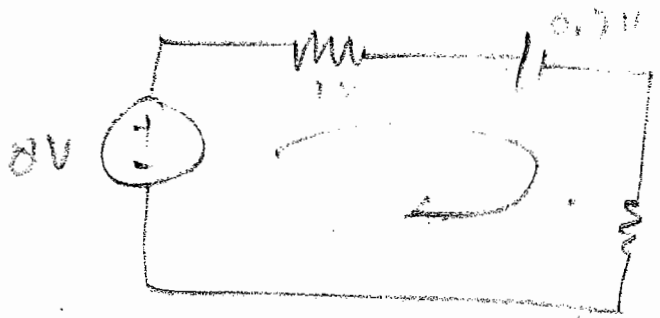


Simplified diagram.



$$R_{11} = \frac{R_1 R_2}{R_1 + R_2} = \frac{12 \times 6}{12+6} = \frac{12 \times 6}{18} = 4\,k\Omega$$



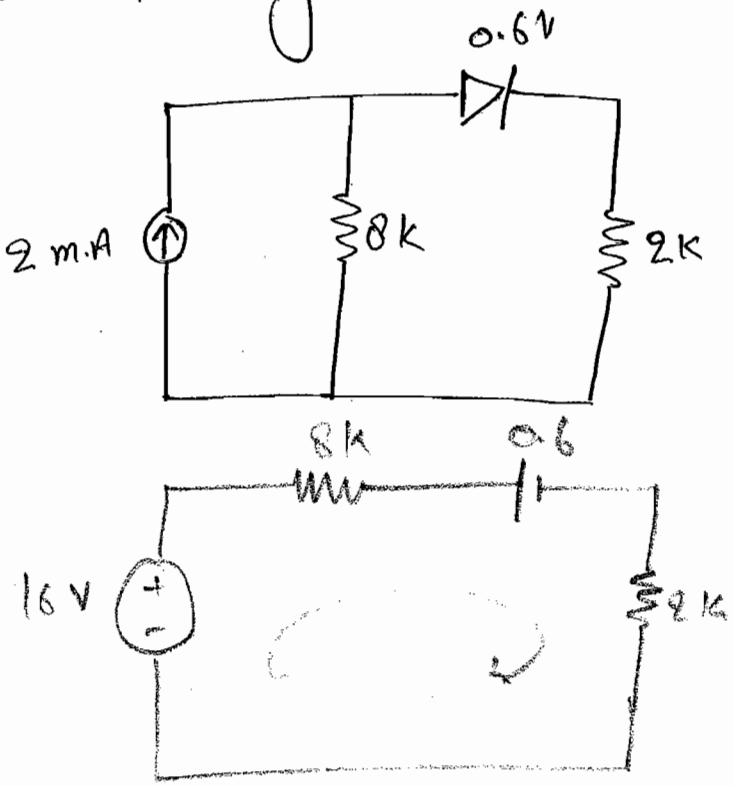


$-8V + 4KI + 0.7 + 3.3I = 0$

$7.3I = 7.3$

$I = 1mA.$

Q. for the given circuit diagram



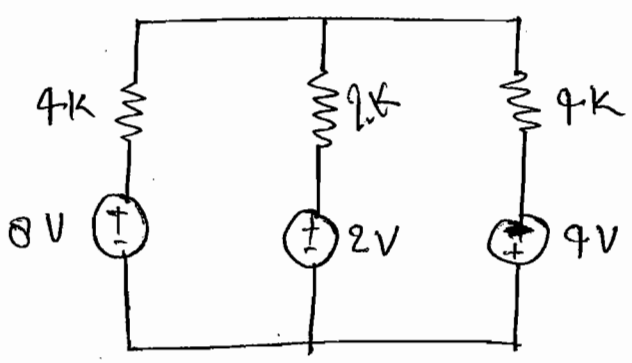
$$-16 + I(8+2)k + 0.6 = 0$$

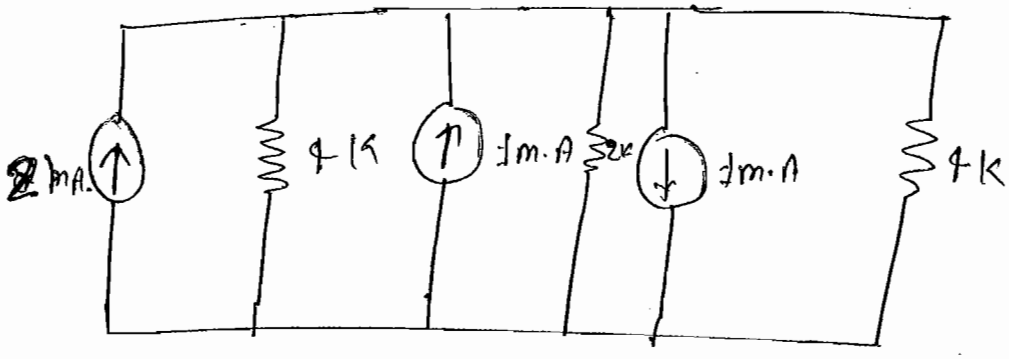
$$10I = 15.4$$

$$I = \frac{15.4}{10}$$

$$I = 1.54 \text{ mA}$$

Q. Convert the entire circuit in single current and single registance.

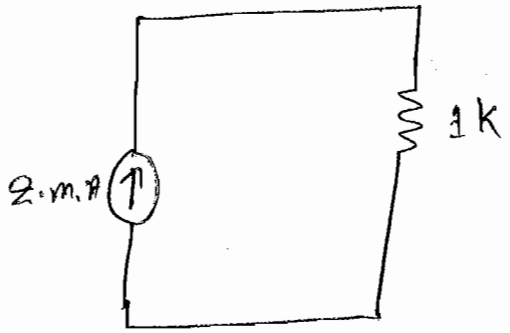




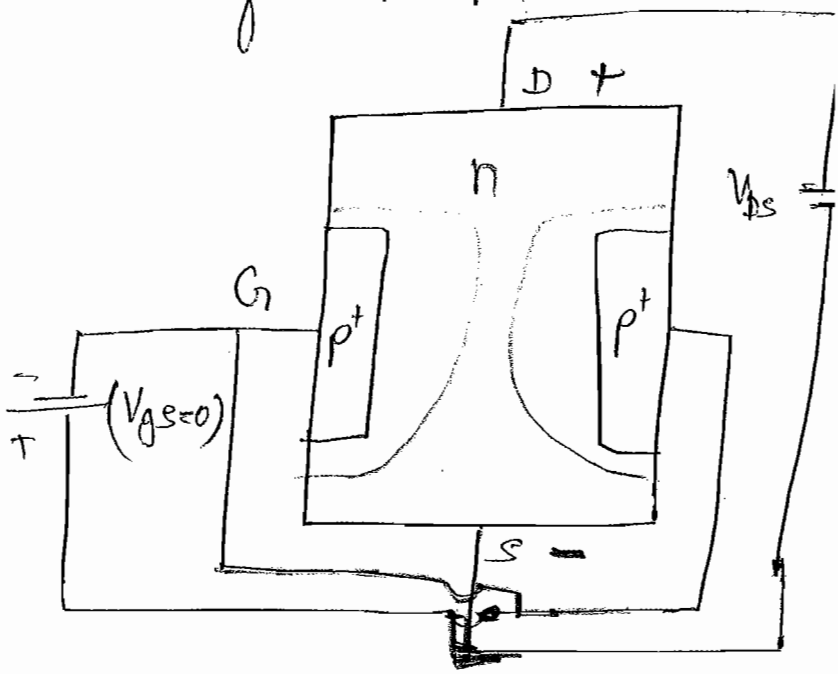
$$R_{11} = \frac{4 \times 2 \times 4}{4+2+4} = \frac{4 \times 2}{4+2} = \frac{8}{6}$$

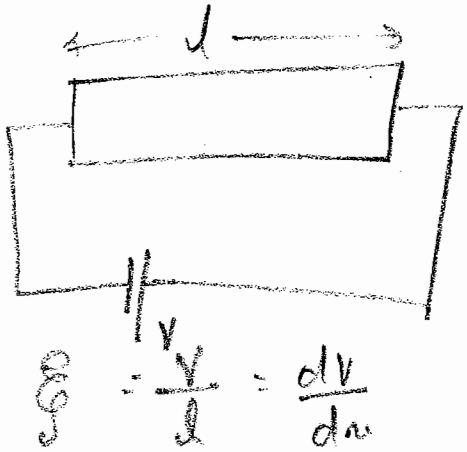
$$= \frac{\frac{8}{6} \times 4 = 2}{\frac{8}{6} + 4 = 2} = \frac{\frac{16}{3}}{\frac{16}{3}} = 1\,k$$

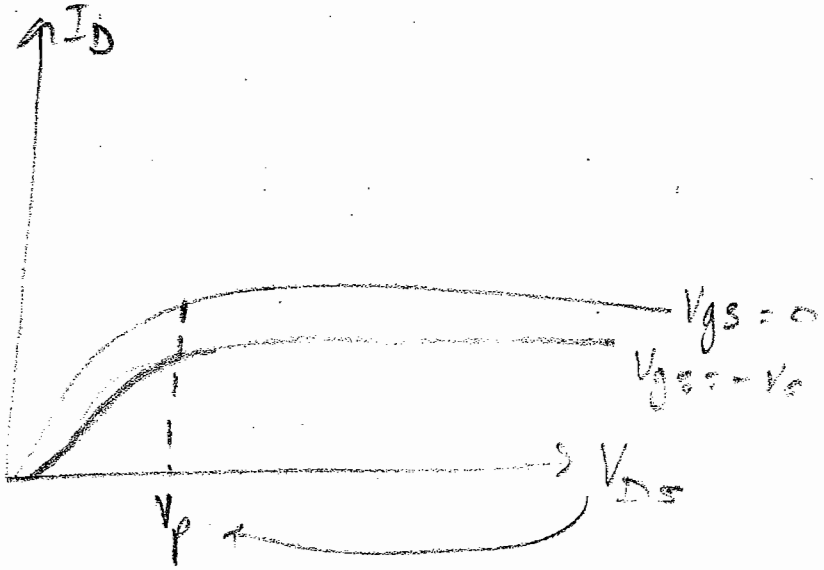
$R_{11} = 1\,k$



* Output characteristics of JFET :-







⇒ When V_{DS} applied the two depletion region will try to move towards each other simultaniously a potential difference is applied hence electric field generated in the channel pointing from (+ to −ve) Drain to Source which will maintains a constant gap between two depletion region, Hence Constant amount of current flows through the channel.

* LOGIC FAMILIES :-

Analog to Digital Converter And Digital to Analog Converter

* Analog to Digital Converter :-
* Counter type ADC ← Basic Converter.
* Successive appox type ADC ← Uniform Converter
* Flash type Converter ADC ← Fastest converter or simultanious converter.
* Dual slope Converter ADC ← Slowest Converter

* Digital to Analog Converter :-
* Weighted register type
* R to 2R ladder network.

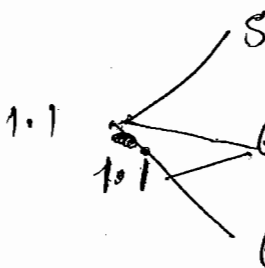
* Characteristic Properties of Digital to analog Convert
→ Different parameters of converter -

① Resolution
② Percentage Resolution
③ Full scale voltage
④ Analog voltage.

① Resolution :-

Due to Increment at 1-bit in L.S.B. change in the analog voltage the change is called as resolution.-

Eg :-



101 — 5

110 — 6

111 — 7

$$\text{Resolution} = \frac{V_r}{2^n - 1}$$

V_r → Voltage applied to corresponding to logic 1.

② Percentage Resolution :-

$$= \frac{\frac{V_r}{2^n - 1}}{V_r} \times 100\%$$

$$\% \text{ Resolution} = \frac{1}{2^n - 1} \times 100\%$$

n = no. of bits

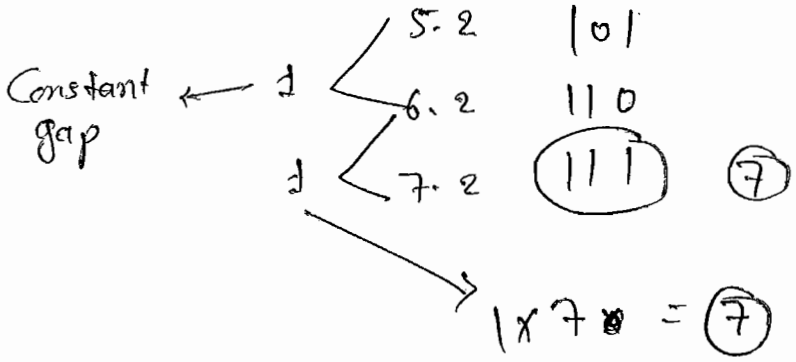
③ Full scale Voltage :-

$$V_{fs} = V_r \quad \text{(always)}$$

④ Analog Voltage :-

Analog voltage = Resolution x Decimal equivalent

Ex -



Q A digital to Analog converter having % R = 0.4, Identify number of bits involved in the conversion

Sol^n

$$\% \text{ Res} = 0.4\% = \frac{1}{2^n - 1} \times 100\%$$

$$\Rightarrow \frac{0.4}{100} = \frac{1}{2^n - 1}$$

$$\Rightarrow \frac{1000}{04} = 2^n - 1$$

$$\Rightarrow 2^n - 1 = 250$$

$$\Rightarrow 2^n = 251$$

$$\Rightarrow 2^n \approx 2^8$$

So $\boxed{n = 8}$

below no. of bits not in fraction or decimal so we write $2^{7.9} = 2^8$ in place of 251 we write 28

Q. A 8 bit Digital to analog converter having voltage applied corresponding to logic-1 = 10V Calculate

(1) R (2) % R (3) V_{fs}

(4) Calculate Analog voltage corresponding to 1110.

Soln

(1) $\text{Res.} = \frac{V_r}{2^n - 1} = \frac{10}{2^8 - 1} = \frac{10}{255} = 0.03$

Res = 0.03

(11) $\% \text{ Res.} = \frac{1}{2^n - 1} \times 100\%$

$= \frac{1}{255} \times 100 = \frac{20}{51}\%$

$= 0.39\%$

(3) $V_{fs} = V_r$

$V_{fs} = 10V$ $\because V_r = 10V$

(4)

$A = 0.03 \times 14$

$A = 0.42$

Q A 3-bit digital to analog to digital converter having applied voltage ring from -10V to +10V Calculate resolution and % Resolut.

Soln

$$R = \frac{V_r}{2^n - 1}$$

$\because V_r$ = potential difference

$$V_r = 10 - (-10) = 20\ V$$

$$\text{So} \quad R = \frac{20}{2^3 - 1} = \frac{20}{8 - 1} = \frac{20}{7}$$

$$\boxed{R = 2.8}$$

$$\% R = \frac{1}{2^3 - 1} \times 100\ \%$$

$$= \frac{1}{7} \times 100$$

$$\boxed{R = 14.2\ \%}$$

Q.93

Soln

$$R = \frac{1}{2^n - 1}$$

$$= \frac{1}{2^6 - 1} = \frac{1}{64 - 1} = \frac{1}{63}$$

$$R = 0.01587$$

$$A = R \times 20$$

$$= 0.01587 \times 20$$

$$A = 0.3174$$

If $V_r = 10$

$$R = \frac{10}{2^6 - 1} = \frac{10}{63} = 3.17$$

$$A = \frac{10}{63} \times 20 = \frac{200}{63}$$

$$A = 63.49.$$

Q.33 The high input impedance of field effect transistor (FET) amplifier is due to.

(a) The pinch-off voltage (b) Its very low gate current

(c) The source and drain being far apart (d) The geometry of the FET

Q.

Modulation

$f(x) \rightleftharpoons F(X)$ (it 10k)

$f(x)\cos w_0 x \rightleftharpoons \frac{1}{2}[F(X-w_0)+F(X+w_0)]$

w_0: 2k; $X-w_0$: 8k; $X+w_0$: 12k ↑ generally consider.

$$\text{Power} = \frac{\text{Energy}}{\text{Time}}$$

$$\uparrow \text{Power} = \text{Energy} \times \text{Frequency} \uparrow$$

* Modulation is used to increase the strength of signal so that it can travel large distance into the space (wireless communication).

Q. 19

Soln

$X = 7\ MHz$

$w_0 = 10K\ Hz$

or

$w_0 = 0.01MHz$

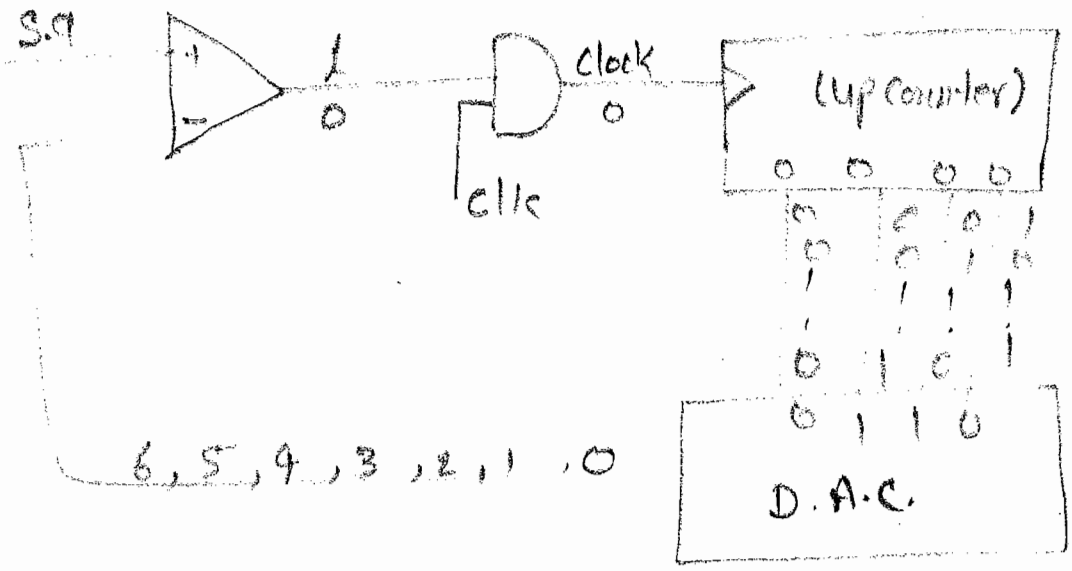
So $= X - w_0$ to $X + w_0$

$= 7 - 0.01$ to $7 + 0.01$

$= 6.99$ to 7.01 Ans

Analog to Digital Converter

* Counter type Converter :-



When all the difference of comparator is +ve, output assumed as 1. Clock will enter into the counter, Count sequence increases.

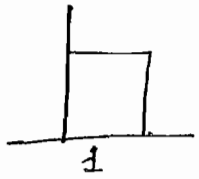
When the difference of op-amp becomes -ve output becomes zero. Clock will stop entering into the counter. The Binary value at which counter stop that will be considered as digital output for the applied analog output.

* When applied voltage is 1 V (~ 0.9 V) then minimum clock pulse required is one.

⇒ **maximum number of clock pulse required = $2^n - 1$.**

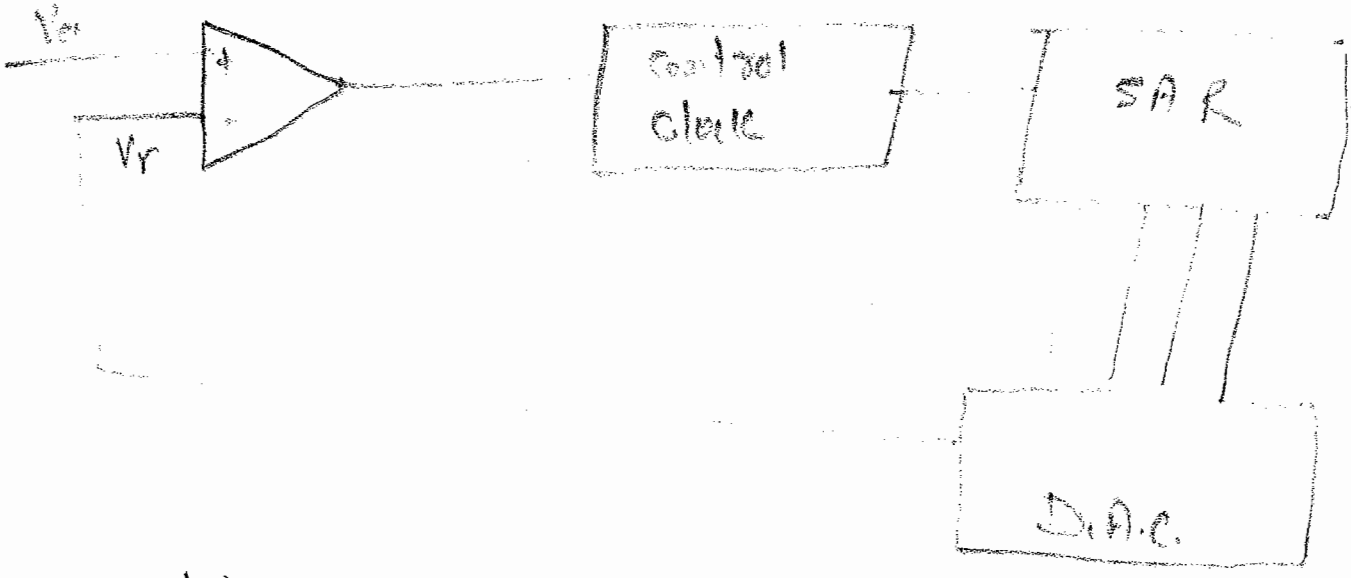
⇒ Minimum conversion time = 1 x T clock

⇒ Maximum = $(2^n - 1) \times$ T clock.



(Memorize)

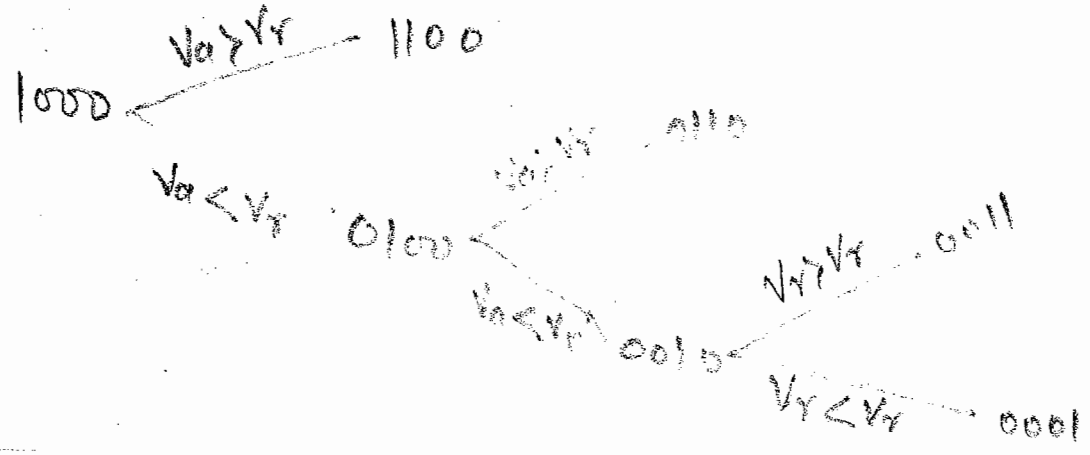
* Successive Approximation type Converter :-



Whenever difference of op-Amp either +ve or negative register will perform shift operation but control circuit is designed in such a way that when difference is 1 during shifting the previous bit which was a 1 will be kept as it is, when difference is zero (-ve) during shifting operation the previous bit which was set (1) becomes reset (0).

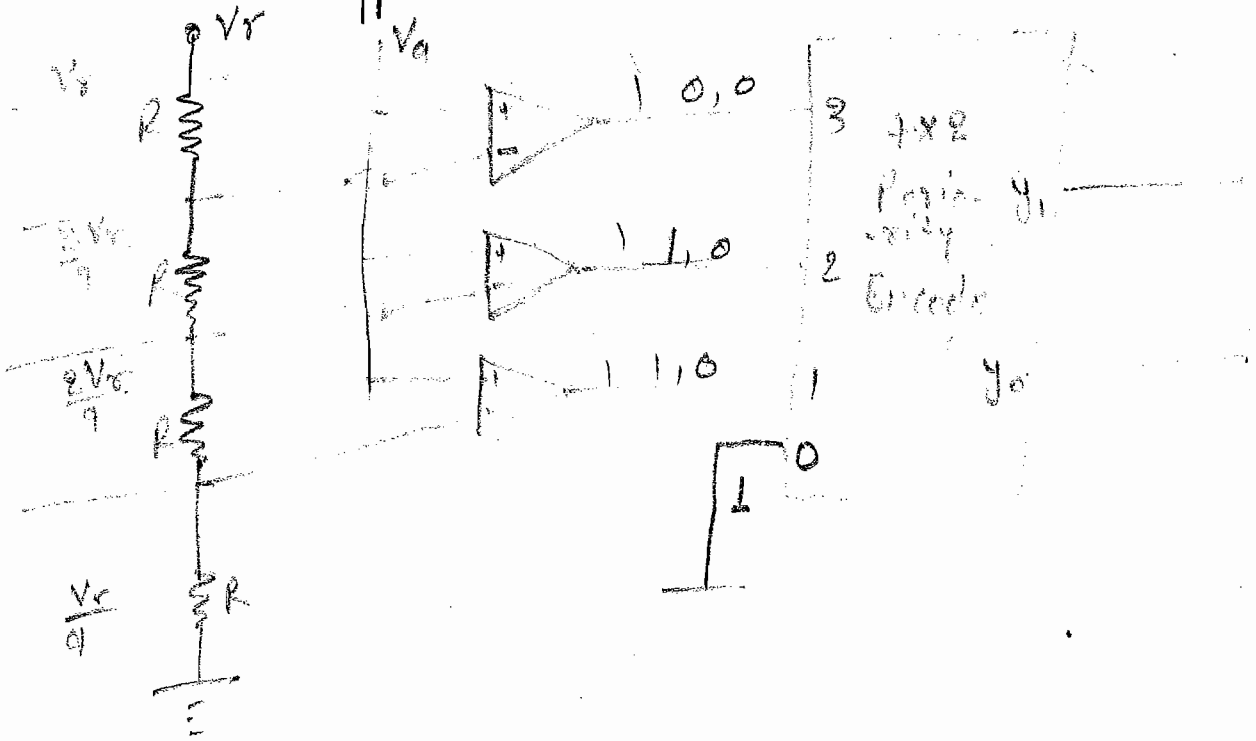
⇒ S.A.R. type converter is independent of applied voltage only depends on number of bits.

No. of Clock pulse required = n



maximum conversion time = $n \times T_{clk}$

* Flash Type Converter :-



Number of used registers $= 2^n$

n = no. of bits

No. of 6 register = 2 (for 2-bit.)

No. of Comparators (op-amp) $= (2^n - 1)$

(99) (9)

79 remains unchanged.

i/p	y_1	y_0
$V_a < V_r/4$	0	0
$\frac{V_r}{4} < V_a < \frac{V_r}{2}$	0	1
$\frac{V_r}{2} < V_a < \frac{3V_r}{4}$	1	0
$V_a > \frac{3V_r}{4}$	1	1

fastest converter (flash type) required only one clock pulse." It is fastest converter but it is ~~fast~~ much expensive?.

No. of clock pulse = 1.

Maximum Conversion time = 1 X Tclock

Converter	no. of clock pulse
Counter type	min = 1 max^m = $2^n - 1$
SAR Type	n
Flash - type	1
Dual Slope	2^{n+1}

Q. A 12-bit converter (ADC), time period of one clock pulse 12 μsec its maximum conversion time is 14 μsec. then the type of converter may be-?

(a) Counter type (b) SAR type

(c) Flash type [✓] (d) Dual slope type.

Sol^n T_{clk} = 12 ps

n = 12

max^m Conv = 14 μsec.

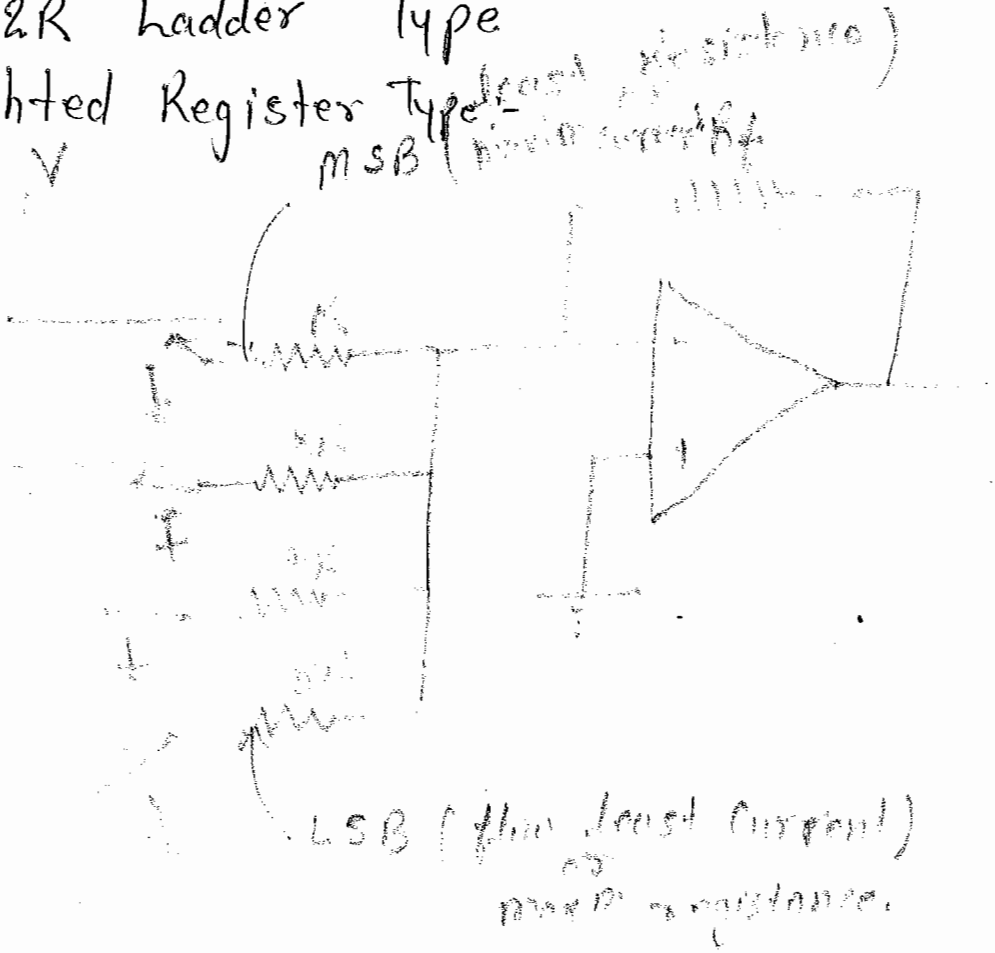
1 X 12 = 12 μsec ≈ 14 μsec. Ans

* Digital to Analog Converter :-

(1) Weighted Register Type

(2) R-2R Ladder Type

(1) Weighted Register Type :-



The branch which is having minimum current represent L.S.B., for maximum branch current represents M.S.B.

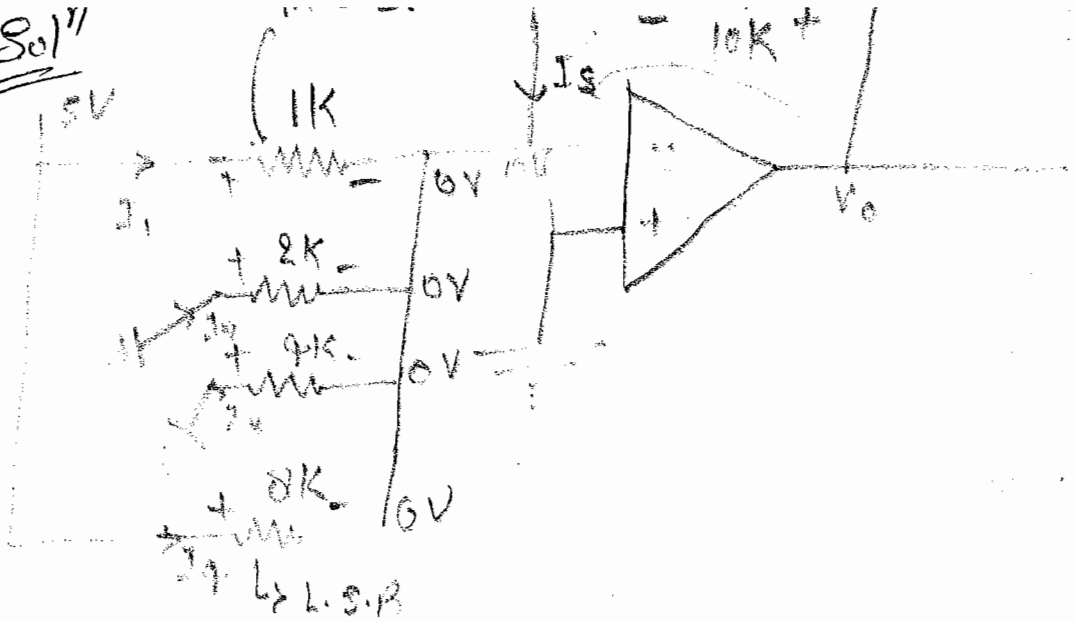
Value of maximum registance = $2^{(n-1)}$

Q. for the given op-amp network shown if the minimum value of registance is 1 kΩ identify current flowing through -

(I) M.S.B. (II) L.S.B. (III) o/p voltage.

(IV) Identify the binary value corresponding to which o/p is calculated.

Sol'n



$$I_{MSB} = \frac{5-0}{1K} = 5\ m.A.$$

$$\boxed{I_{MSB} = 5\ m.A.}$$

$$I_{LSB} = \frac{5-0}{8} = \frac{5}{8} = 0.625\ m.A.$$

$$\boxed{I_{LSB} = 0.625\ m.A.}$$

$$I_1 + I_2 + I_3 + I_4 + I_S = 0$$

$$5\ m.A. + 0.625 + \frac{V_0 - 0}{10K} = 0$$

$$\frac{V_0}{10} = -5.625\ m.A.$$

$$\boxed{V_0 = -56.25V}$$

MSB LSB

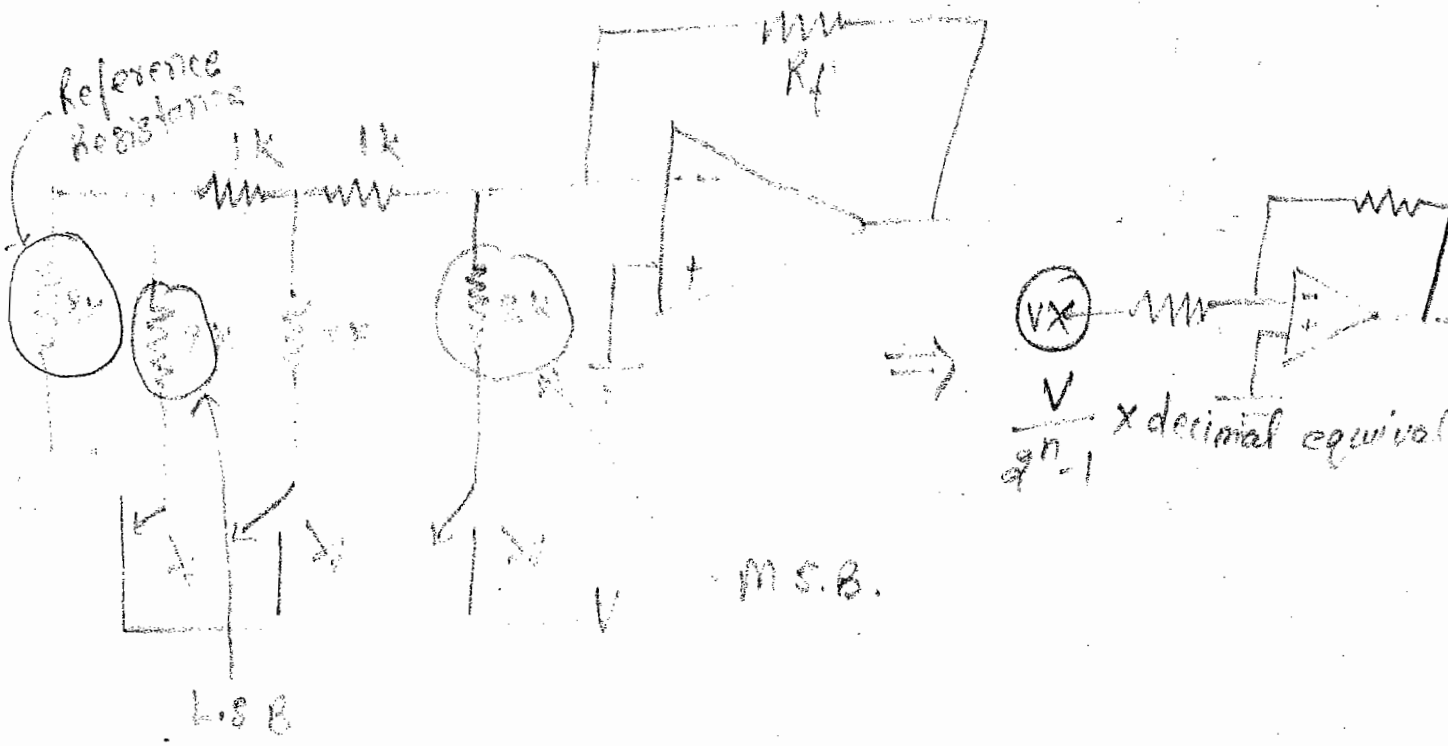
1 0 0 1

↓ ↓

(5V) (5V)

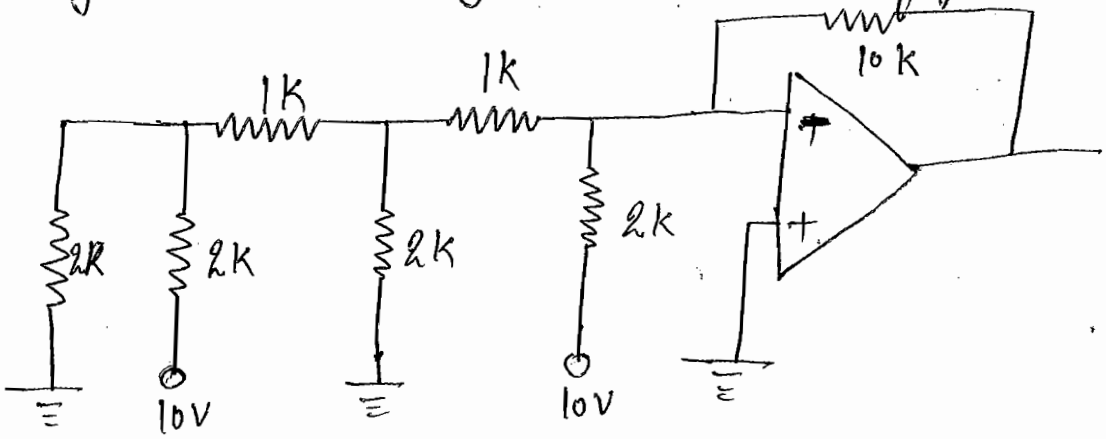
= 9

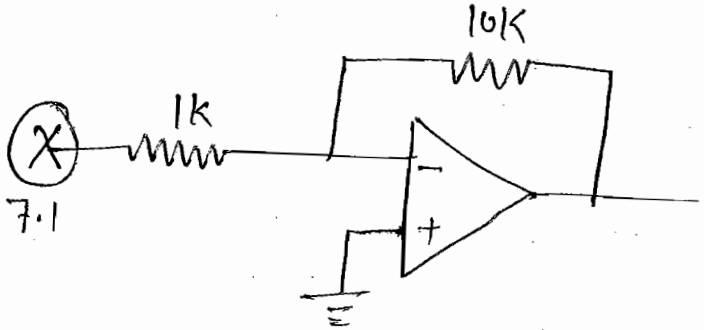
(4.) R-2R Ladder Network :-



Decimal voltage = $\frac{V}{2^{n}-1}$ x decimal equi.

Q. For the given circuit diagram calculate the analog o/p voltage shown in figure.





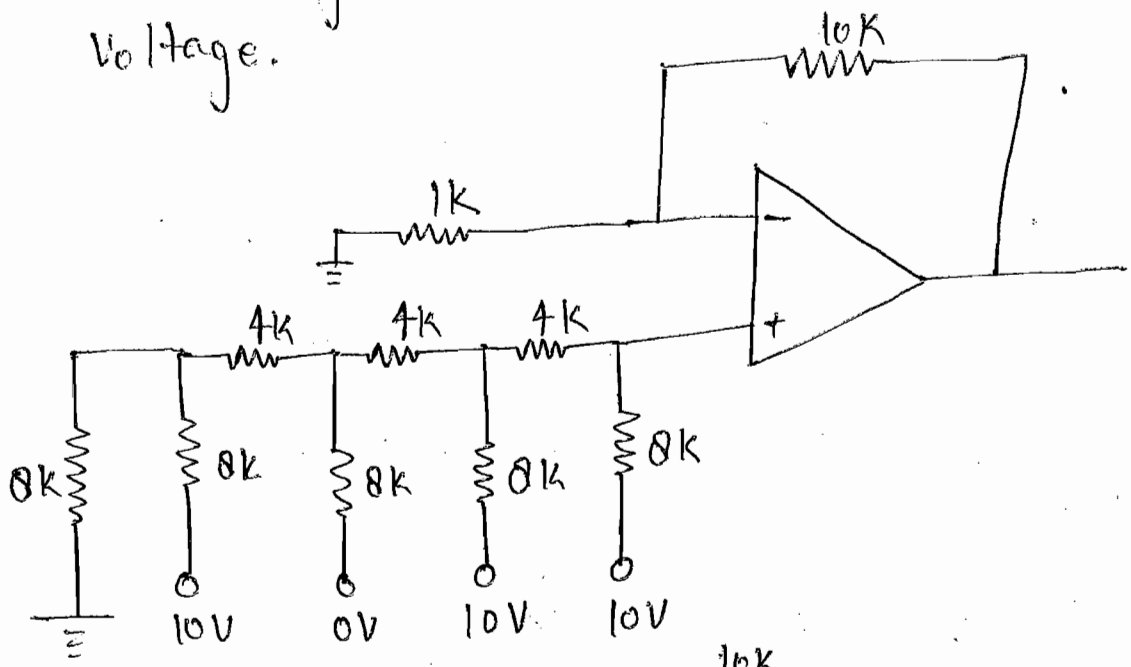
$$V = \frac{10}{2^3-1} \times 5 = \frac{50}{7} = 7.1V.$$

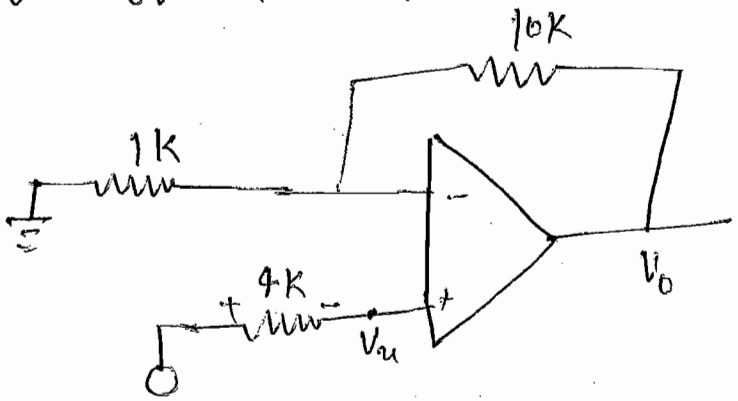
$$\frac{V_0}{7.1} = -\frac{R_f}{R_1}$$

$$\frac{V_0}{7.1} = \frac{-10k}{1k}$$

$$\boxed{V_0 = -71V}$$

Q. for the given network calculate analog o/p voltage.





$\frac{V_r}{2^n-1}$ x decimal equivalent.

$$V = \frac{10}{2^4-1} \times 13 = \frac{10}{15} \times 13 = \frac{130}{15} = 8.6V.$$

$$\boxed{V = 8.6V}$$

$$\frac{0.6 - V_a}{4k} = I \approx 0$$

$$\boxed{V_a = 0.6\ V}$$

$$I_1 + I_2 = 0$$

$$\frac{0 - 0.6}{1k} + \frac{V_0 - 0.6}{10k} = 0$$

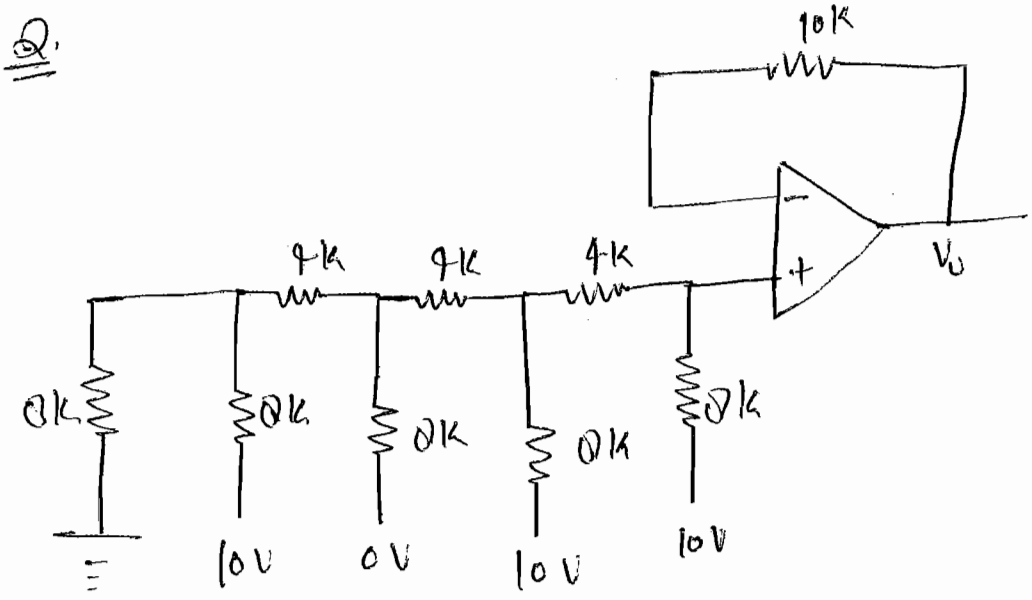
$$\frac{V_0 - 0.6}{10} = 0.6$$

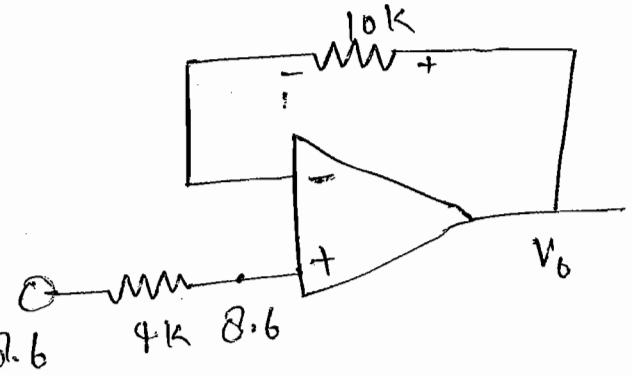
$$V_0 - 0.6 = 06$$

$$V_0 = 06 + 0.6$$

$$\boxed{V_0 = 94.6\ V}$$ Ans

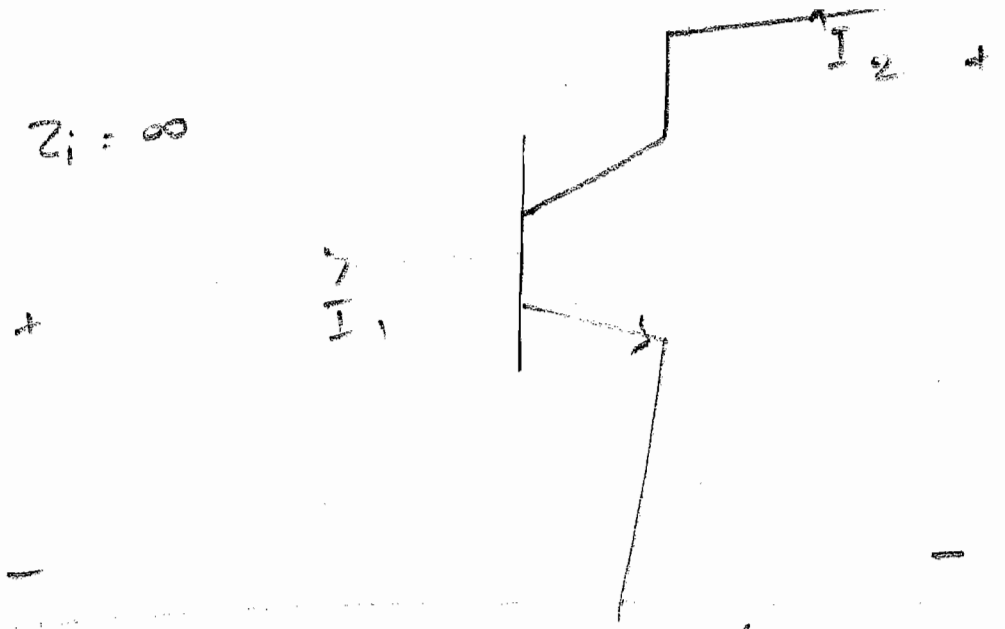
Q.





$$\frac{V_0 - 0.6}{K} = 0$$

$$\boxed{V_0 = 0.6\ V}$$



$V_1 = f(I_1, V_2)$ — (1)

$I_2 = f(I_1, V_2)$ — (2)

$\frac{I_c}{I_B} = \beta$

$I_c = \beta I_B$

$I_2 = \beta I_1$

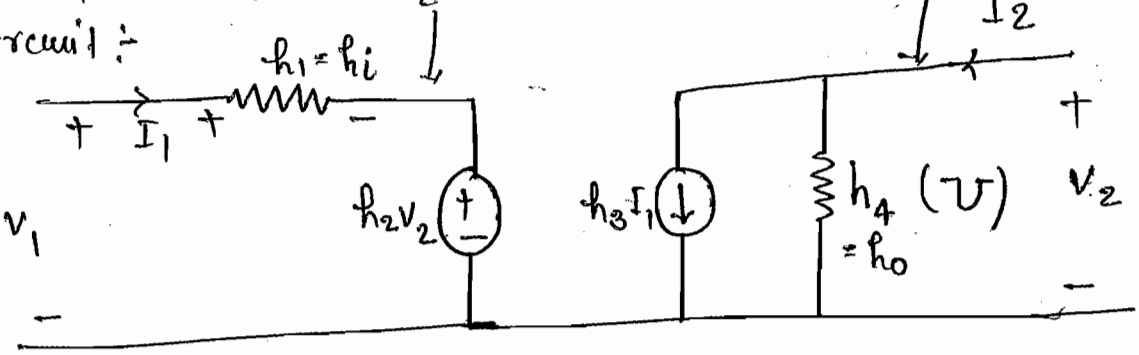
Now $V_1 = h_1 I_1 + h_2 V_2$ — (*)

$I_2 = h_3 I_1 + h_4 V_2$ — (**)

$\Rightarrow -V_1 + h_1 I_1 + h_2 V_2 = 0$

$I_2 = h_3 I_1 + h_4 V_2$

So, Draw circuit :-



$\because V_1 = h_1 I_1 + h_2 V_2$

$I_2 = h_3 I_1 + h_4 V_2$

When o/p voltage = 0 means $\boxed{V_2 = 0}$

then, $\boxed{h_1 = \frac{V_1}{I_1} = h_i}$

$h_3 = \frac{I_2}{I_1}$ means it is gain (constant) = h_f

forward gain

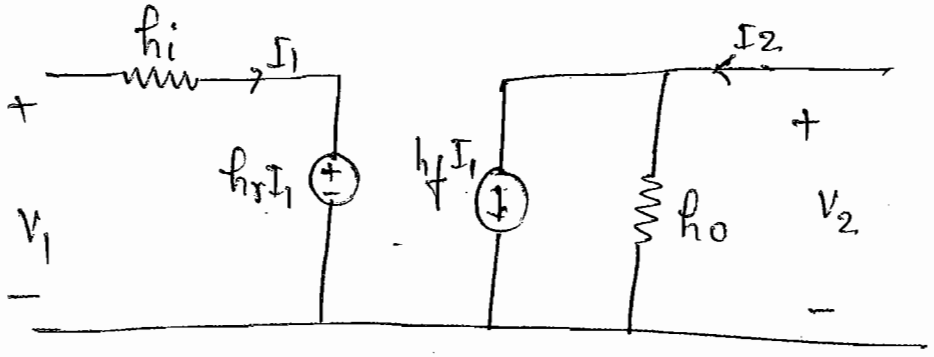
$$I_1 = 0$$

$$V_1 = h_2 V_2$$

$$h_2 = \frac{V_1}{V_2} = h_r = \text{Reverse voltage gain.}$$

$$\Rightarrow \quad I_2 = h_4 V_2$$

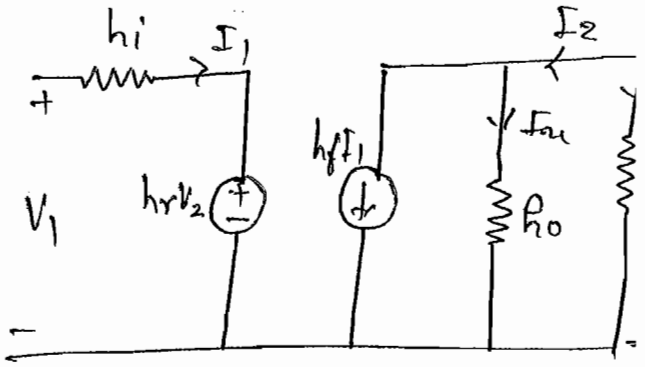
$$h_4 = \frac{I_2}{V_2} = h_o =$$



	CE	C.C.	CB
h_i	h_{ie}	h_{ic}	h_{ib}
h_r	h_{re}	h_{rc}	h_{rb}
h_f	h_{fe}	h_{fc}	h_{fb}
h_o	h_{oe}	h_{oc}	h_{ob}

A_F, A_I, R_{in}, R_{out} → then we can not apply loop we can apply above steps.

* Current Gain :-



A_I = Current gain

$$\boxed{I_L = -I_2}$$

$$V_2 = I_L R_L$$

$$\boxed{V_2 = -I_2 R_L}$$

$$I_2 = h_f I_1 + I_2$$

$$I_2 = h_f I_1 + V_2 h_o$$

$$I_2 = h_f I_1 - I_2 \cdot R_c h_o$$

$$I_2 + I_2 h_o R_i = h_f I_1$$

$$I_2 [1 + h_o R_i] = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_i}$$

$$\boxed{\frac{I_L}{I_f} = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o R_i}}$$

* Input Resistance :-

$$-V_1 + I_2 h_i + h_r V_2 = 0$$

$$V_1 = h_i I_1 + h_r V_2$$

Now divided by I_1

$$\frac{V_1}{I_1} = h_i + h_r \frac{V_2}{I_1}$$

$$\frac{V_1}{I_1} = h_i + h_r \left(\frac{I_2}{I_1}\right) R_L$$

$$R_{in} = \frac{V_1}{I_1} = h_i + h_r A_I R_L$$

* Voltage Gain (A_V) :-

$$V = IR$$

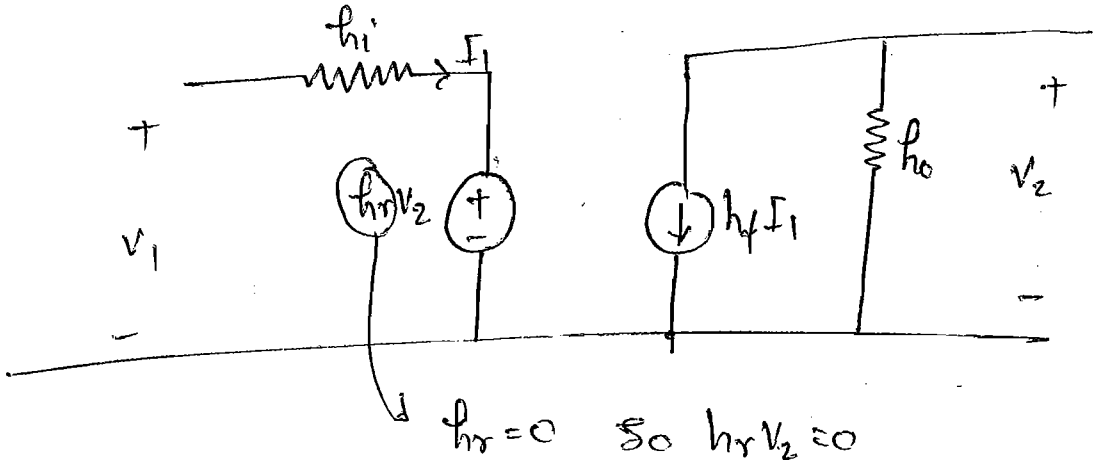
$$A_V = A_I R_g$$

So $$A_V = A_I + \frac{R_L}{R_{in}}$$

* Output Resistance :-

$$R_o = \frac{1}{h_o}$$

Equivalent diagram :-



$h_r = 0$ So $h_r V_2 = 0$

$$A_I = \frac{-h_f}{1+h} = -h_f$$

$$R_{in} = h_i$$

$$A_V = \frac{A_I R_L}{R_{in}}$$

$$R_o = \frac{1}{h_o}$$

Steps of A.C. Analysis :-

(1) Ground all the DC sources.

(2) Short all the capaciter

(3) Draw the equivalent diagram for the calculation of equivalent load resistance. and use that R_L in circuit analysis.

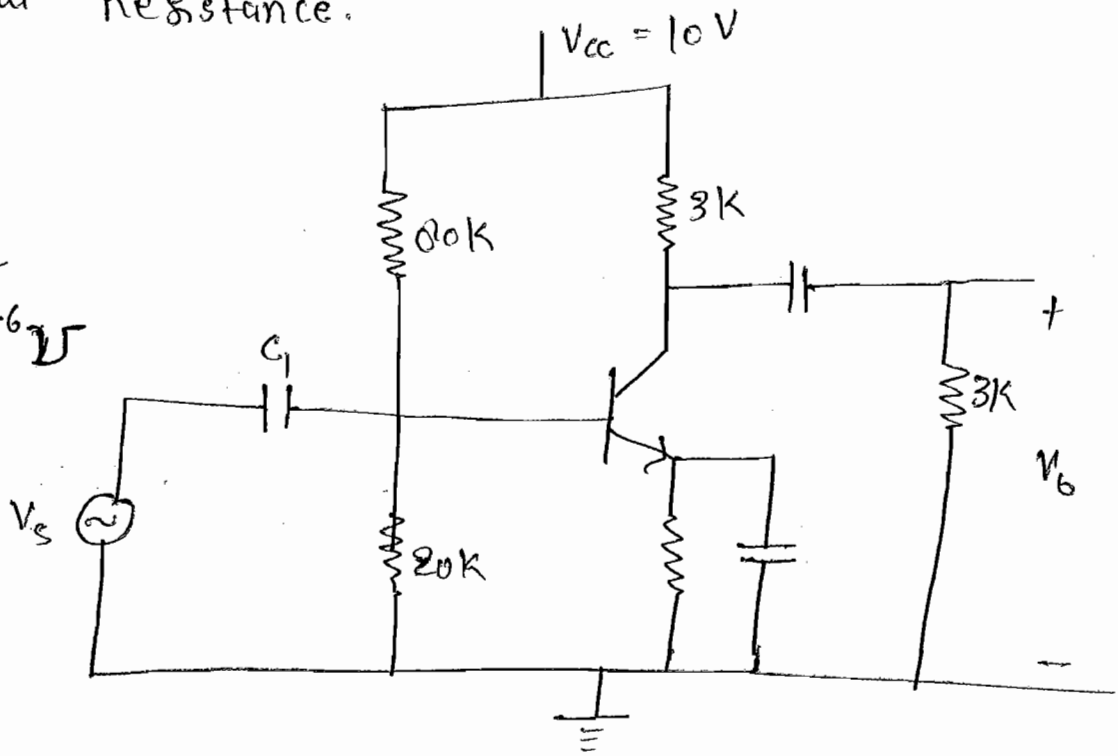
Q. for the given circuit ~~or~~ diagram Calculate - Current gain, voltage gain, input Resistance and Output Resistance.

$h_{ie} = 2k$

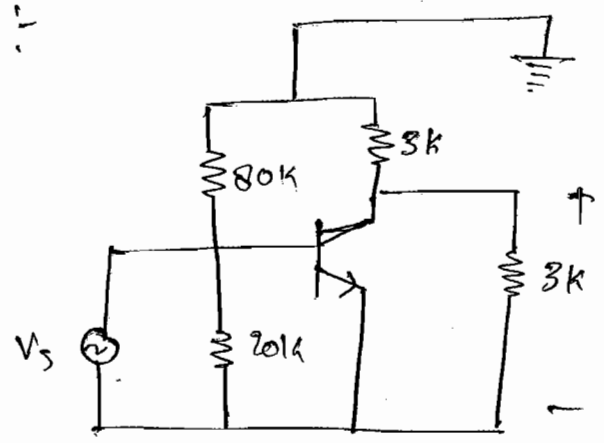
$h_{fe} = 100$

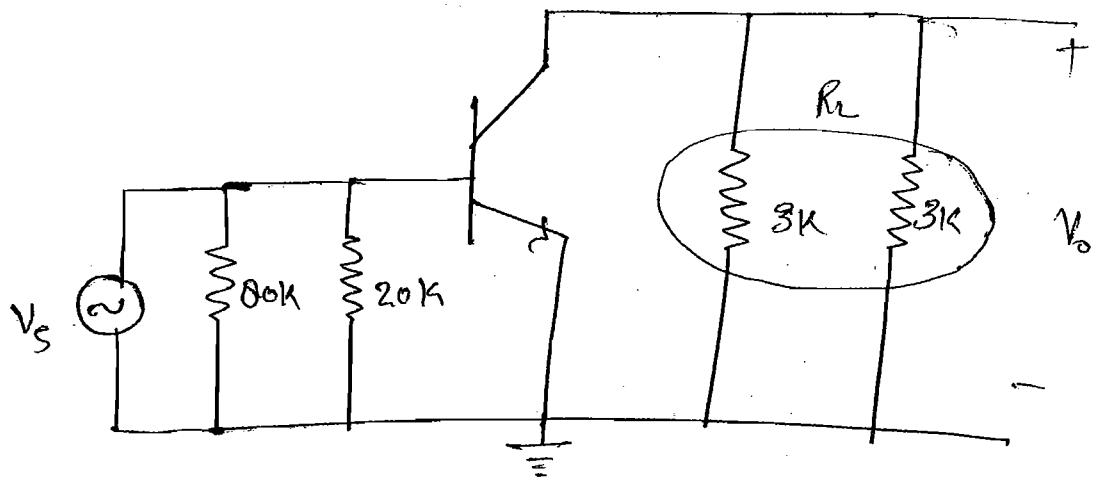
$h_{re} = 2 \times 10^{-4}$

$h_{oe} = 2 \times 10^{-6} \mho$



Sol'n Equivalent diagram :-





$$A_I = -h_{fe} = -100$$

$$R_{in} = 2k = h_{ie}$$

$$A_V = A_I \frac{R_L}{R_{in}}$$

$$A_V = -100 \times \frac{1.5k}{2k} = -75$$

$$R_o = \frac{1}{h_{oe}} = \frac{1}{2\times10^{-6}} =$$

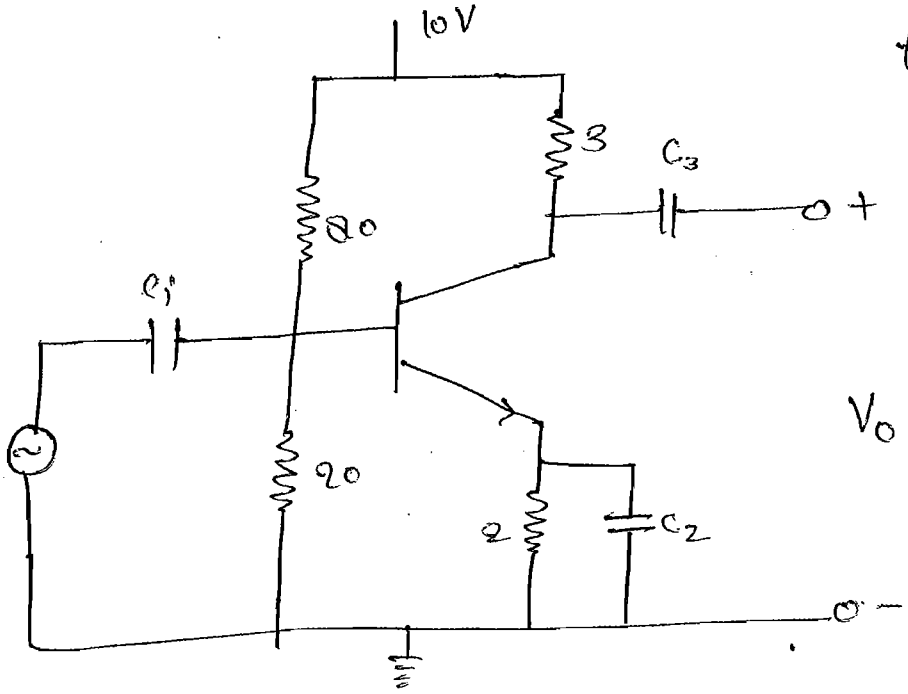
Now from equations -

$$R_{in} = h_{ie} + h_{re} \times A_I \times R$$

$$= 2k + (2\times10^{-4}) \times (-100) \times 1.5$$

$$R_{in} = 2 -$$

Q. For the given circuit diagram determine input Resistance, Output resistance, Current gain, Voltage gain.



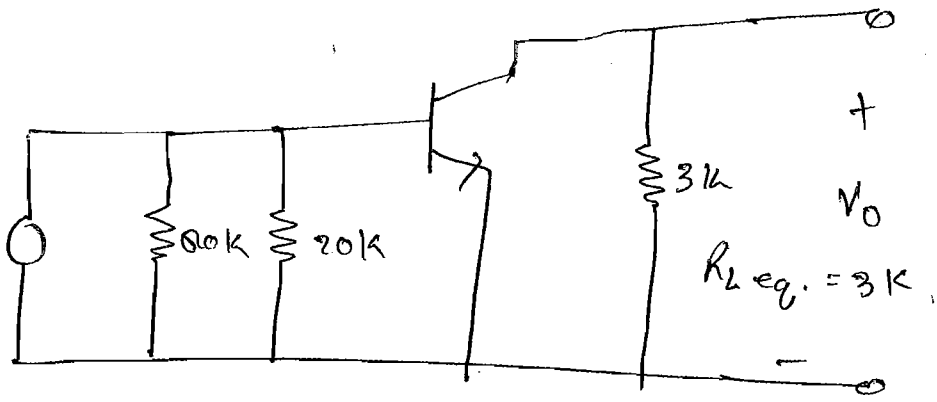
$h_{ie} = 1.5K$

$h_{fe} = 200$

$h_{re} = 2 \times 10^{-5}$

$h_{oe} = 2 \times 10^{-6} \mho$

Sol^n



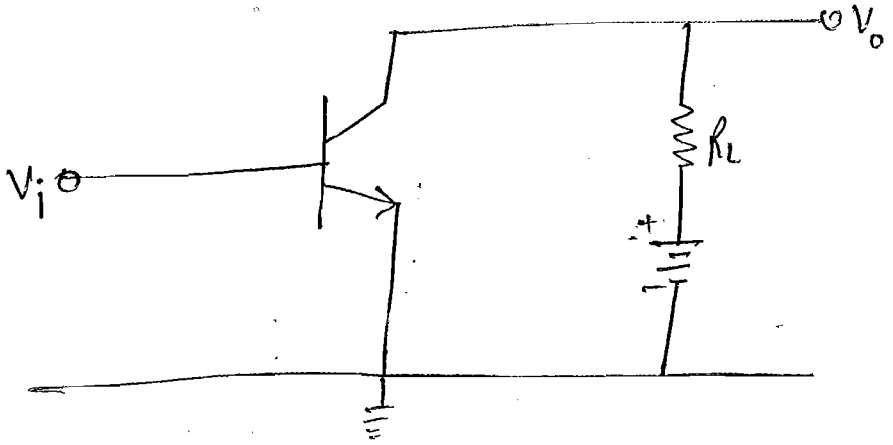
$$A_I = -h_{fe} = -200$$

$$h_{ie} = 1.5 = R_{in}$$

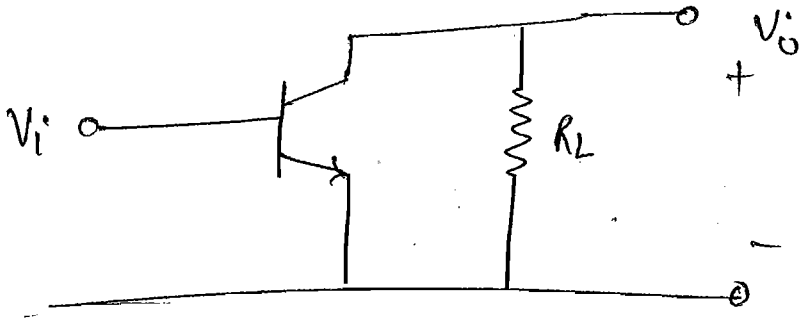
$$A_V = A_I \frac{R_L}{R_{in}} = -200 \times \frac{3}{1.5} = -400$$

$$R_o = \frac{1}{2 \times 10^{-6}} = 0.5\,\Omega$$

Q.10



Soln



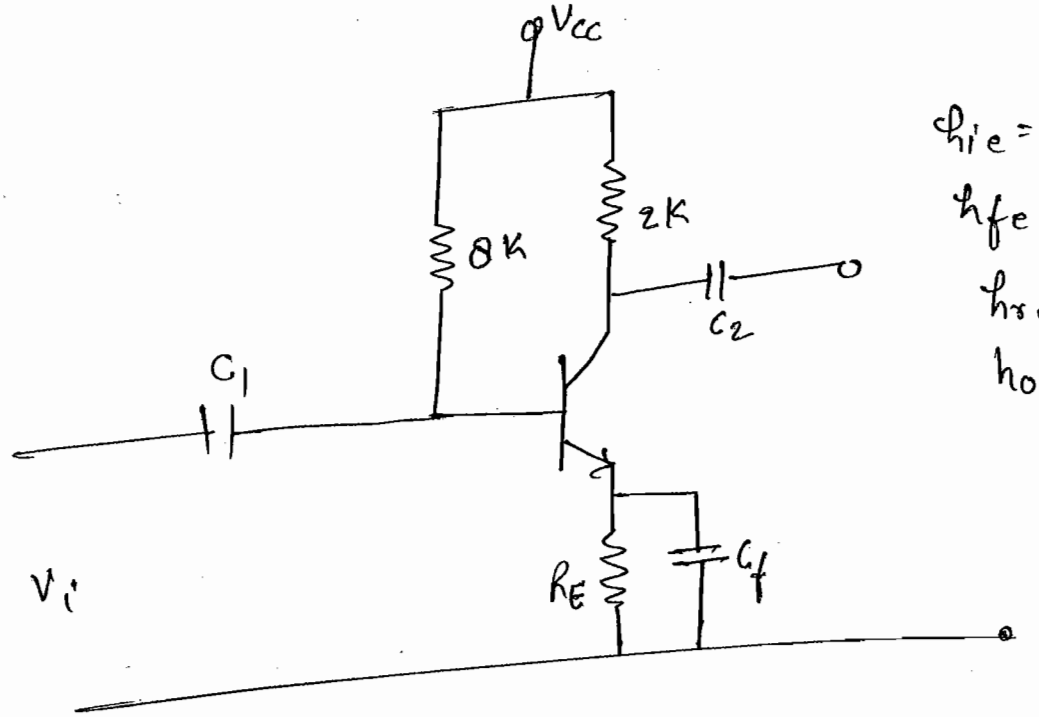
$$A_I = -35 = -h_{fe}$$

$$A_V = A_I \cdot \frac{R_L}{R_{in}} = -35 \times \frac{1000}{1000}$$

$$A_V = -35$$

2. For the given circuit diagram Calculate Current gain, voltage gain, input ~~current~~, resistance, output resistance

Soln



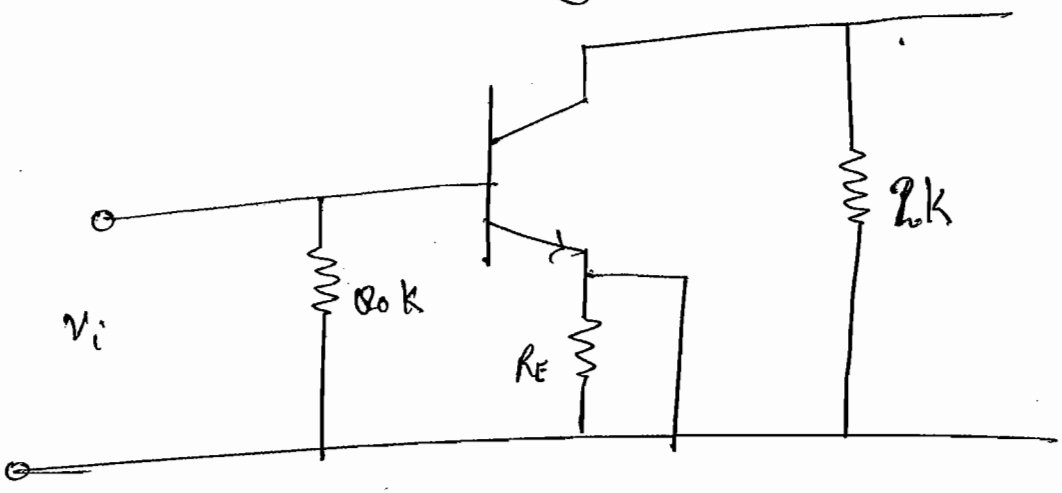
$h_{ie} = 2K$

$h_{fe} = 180$

$h_{re} = 0$

$h_{oe} = 0$

Equivalent circuit diagram -



$$A_I = -h_{fe}$$

$$A_I = -100$$

$$R_{in} = h_{ie} = 2K$$

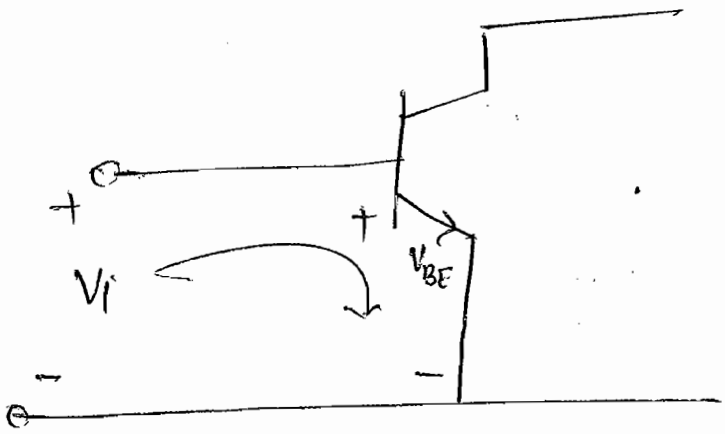
$$A_V = A_I \frac{R_L}{R_{in}}$$

$$= -150 \times \frac{2}{2}$$

$$A_V = -150$$

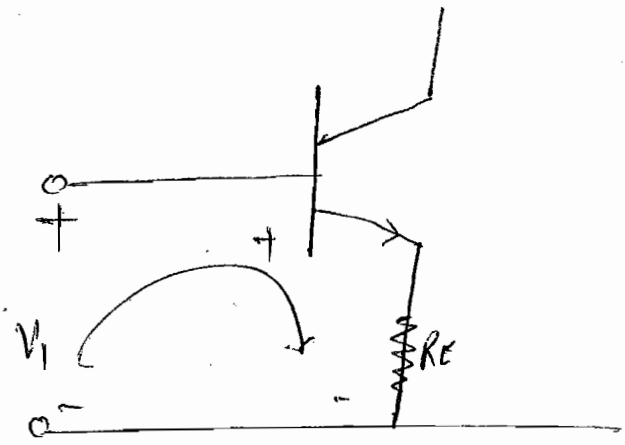
$$R_o = \frac{1}{h_o} = \infty$$

* Effect of R_E in the circuit :-



$$-V_i + V_{BE} = 0$$

$$\boxed{V_i = V_{BE}}$$

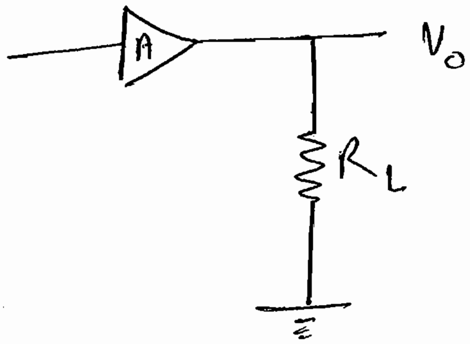


$$-V_i + V_{BE} + I_E R_E = 0$$

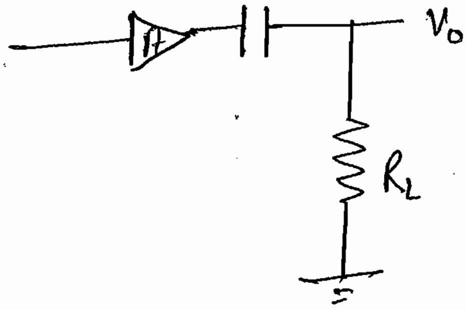
$$\boxed{V_{BE} = V_i - I_E R_E}$$ ← Negative feedback.

- The presence of emmiter resister creats negative feedback.
- The presence of emmitter resister in circuit reduces the overall voltage gain because it decreases the capability of transister to reach cut-in voltage.

* RC - Coupled Amplifier :-



Direct.



RC - Coupled

When the output of (op-amp) any amp. directly connected with resistance (Load) then it is called Direct coupled amplifier.

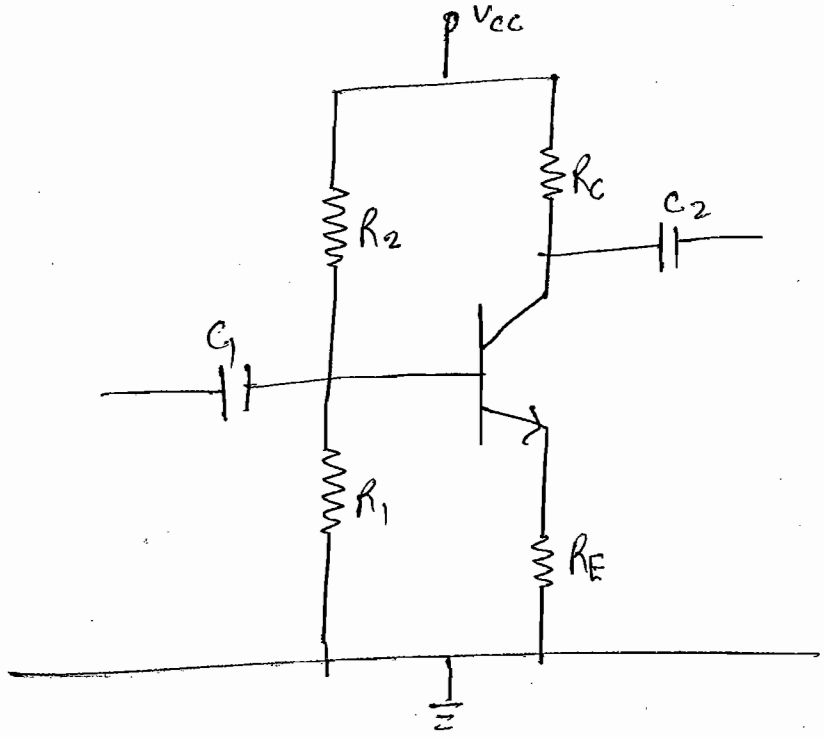
When the output of any amp. connected with load via capacitor then it is called RC - Coupled amplifier.

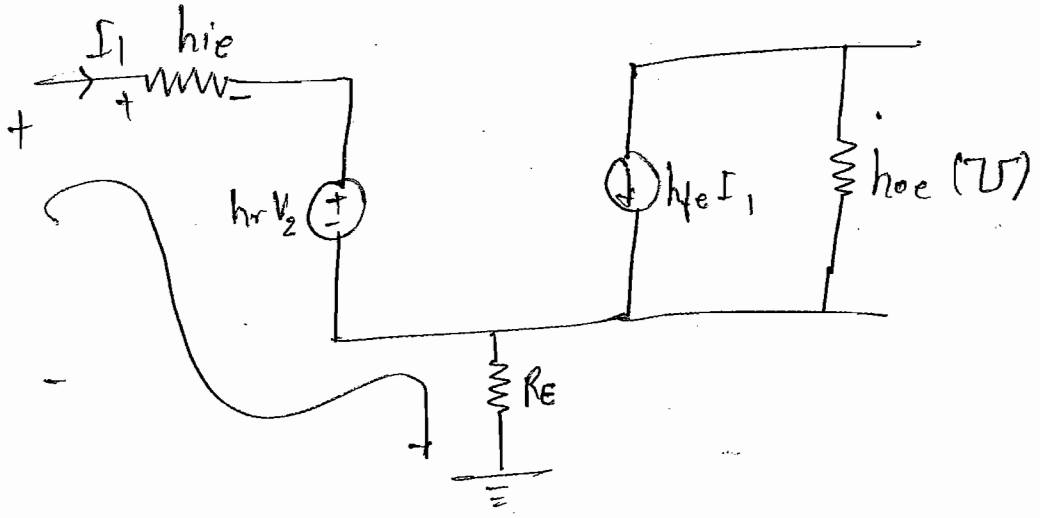
In direct coupled amplifier output may contain d.c. and a.c. But in RC Coupled amplifier output contains only a.c. becoz capacitor blocks d.c. hence called as blocking capacitor.

$$X_c = \frac{1}{wC}$$

for d.c. $X_c = \infty$, $f = 0$

for a.c. ...





$$-V_1 + I_1 h_{ie} + h_{re} V_2 + I_E R_E = 0$$

$\because$ here $h_{re} \approx$ very less ≈ 0

So $h_{re} V_2 \approx 0$

$$V_1 = h_{ie} I_1 + (I_B + I_C) R_E$$

$$V_1 = h_{ie} I_B + (I_B + I_C) R_E$$

$$V_1 = I_B h_{ie} + (I_B + \beta I_B) R_E$$

$$V_1 = I_B [h_{ie} + (1+\beta) R_E]$$

$$\frac{V_1}{I_B} = h_{ie} + (1+\beta) R_E$$

$$R_{in} = h_{ie} + (1+\beta) R_E$$

$\therefore$ $\uparrow R_{in}$

$$A_V = A_I \frac{R_L}{R_{in}\uparrow}$$ $\therefore$ $A_V \downarrow$

With C_E	without C_E
$R_{in} = h_{ie}$	$h_{ie} + (1+\beta) R_E = R_{in}$

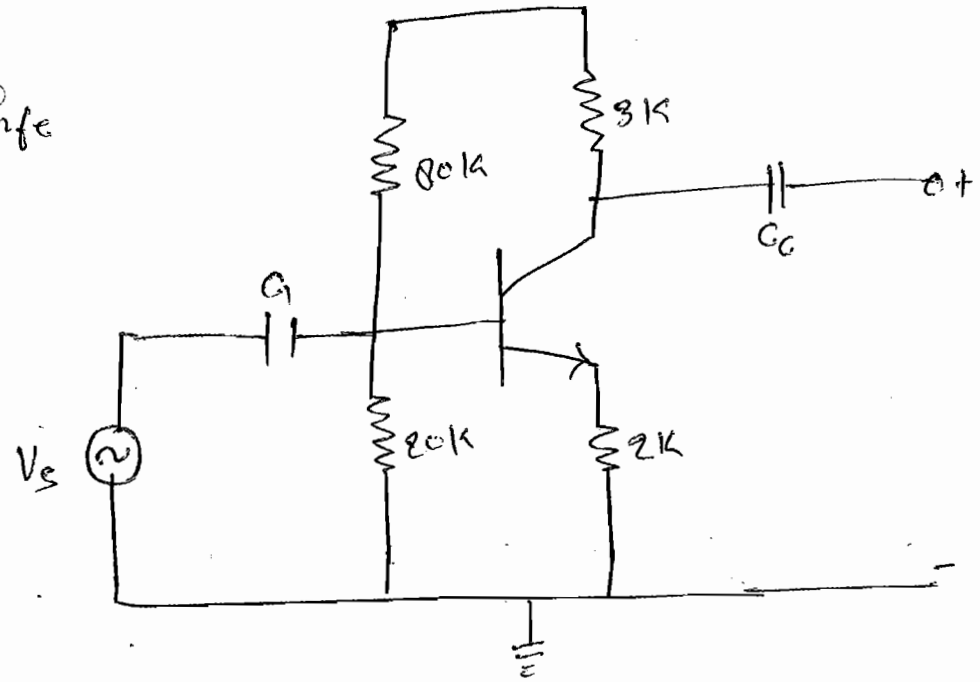
Q. for the given circuit diagram calculate A_V, A_I, R_{in}, R_o

$h_{ie} = 2k$

$\beta = 100 = h_{fe}$

$h_{oc} = 0$

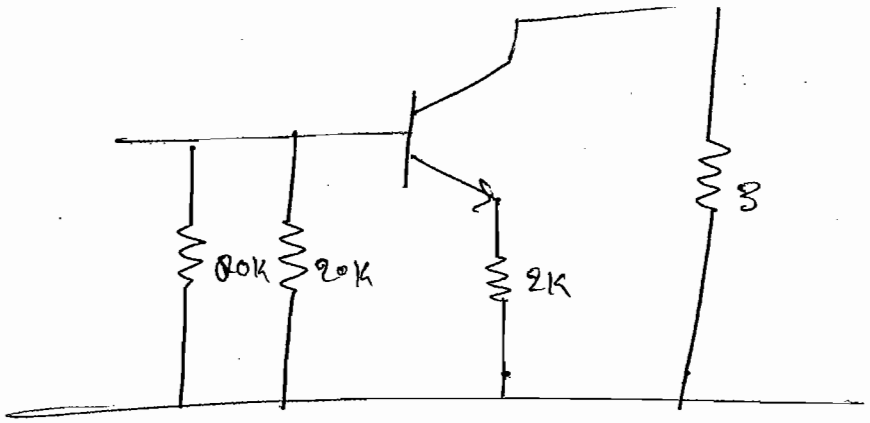
$h_{re} = 0$



Soln

$$\frac{I_2}{I_1} = h_{fe} = \frac{I_c}{I_B} = \beta$$

$$\beta = h_{fe}$$



$$A_I = -h_{fe} = -100$$

$$R_{in} = h_{ie} + R_E(1+\beta)$$

$$= 2K + 2K(100+1)$$

$$= 204\ K$$

$$A_V = A_I \times \frac{R_L}{R_{in}}$$

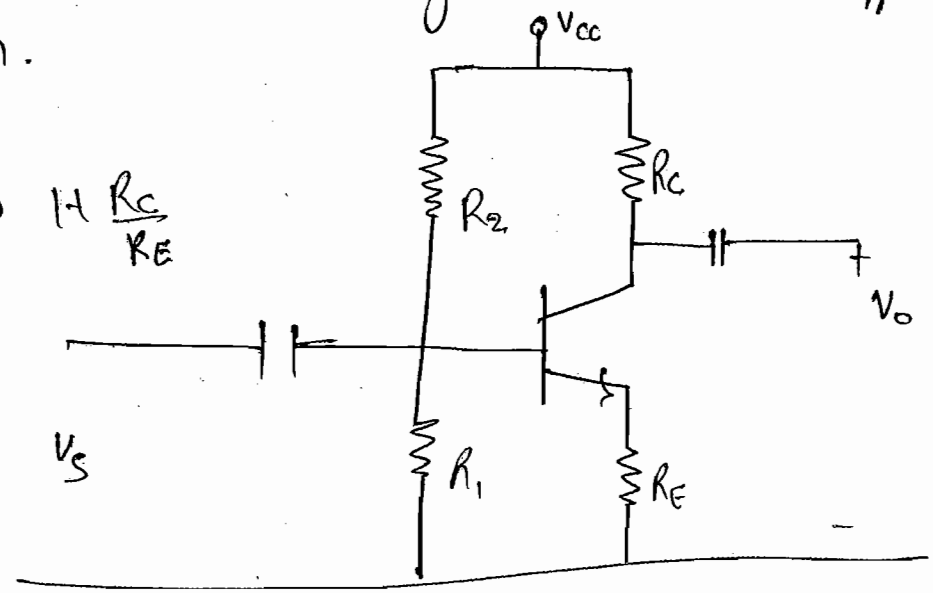
$$= -100 \times \frac{2}{204}$$

$$A_V =$$

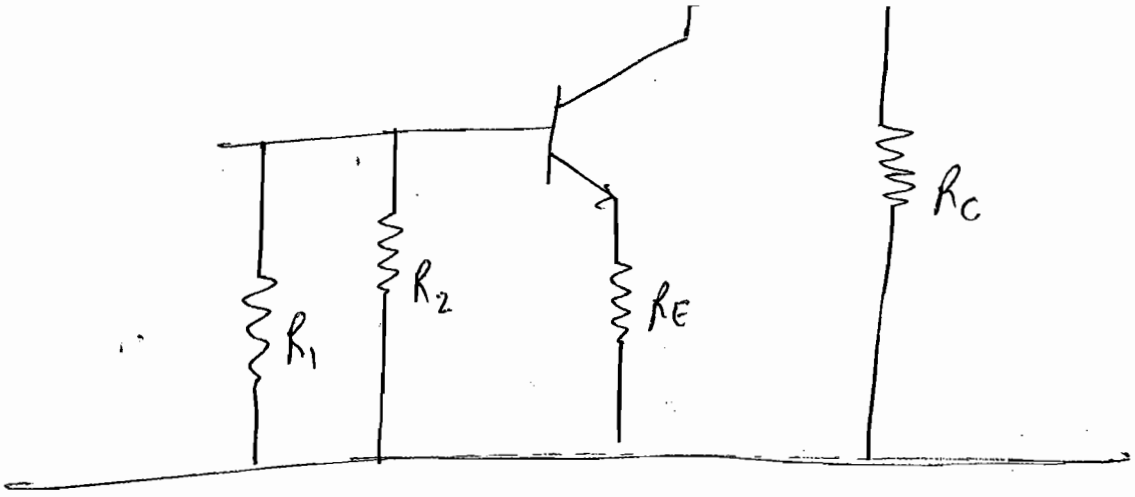
Q. For the given circuit diagram determine approximate voltage gain.

(a) $-\frac{R_C}{R_E}$ (b) $1+\frac{R_C}{R_E}$

(c) $\frac{R_C \| R_E}{2}$ (d) $-\frac{(R_C \| R_E)}{2}$



Soln



$$A_V = A_I \frac{R_L}{R_{in}}$$

$$A_V = \frac{-\beta R_C}{R_E(1+\beta) + h_{ie}}$$

$$R_{in} = R_E(1+\beta) + h_{ie}$$

$$A_I = -\beta = -h_{fe}$$

$$R_L = R_C$$

$\beta >>>$

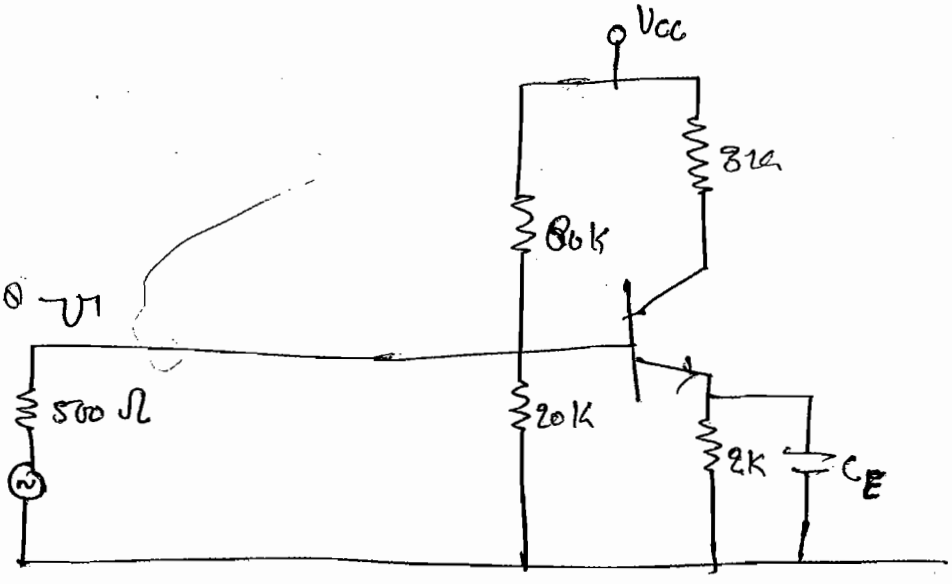
$$A_V = \frac{-\beta R_C}{h_{ie}} = -\frac{\beta . R_C}{R_E} = -\frac{R_C}{R_E}$$

Q. For the given circuit diagram calculate (impedance) overall input resistance and overall output resistance.

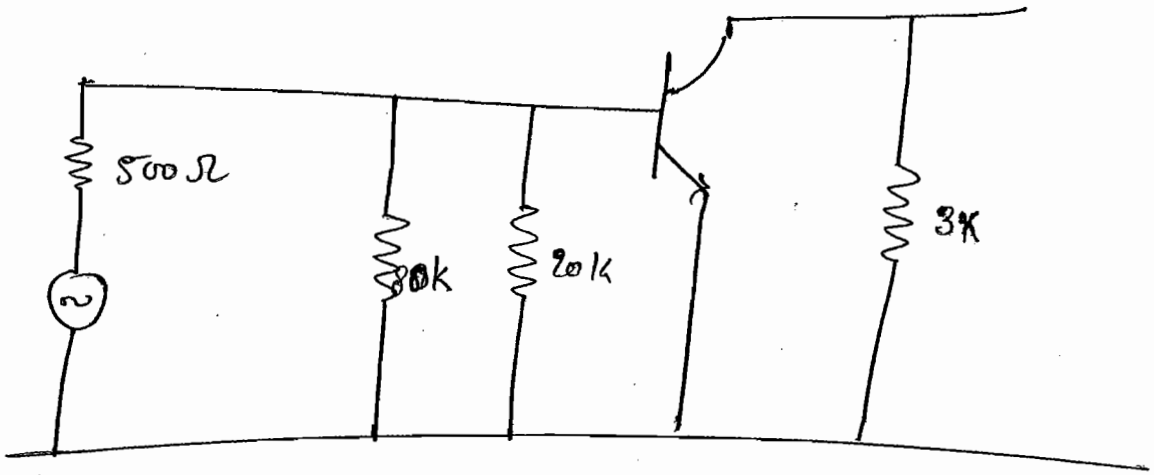
$h_{ie} = 2$

$h_{fe} = 100$

$h_{re} = 2 \times 10^{-6}$ V



Equivalent



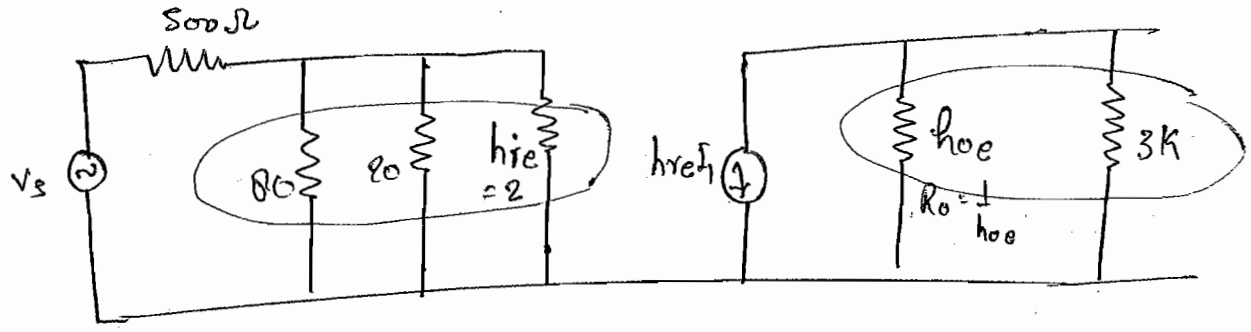
$A_I = -h_{fe} = -100$

$R_{in} = h_{ie} = 2K$

$A_V = A_I \frac{R_L}{R_{in}} = -100 \times \frac{3}{2}$

$= -150\,\Omega$

$R_L = 0.5\,m\,\Omega$



overall input Resistance. $= \frac{80 \times 20}{80+20} = \frac{1600}{100} = 16\,K\Omega +$

$= \frac{16 \times 2}{16+2} = \frac{32}{18} = 1.7 \Omega + 500\,\Omega$

$= 0.5 + 1.7 = 2.2\,K\Omega.$

Overall output resistance -

$$= \frac{0.5 \times 3}{0.5 + 3} = \frac{1.5}{3.5}\ 3 = \frac{3}{7} = 0.42\ K\Omega$$

$$= 0.42 K\Omega.$$

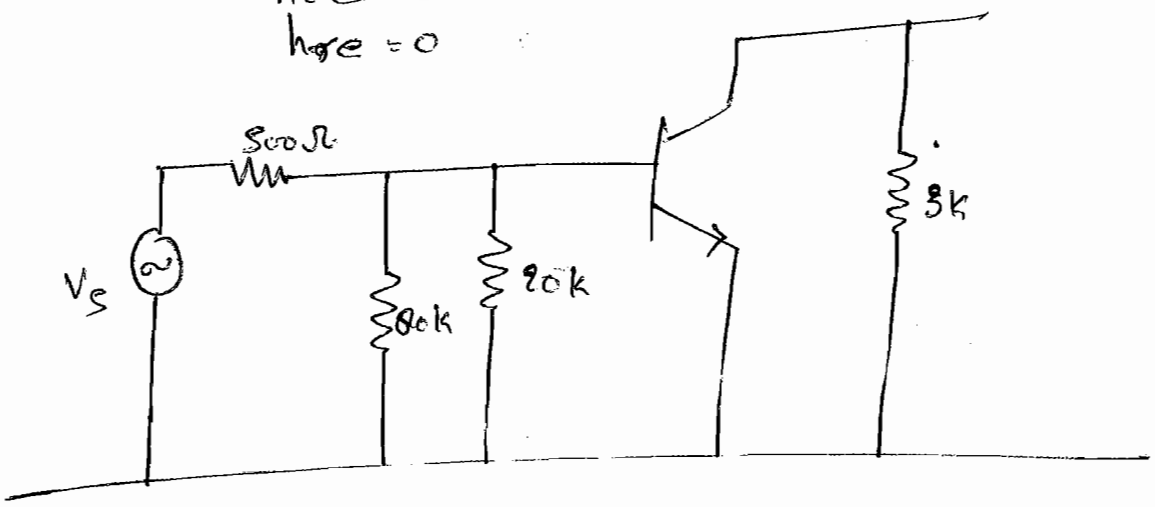
Q. for the previous circuit calculate

Ans $h_{ie} = 1K$

$h_{fe} = 150$

$h_{oe} = 0$

$h_{re} = 0$



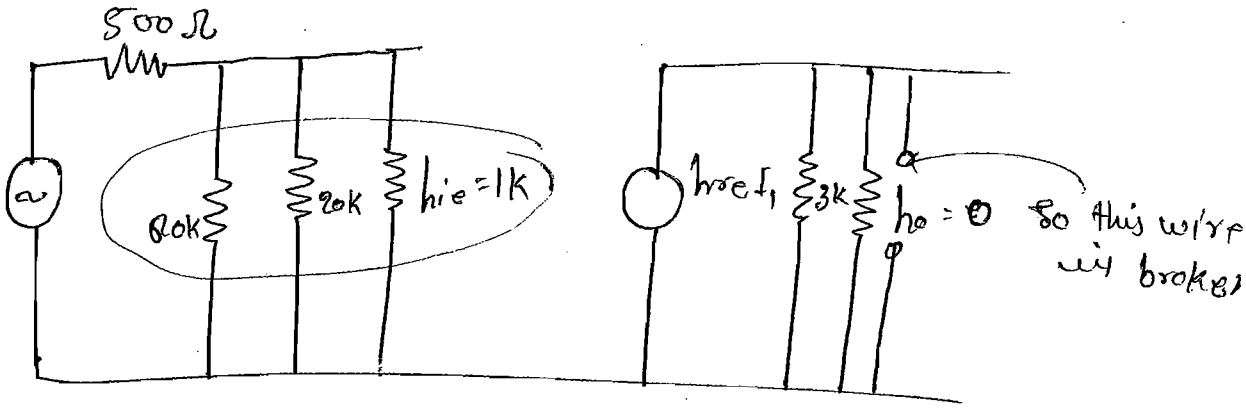
$$A_I = -150$$

$$R_{in} = 1K$$

$$A_V = \frac{-150 \times 3}{1}$$

$$A_V = -450\ K\Omega$$

$$R_o = \frac{1}{h_o} = \infty$$



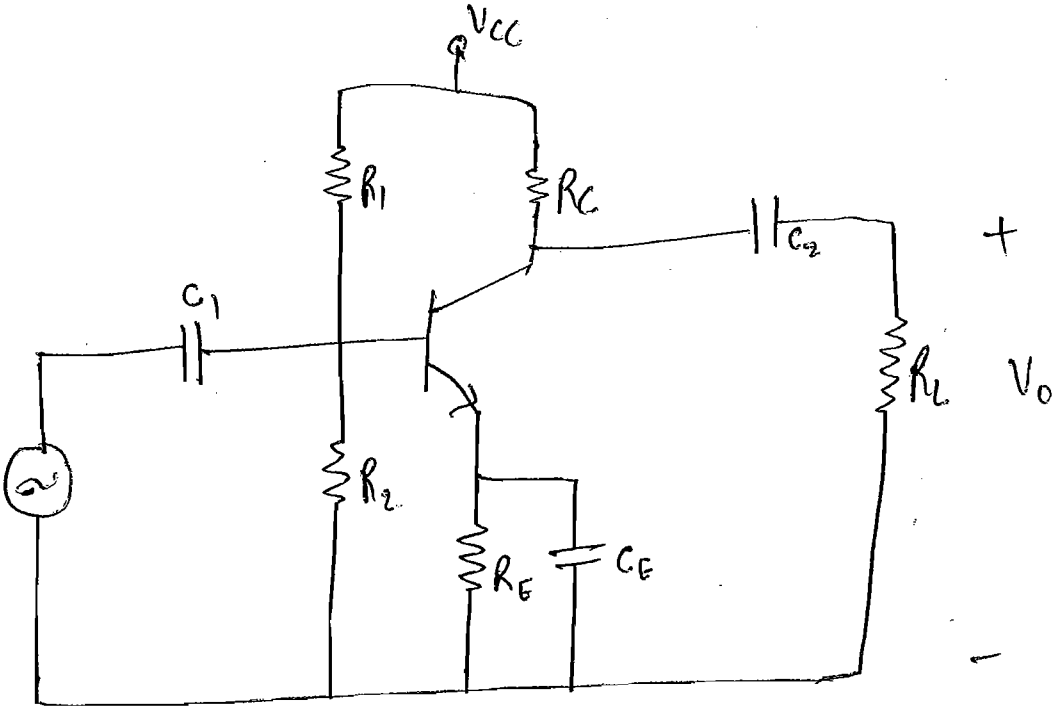
$$= \frac{80 \times 20}{80+20} = \frac{160}{100} \Rightarrow \frac{16 \times 1}{16+1} = \frac{16}{17}$$

$$= \frac{16}{17} + 0.5 = \frac{16 + 8.5}{17}$$

overall i/p resis. = $\frac{24.5}{17}$

overall o/p resistance = $\frac{3\text{K}}{}$

Q.



C_1 = Blocking as well as Coupling Capacitor

C_2 = Blocking Capacitor & Coupling Capacitor

C_G = Bypass Capacitor

R_1 & R_2 → Biasing Resistor

R_C is used for the calculation of V_o in

Chapter-1

Logic Families

These are the technologies which are used to implement the logic function.

Logic Families

Saturated

Those logic families in which the devices inters into saturation region.

- → RTL (Resistor Transister Logic)
- → DCTL (Direct Coupled Transistor Logic)
- → I^2L (Integrated Injected Logic)
- → DTL (Diode Transistor Logic)
- → HTL (High threshold transistor Logic)
- → TTL (Transistor-Transister Logic)

Non-Saturated

Device does not enters in the saturation region.

- → ECL [Emitter Coupled Logic]
- → CMOS [Complementry metal oxide semiconducte technology]

* Characteristic parameters of Logic families :-

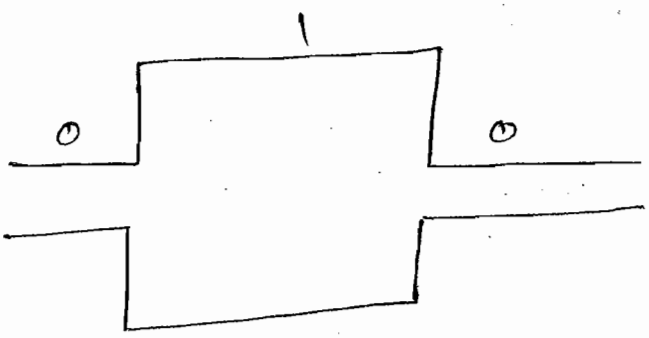
1. Time propagation delay
2. Power dissipation
3. figure of merit (FOM)
4. Fan in
5. Fan Out

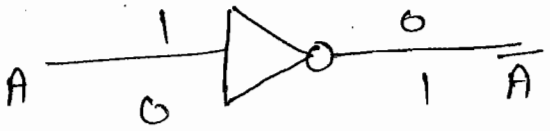
(6) Nois Margin

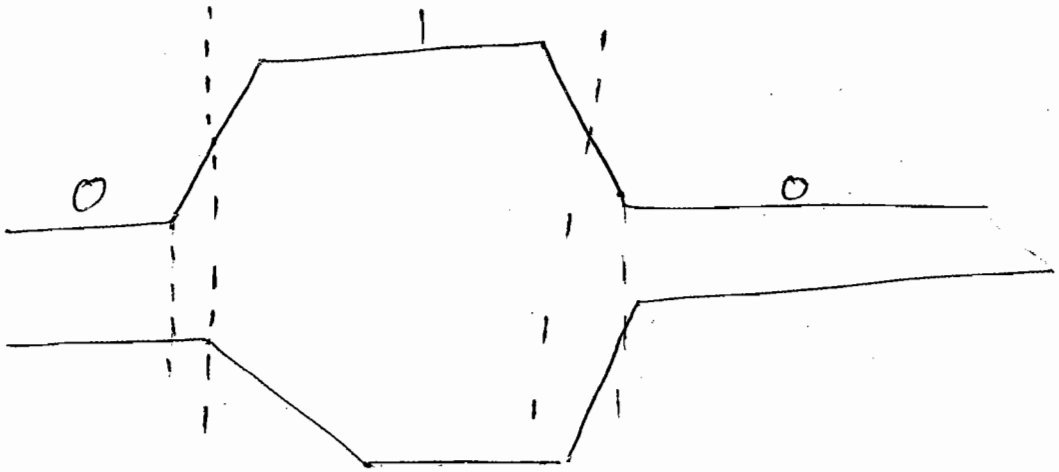
(7) Hi~~g~~d Logic

(1) Time Propagation Delay :-

It is the delay offered by per logic gate normally measured in nano second.







Delay is offered in the logic gate during the transition from high to low or low to high

Imp. ⇒ Fastest Logic family is ECL, HTL is slowest.

(2) Power Dissipation :-

Power expenditure inside the logic gate to produce o/p.

CMOS has minimum power dissipation.
ECL has maximum power dissipation.

(3) Figure of Merit (FOM) :-

Figure of Merit = Power dissipation (n.s) x power dissipation delay (m.w)

Unit → Pico Joule.

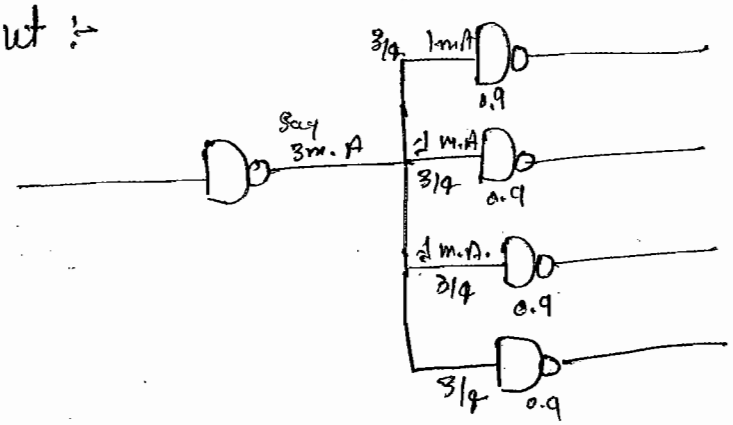
Figure of merit must be as low as possible.
I^2L has best figure of merit
HTL has worst figure of merit.

not imp.

(4) Fan in :-

Maximum no. of i/p.s that can be applied to a logic gate.

(5) Fan Out :-

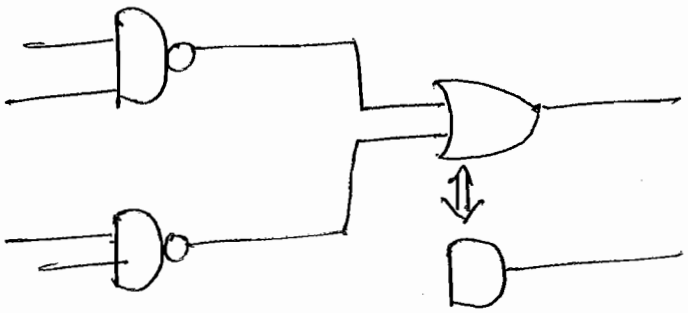


The output of one logic gate can be applied as input to the maximum no. of logic gate of same type is called as fan out.

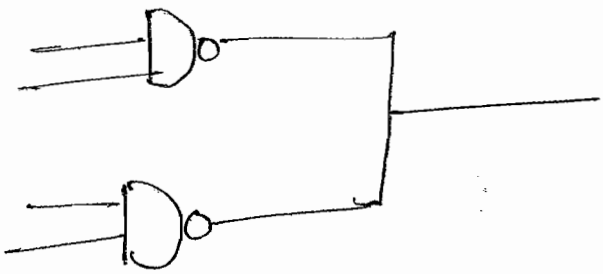
CMOS : Maximum fan out

RTL : Minimum fan out.

⑥ Wired Logic :-



But



The output of two logic gate are joint at a point that point will behave as either OR-gate or AND-gate.

Only ECL behave as wired-OR rest all other logic behave as wired-AND.

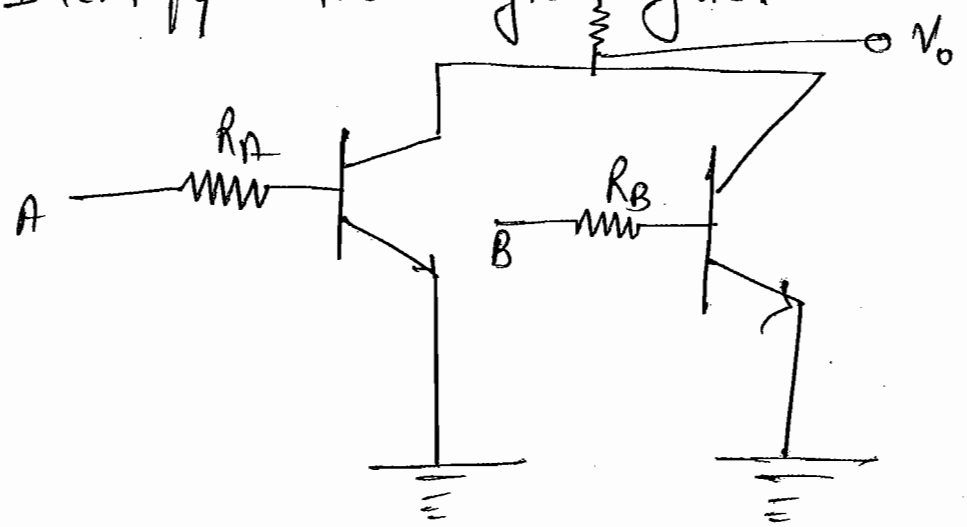
⑦ Noise Margin :-

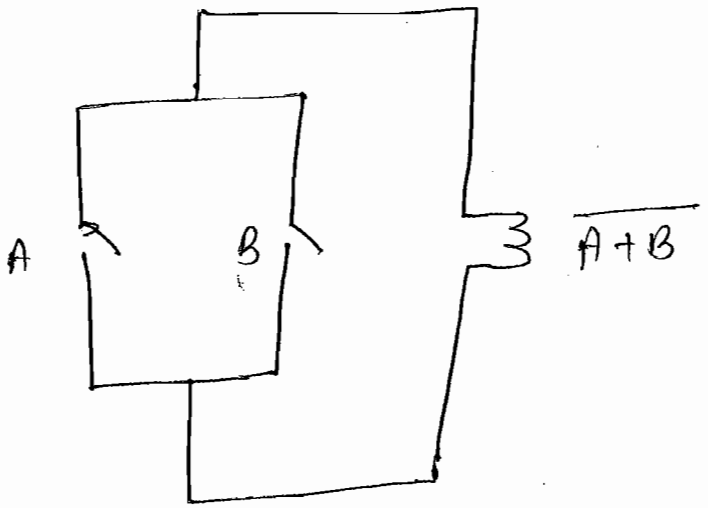
Maximum amount of noise added at the input so that it should not affect the output is called 'Noise Margin.

HTL ⇒ Best Noise Margin.

RTL ⇒ Worst Noise Margin

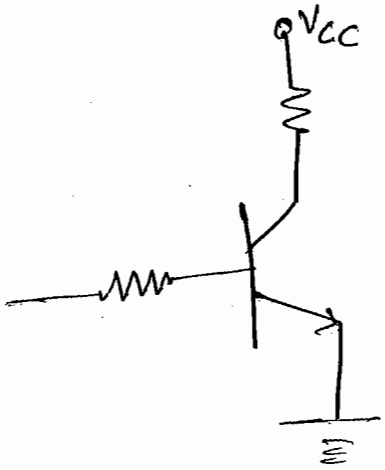
Q. Identify the logic gate.

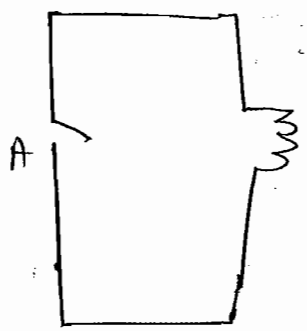




= Not gate.

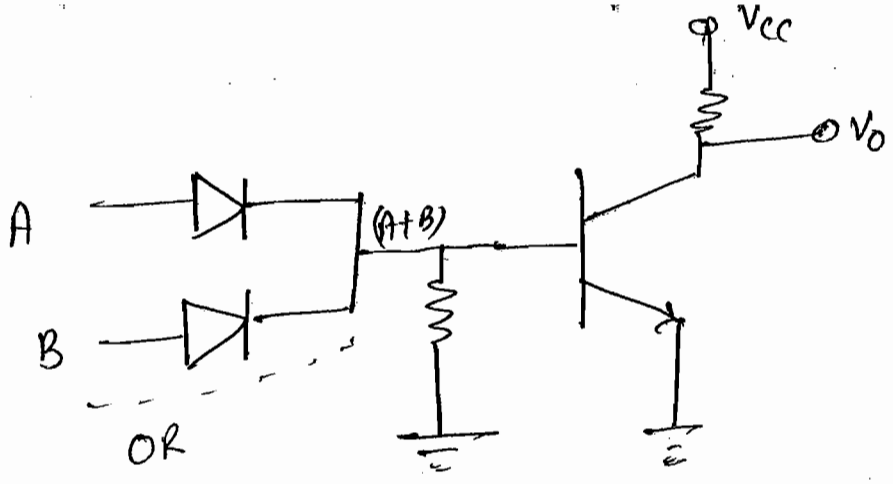
Q. Identify the logic gate.

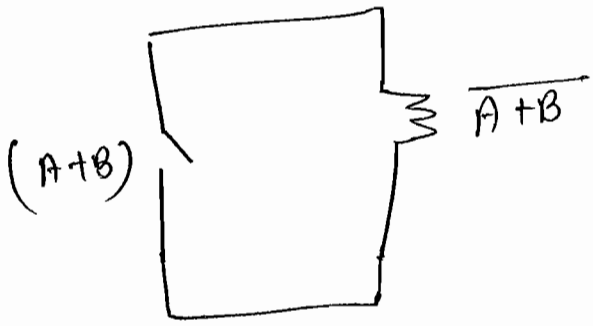




Not.

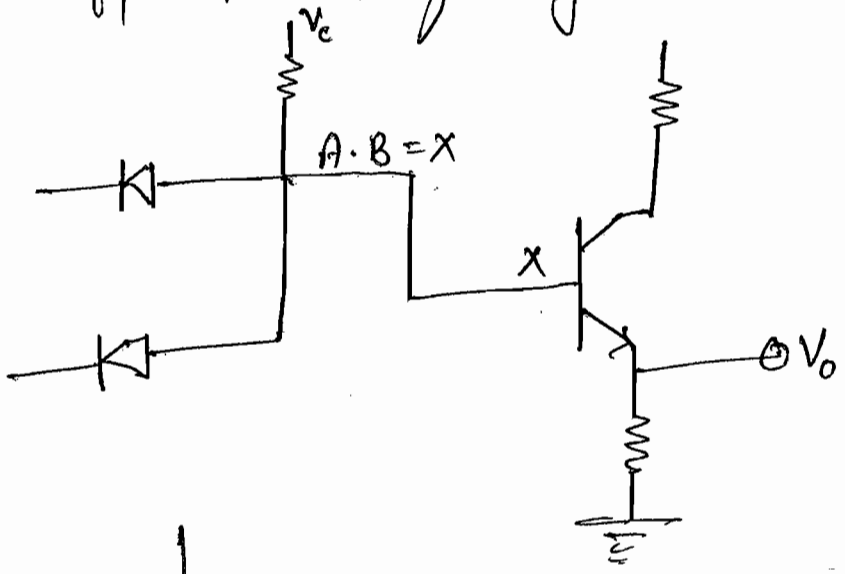
Q.





(Not)

Q. Identify the logic gate



(AND Gate)

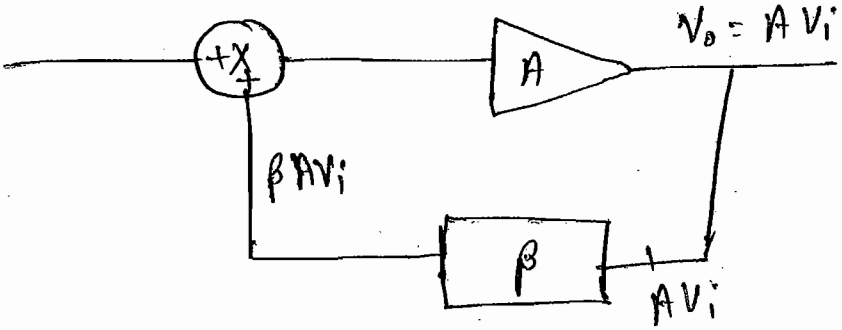
Parameters	RTL/DTL	I^2L	DTL	HTL	TTL	ECL	CM
Time propagation Delay				Slowest		fastest	
Power Dissipation						Max	Min
FOM							
fan out							
Noise Margin							
Hired Logic							
Basic gate							

Oscillators

Those circuit which produces sustained oscillations are called as oscilators.

- Oscillators
  - Sinusoidal
    - Low freq. Osci. [Audio freq.]
      - → R-C phase shift oscillator
      - → Wein's Bridge Oscillator
    - High freq. Osci. [Radio freq.]
      - → Heartly Oscillater
      - → Colpits Oscillater
  - Relaxation Oscillater

In an oscillator always +ve feedback is used.



$\therefore \frac{V_o}{V_{in}} = A$

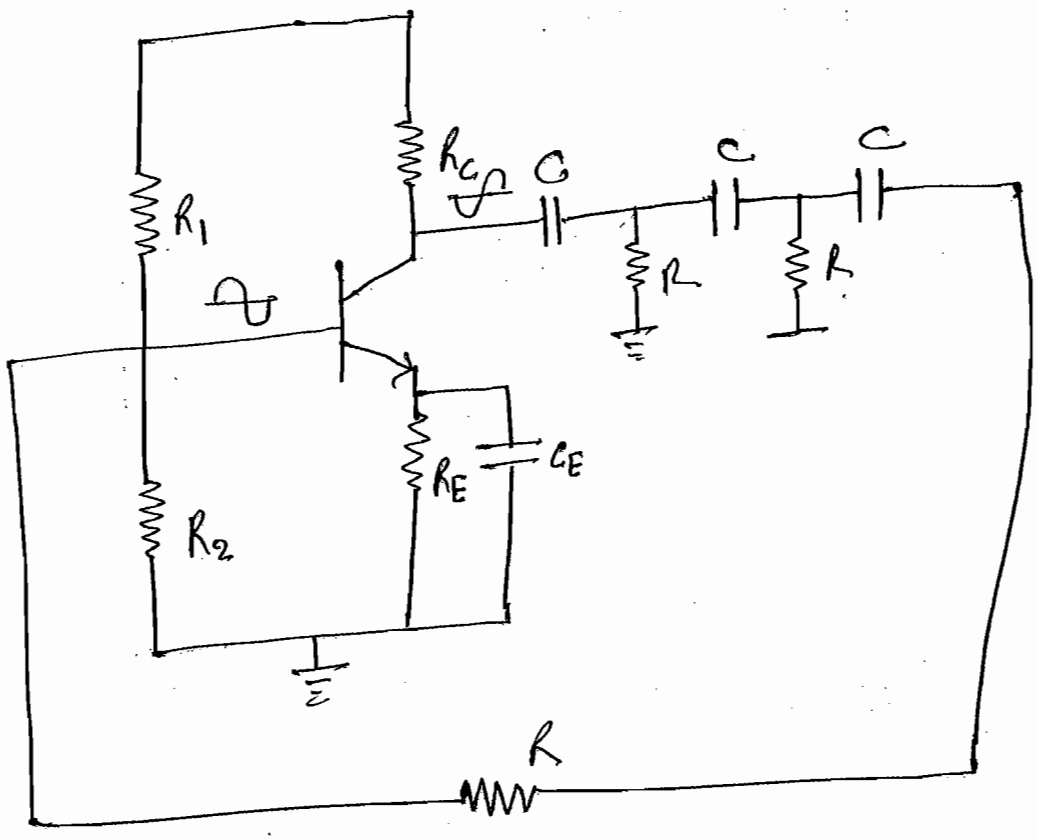
$V_o = AV_i$

Oscillater works without any external applied input.

Any disturbance (Noise) at the input may produce sustained oscillation.

Only if $|A\beta| = 1$ it also called Barkhausen Criteria.

* R-C Phase Shift Oscillater :-



The output of the common emitter configuration produces the phase shift of 180° the additional 3 R-C stages are used to provide a phase shift of additional 180° so that overall phase shift become 360° (0°).